72-Mbit (2 M × 36) Pipelined DCD Sync SRAM

Features

- Supports bus operation up to 250 MHz
- Available speed grade is 250 MHz
- Registered inputs and outputs for pipelined operation
- Optimal for performance (double cycle deselect)
- Depth expansion without wait state
- 3.3 V core power supply (V_{DD})
- 2.5 V and 3.3 V I/O operation
- Fast clock to output times
  - 3.0 ns (for 250 MHz device)
- Provide high performance 3-1-1-1 access rate
- User selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self timed writes
- Asynchronous output enable
- CY7C1484BV33 available in Pb-free 165-ball FBGA package
- IEEE 1149.1 JTAG compatible boundary scan
- "ZZ" sleep mode option

Functional Description

The CY7C1484BV33 SRAM integrates 2 M × 36 SRAM cells with advanced synchronous peripheral circuitry and a 2-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive edge triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address pipelining Chip Enable ($\overline{CE_1}$), depth expansion Chip Enables (CE_2 and $\overline{CE_3}$), Burst Control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), Write Enables ($\overline{BW_X}$, and $\overline{BWE}$), and Global Write ($\overline{GW}$). Asynchronous inputs include the Output Enable ($\overline{OE}$) and the ZZ pin.

Addresses and chip enables are registered at rising edge of clock when either Address Strobe Processor ($\overline{ADSP}$) or Address Strobe Controller ($\overline{ADSC}$) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin ($\overline{ADV}$).

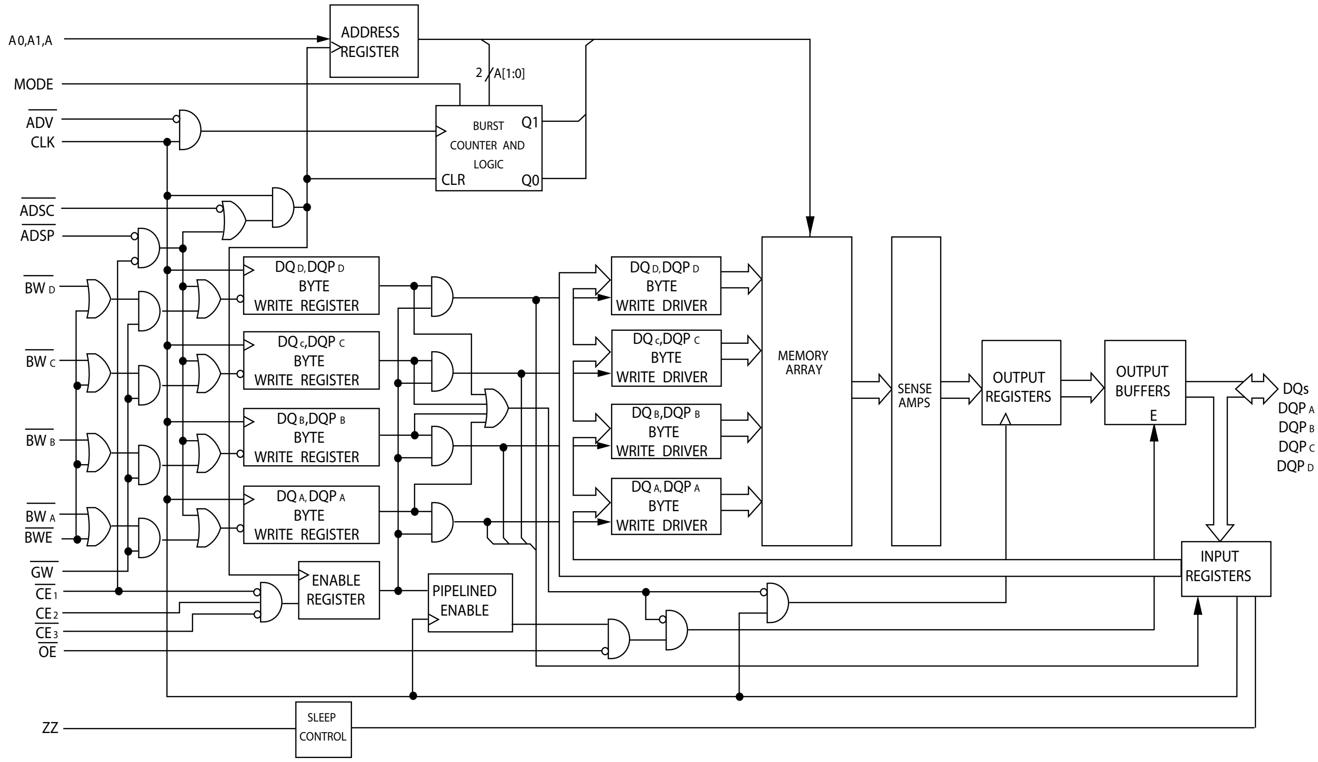
Address, data inputs, and write controls are registered on-chip to initiate a self timed write cycle. This part supports byte write operations (see Pin Definitions on page 5 and Truth Table on page 8 for more information). Write cycles can be one to four bytes wide as controlled by the byte write control inputs. $\overline{GW}$ active LOW causes all bytes to be written. This device incorporates an additional pipelined enable register, which delays turning off the output buffers an additional cycle when a deselect is executed. This feature allows depth expansion without penalizing system performance.

The CY7C1484BV33 operates from a +3.3 V core power supply while all outputs operate with a +3.3 V or a +2.5 V supply. All inputs and outputs are JEDEC standard JESD8-5 compatible.

Selection Guide

Description	250 MHz	Unit
Maximum Access Time	3.0	ns
Maximum Operating Current	500	mA
Maximum CMOS Standby Current	120	mA

Logic Block Diagram – CY7C1484BV33



Contents

Pin Configurations

Figure 1. 165-ball FBGA (15 × 17 × 1.4 mm) pinout

CY7C1484BV33 (2 M × 36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/288M	A	$\overline{CE}_1$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
B	NC/144M	A	CE_2	$\overline{BW}_D$	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC/576M
C	DQP_C	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC/1G	DQP_B
D	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
E	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
F	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
G	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
K	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
L	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
M	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
N	DQP_D	NC	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	DQP_A
P	NC	A	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	A	A	A	TMS	A0	TCK	A	A	A	A

Pin Definitions

Pin Name	I/O	Description
A_0, A_1, A	Input-Synchronous	**Address Inputs Used to Select One of the Address Locations**. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are sampled active. A1:A0 are fed to the 2-bit counter.
$\overline{BW_A}$, $\overline{BW_B}$ $\overline{BW_C}$, $\overline{BW_D}$	Input-Synchronous	**Byte Write Select Inputs, Active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-Synchronous	**Global Write Enable Input, Active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{BW_X}$ and $\overline{BWE}$).
$\overline{BWE}$	Input-Synchronous	**Byte Write Enable Input, Active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input-Clock	**Clock Input**. Capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW during a burst operation.
$\overline{CE_1}$	Input-Synchronous	**Chip Enable 1 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE_3}$ to select or deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH. $\overline{CE_1}$ is sampled only when a new external address is loaded.
CE_2	Input-Synchronous	**Chip Enable 2 Input, Active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $\overline{CE_3}$ to select or deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE_3}$	Input-Synchronous	**Chip Enable 3 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and CE_2 to select or deselect the device. $\overline{CE_3}$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-Asynchronous	**Output Enable, Asynchronous Input, Active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, DQ pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	Input-Synchronous	**Advance Input Signal, Sampled on the Rising Edge of CLK, Active LOW**. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input-Synchronous	**Address Strobe from Processor, Sampled on the Rising Edge of CLK, Active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1:A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ASDP}$ is ignored when $\overline{CE_1}$ is deasserted HIGH.
$\overline{ADSC}$	Input-Synchronous	**Address Strobe from Controller, Sampled on the Rising Edge of CLK, Active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1:A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
ZZ	Input-Asynchronous	**ZZ "Sleep" Input, Active HIGH**. When asserted HIGH, places the device in a non time-critical "sleep" condition with data integrity preserved. For normal operation, this pin must be LOW or left floating. ZZ pin has an internal pull down.
DQs, DQPs	I/O-Synchronous	**Bidirectional Data I/O Lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs and DQP_X are placed in a tri-state condition.
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device**.
V_{SS}	Ground	**Ground for the Core of the Device**.
V_{DDQ}	I/O Power Supply	**Power Supply for the I/O Circuitry**.
MODE	Input-Static	**Selects Burst Order**. When tied to GND, selects linear burst sequence. When tied to V_{DD} or left floating, selects interleaved burst sequence. This is a strap pin and must remain static during device operation. Mode Pin has an internal pull up.
TDO	JTAG Serial Output Synchronous	**Serial Data-Out to the JTAG Circuit**. Delivers data on the negative edge of TCK. If the JTAG feature is not used, this pin must be disconnected.

Pin Definitions (continued)

Pin Name	I/O	Description
TDI	JTAG Serial Input Synchronous	**Serial Data-In to the JTAG Circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not used, this pin can be disconnected or connected to V_{DD}.
TMS	JTAG Serial Input Synchronous	**Serial Data-in to the JTAG Circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not used, this pin can be disconnected or connected to V_{DD}.
TCK	JTAG Clock	**Clock Input to the JTAG Circuitry**. If the JTAG feature is not used, this pin must be connected to V_{SS}.
NC	–	**No Connects**. Not internally connected to the die. 144M, 288M, 576M, and 1G are address expansion pins and are not internally connected to the die.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock.

The CY7C1484BV33 supports secondary cache in systems using either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that use a linear burst sequence. The burst order is user selectable and is determined by sampling the MODE input. Accesses are initiated with either the Processor Address Strobe ($\overline{ADSP}$) or the Controller Address Strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input. A 2-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable ($\overline{BWE}$) and Byte Write Select ($\overline{BW_X}$) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self timed write circuitry.

Synchronous Chip Selects $\overline{CE_1}$, CE_2, $\overline{CE_3}$ and an asynchronous Output Enable ($\overline{OE}$) provide easy bank selection and output tri-state control. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW, (2) chip selects are all asserted active, and (3) the write signals ($\overline{GW}$, $\overline{BWE}$) are all deasserted HIGH. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH. The address presented to the address inputs is stored into the address advancement logic and the address register while being presented to the memory core. The corresponding data is allowed to propagate to the input of the output registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within t_{CO} if $\overline{OE}$ is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state; its outputs are always tri-stated during the first cycle of the access. After the first cycle of the access, the $\overline{OE}$ signal controls the outputs. Consecutive single read cycles are supported.

The CY7C1484BV33 is a double cycle deselect part. After the SRAM is deselected at clock rise by the chip select and either $\overline{ADSP}$ or $\overline{ADSC}$ signals, its output tri-states immediately after the next clock rise.

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when both the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ is asserted LOW and (2) chip select is asserted active. The address presented is loaded into the address register and the address advancement logic while being delivered to the memory core. The write signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW_X}$) and $\overline{ADV}$ inputs are ignored during this first cycle.

$\overline{ADSP}$ triggered write accesses require two clock cycles to complete. If $\overline{GW}$ is asserted LOW on the second clock rise, the data presented to the DQ_x inputs is written into the corresponding address location in the memory core. If $\overline{GW}$ is HIGH, then the $\overline{BWE}$ and $\overline{BW_X}$ signals control the write operation. The CY7C1484BV33 provides byte write capability that is described in the Truth Table on page 8. Asserting the Byte Write Enable input ($\overline{BWE}$) with the selected byte write input selectively writes to only the desired bytes. Bytes not selected during a byte write operation remain unaltered. A synchronous self timed write mechanism is provided to simplify the write operations.

Because the CY7C1484BV33 is a common I/O device, the Output Enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the DQ inputs. Doing so tri-states the output drivers. As a safety precaution, DQ are automatically tri-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by $\overline{ADSC}$

$\overline{ADSC}$ write accesses are initiated when the following conditions are satisfied: (1) $\overline{ADSC}$ is asserted LOW, (2) $\overline{ADSP}$ is deasserted HIGH, (3) chip select is asserted active, and (4) the appropriate combination of the write inputs ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW_X}$) are asserted active to conduct a write to the desired bytes. $\overline{ADSC}$ triggered write accesses require a single clock cycle to complete. The address presented is loaded into the address register and the address advancement logic while being delivered to the memory core. The $\overline{ADV}$ input is ignored during this cycle. If a global write is conducted, the data presented to the DQ_X is written into the corresponding address location in the memory core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation remain unaltered. A synchronous self timed write mechanism is provided to simplify the write operations.

Because the CY7C1484BV33 is a common I/O device, the Output Enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the DQ_X inputs. Doing so tri-states the output drivers. As a safety precaution, DQ_X are automatically tri-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The CY7C1484BV33 provides a 2-bit wraparound counter, fed by $A_{[1:0]}$, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input. Both read and write burst operations are supported.

Asserting $\overline{ADV}$ LOW at clock rise automatically increments the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

Sleep Mode

The ZZ input pin is asynchronous. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected before entering the “sleep” mode. $\overline{CE}$s, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table (MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table (MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	$ZZ \geq V_{DD} – 0.2$ V	–	120	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} – 0.2$ V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2$ V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ Active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

Truth Table

The truth table for CY7C1484BV33 follows. [1, 2, 3, 4, 5]

Operation	Address Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect Cycle, Power Down	None	H	X	X	L	X	L	X	X	X	L–H	Tri-State
Deselect Cycle, Power Down	None	L	L	X	L	L	X	X	X	X	L–H	Tri-State
Deselect Cycle, Power Down	None	L	X	H	L	L	X	X	X	X	L–H	Tri-State
Deselect Cycle, Power Down	None	L	L	X	L	H	L	X	X	X	L–H	Tri-State
Deselect Cycle, Power Down	None	L	X	H	L	H	L	X	X	X	L–H	Tri-State
Sleep Mode, Power Down	None	X	X	X	H	X	X	X	X	X	X	Tri-State
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L–H	Q
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L–H	Tri-State
Write Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L–H	D
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L–H	Q
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L–H	Tri-State
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L–H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L–H	Tri-State
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L–H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L–H	Tri-State
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L–H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L–H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L–H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L–H	Tri-State
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L–H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L–H	Tri-State
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L–H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L–H	D

Notes
1. X = Don't Care, H = Logic HIGH, L = Logic LOW.
2. $\overline{WRITE}$ = L when any one or more Byte Write Enable signals and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all Byte Write Enable signals, $\overline{BWE}$, $\overline{GW}$ = H.
3. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
4. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW_X}$. Writes can occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to enable the outputs to tri-state. $\overline{OE}$ is a don't care for the remainder of the write cycle.
5. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tri-state when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Truth Table for Read/Write

The read/write truth table for CY7C1484BV33 and follows. [6, 7]

Function (CY7C1484BV33)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_D$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{BW}_A$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte A – (DQ_A and DQP_A)	H	L	H	H	H	L
Write Byte B – (DQ_B and DQP_B)	H	L	H	H	L	H
Write Bytes B, A	H	L	H	H	L	L
Write Byte C – (DQ_C and DQP_C)	H	L	H	L	H	H
Write Bytes C, A	H	L	H	L	H	L
Write Bytes C, B	H	L	H	L	L	H
Write Bytes C, B, A	H	L	H	L	L	L
Write Byte D – (DQ_D and DQP_D)	H	L	L	H	H	H
Write Bytes D, A	H	L	L	H	H	L
Write Bytes D, B	H	L	L	H	L	H
Write Bytes D, B, A	H	L	L	H	L	L
Write Bytes D, C	H	L	L	L	H	H
Write Bytes D, C, A	H	L	L	L	H	L
Write Bytes D, C, B	H	L	L	L	L	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

Notes

6. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
7. Table includes only a partial listing of the byte write combinations. Any combination of $\overline{BW}_X$ is valid. Appropriate write is based on which byte write is active.

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1484BV33 incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC standard 3.3 V or 2.5 V I/O logic levels.

The CY7C1484BV33 contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, tie TCK LOW (V_{SS}) to prevent device clocking. TDI and TMS are internally pulled up and may be unconnected. They may alternatively be connected to V_{DD} through a pull up resistor. TDO must be left unconnected. During power up, the device comes up in a reset state, which does not interfere with the operation of the device.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input gives commands to the TAP controller and is sampled on the rising edge of TCK. it is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI ball serially inputs information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information about loading the instruction register, see the TAP Controller State Diagram on page 12. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register.

Test Data-Out (TDO)

The TDO output ball serially clocks data-out from the registers. Whether the output is active depends on the current state of the TAP state machine (see Identification Codes on page 16). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

Perform a RESET by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

During power up, the TAP is reset internally to ensure that TDO comes up in a High Z state.

TAP Registers

Registers are connected between the TDI and TDO balls to scan the data in and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions are serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls, as shown in the TAP Controller Block Diagram on page 13. During power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary ‘01’ pattern to enable fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single bit register that is placed between the TDI and TDO balls. This enables shifting of data through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM. The x36 configuration has a 73-bit long register and the x18 configuration has a 54-bit long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller moves to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions are used to capture the contents of the I/O ring.

The Boundary Scan Exit Order on page 17 show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in Identification Register Definitions on page 16.

TAP Instruction Set

Overview

Eight different instructions are possible with the 3-bit instruction register. All combinations are listed in Identification Codes on page 16. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in detail in this section.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented.

The TAP controller cannot be used to load address data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction after it is shifted in, the TAP controller must be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction that is executed whenever the instruction register is loaded with all zeros. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1. The TAP controller does recognize an all-zero instruction.

When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction is loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High Z state.

IDCODE

The IDCODE instruction loads a vendor specific, 32-bit code into the instruction register. It also places the instruction register between the TDI and TDO balls and shifts the IDCODE out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register at power up or whenever the TAP controller is in a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1 compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register.

Be aware that the TAP controller clock only operates at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output may undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that may be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (t_{CS} plus t_{CH}).

The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CLK captured in the boundary scan register.

After the data is captured, shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO balls.

Note that because the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction has the same effect as the Pause-DR command.

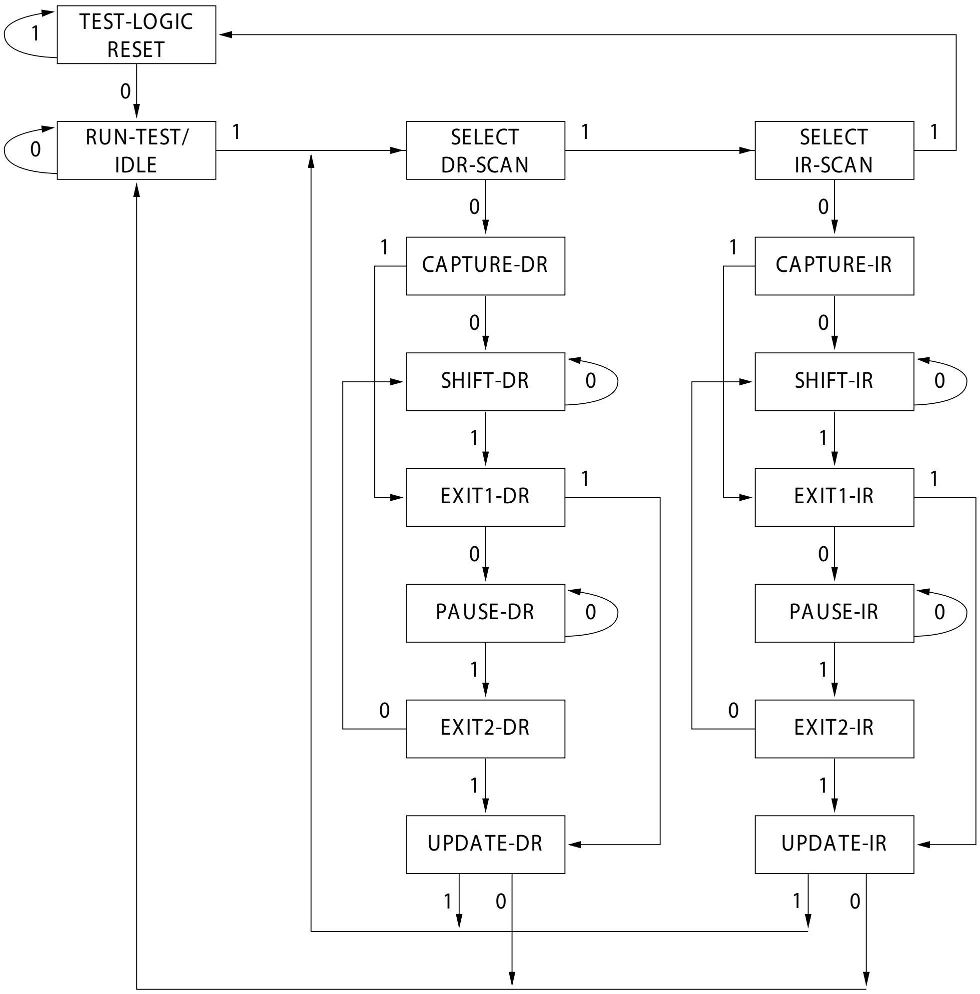
BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

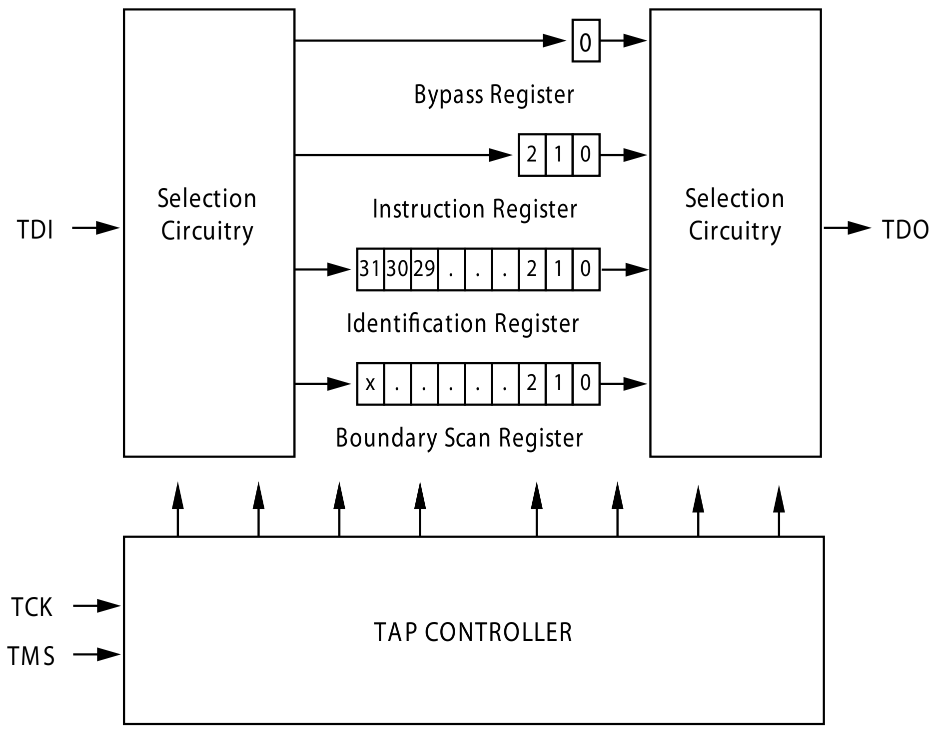
These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram



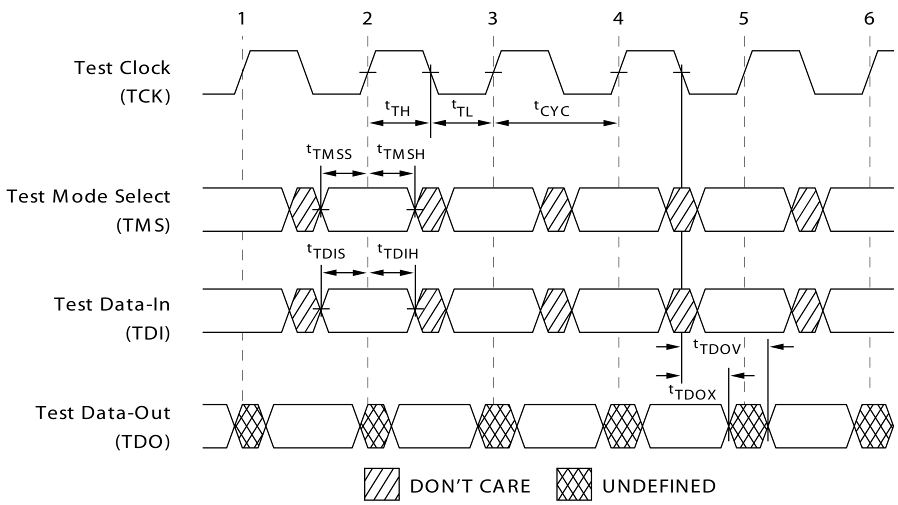
The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Timing

Figure 2. TAP Timing



TAP AC Switching Characteristics

Over the Operating Range

Parameter [8, 9]	Description	Min	Max	Unit
Clock				
t_{TCYC}	TCK Clock Cycle Time	50	–	ns
t_{TF}	TCK Clock Frequency	–	20	MHz
t_{TH}	TCK Clock HIGH Time	20	–	ns
t_{TL}	TCK Clock LOW Time	20	–	ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid	–	10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0	–	ns
Setup Times				
t_{TMSS}	TMS Setup to TCK Clock Rise	5	–	ns
t_{TDIS}	TDI Setup to TCK Clock Rise	5	–	ns
t_{CS}	Capture Setup to TCK Rise	5	–	ns
Hold Times				
t_{TMSH}	TMS hold after TCK Clock Rise	5	–	ns
t_{TDIH}	TDI Hold after Clock Rise	5	–	ns
t_{CH}	Capture Hold after Clock Rise	5	–	ns

Notes

8. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
9. Test conditions are specified using the load in TAP AC Test Conditions. t_R/t_F = 1 ns.

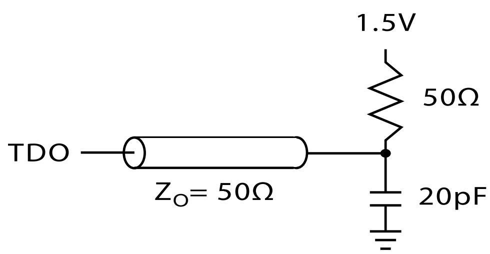
3.3 V TAP AC Test Conditions

Input pulse levels .... V_{SS} to 3.3 V
Input rise and fall times ....1 ns
Input timing reference levels .... 1.5 V
Output reference levels .... 1.5 V
Test load termination supply voltage .... 1.5 V

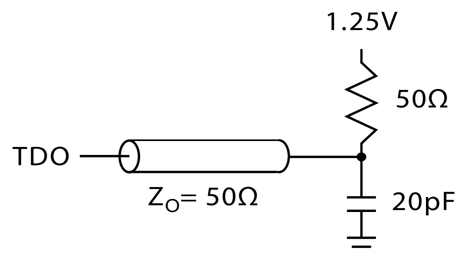
2.5 V TAP AC Test Conditions

Input pulse levels .... V_{SS} to 2.5 V
Input rise and fall time ....1 ns
Input timing reference levels .... 1.25 V
Output reference levels .... 1.25 V
Test load termination supply voltage .... 1.25 V

3.3 V TAP AC Output Load Equivalent



2.5 V TAP AC Output Load Equivalent



TAP DC Electrical Characteristics and Operating Conditions

(0 °C < T_A < +70 °C; V_{DD} = 3.135 V to 3.6 V unless otherwise noted)

Parameter [11]	Description	Test Conditions		Min	Max	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –4.0 mA, V_{DDQ} = 3.3 V		2.4	–	V
		I_{OH} = –1.0 mA, V_{DDQ} = 2.5 V		2.0	–	V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	V_{DDQ} = 3.3 V	2.9	–	V
			V_{DDQ} = 2.5 V	2.1	–	V
V_{OL1}	Output LOW Voltage	I_{OL} = 8.0 mA, V_{DDQ} = 3.3 V		–	0.4	V
		I_{OL} = 1.0 mA, V_{DDQ} = 2.5 V		–	0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA	V_{DDQ} = 3.3 V	–	0.2	V
			V_{DDQ} = 2.5 V	–	0.2	V
V_{IH}	Input HIGH Voltage	V_{DDQ} = 3.3 V		2.0	V_{DD} + 0.3	V
		V_{DDQ} = 2.5 V		1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage	V_{DDQ} = 3.3 V		–0.5	0.7	V
		V_{DDQ} = 2.5 V		–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_{IN} ≤ V_{DDQ}		–5	5	µA

Note
11. All voltages refer to V_{SS} (GND).

Identification Register Definitions

Bit# 24 is "1" in the ID Register definitions for both 2.5 V and 3.3 V versions of the device.

Instruction Field	CY7C1484BV33 (2 M × 36)	Description
Revision Number (31:29)	000	Describes the version number
Device Depth (28:24)	01011	Reserved for internal use
Architecture/Memory Type(23:18)	000110	Defines memory type and architecture
Bus Width/Density (17:12)	100100	Defines width and density
Cypress JEDEC ID Code (11:1)	00000110100	Enables unique identification of SRAM vendor
ID Register Presence Indicator (0)	1	Indicates the presence of an ID register

Scan Register Sizes

Register Name	Bit Size (× 36)
Instruction	3
Bypass	1
ID	32
Boundary Scan Order – 165-ball FBGA	73

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

Boundary Scan Exit Order

(2 M × 36)

Bit #	165-Ball ID
1	C1
2	D1
3	E1
4	D2
5	E2
6	F1
7	G1
8	F2
9	G2
10	J1
11	K1
12	L1
13	J2
14	M1
15	N1
16	K2
17	L2
18	M2
19	R1
20	R2

Bit #	165-Ball ID
21	R3
22	P2
23	R4
24	P6
25	R6
26	N6
27	P11
28	R8
29	P3
30	P4
31	P8
32	P9
33	P10
34	R9
35	R10
36	R11
37	N11
38	M11
39	L11
40	M10

Bit #	165-Ball ID
41	L10
42	K11
43	J11
44	K10
45	J10
46	H11
47	G11
48	F11
49	E11
50	D10
51	D11
52	C11
53	G10
54	F10
55	E10
56	A10
57	B10
58	A9
59	B9
60	A8

Bit #	165-Ball ID
61	B8
62	A7
63	B7
64	B6
65	A6
66	B5
67	A5
68	A4
69	B4
70	B3
71	A3
72	A2
73	B2

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .... –65 °C to +150 °C

Ambient Temperature with Power Applied .... –55 °C to +125 °C

Supply Voltage on V_{DD} Relative to GND .....–0.5 V to +4.6 V

Supply Voltage on V_{DDQ} Relative to GND .... –0.5 V to $+V_{DD}$

DC Voltage Applied to Outputs in Tri-State ....–0.5 V to V_{DDQ} + 0.5 V

DC Input Voltage ....–0.5 V to V_{DD} + 0.5 V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) .... >2001 V

Latch Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}
Industrial	–40 °C to +85 °C		

Electrical Characteristics

Over the Operating Range

Parameter [12, 13]	Description	Test Conditions	Min	Max	Unit
V_{DD}	Power Supply Voltage		3.135	3.6	V
V_{DDQ}	I/O Supply Voltage	For 3.3 V I/O	3.135	V_{DD}	V
		For 2.5 V I/O	2.375	2.625	V
V_{OH}	Output HIGH Voltage	For 3.3 V I/O, I_{OH} = –4.0 mA	2.4	–	V
		For 2.5 V I/O, I_{OH} = –1.0 mA	2.0	–	V
V_{OL}	Output LOW Voltage	For 3.3 V I/O, I_{OL} = 8.0 mA	–	0.4	V
		For 2.5 V I/O, I_{OL} = 1.0 mA	–	0.4	V
V_{IH}	Input HIGH Voltage [12]	For 3.3 V I/O	2.0	V_{DD} + 0.3 V	V
		For 2.5 V I/O	1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW Voltage [12]	For 3.3 V I/O	–0.3	0.8	V
		For 2.5 V I/O	–0.3	0.7	V
I_X	Input Leakage Current Except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}	–5	5	µA
	Input Current of MODE	Input = V_{SS}	–30	–	µA
		Input = V_{DD}	–	5	µA
	Input Current of ZZ	Input = V_{SS}	–5	–	µA
		Input = V_{DD}	–	30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ $V_{DDQ,}$ Output Disabled	–5	5	µA
I_{DD} [14]	V_{DD} Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC} — 4 ns cycle, 250 MHz	–	500	mA
I_{SB1}	Automatic CE Power Down Current – TTL Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX} = 1/t_{CYC} — 4 ns cycle, 250 MHz	–	245	mA
I_{SB2}	Automatic CE Power Down Current – CMOS Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V, f = 0 — 4 ns cycle, 250 MHz	–	120	mA

Notes

12. Overshoot: $V_{IH(AC)} < V_{DD}$ +1.5 V (pulse width less than t_{CYC}/2). Undershoot: $V_{IL(AC)}$ > –2 V (pulse width less than t_{CYC}/2).
13. Power up: assumes a linear ramp from 0 V to $V_{DD(minimum)}$ within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \le V_{DD}$.
14. The operation current is calculated with 50% read cycle and 50% write cycle.

Electrical Characteristics (continued)

Over the Operating Range

Parameter [12, 13]	Description	Test Conditions		Min	Max	Unit
I_{SB3}	Automatic CE Power Down Current – CMOS Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V, $f = f_{MAX} = 1/t_{CYC}$	4 ns cycle, 250 MHz	–	245	mA
I_{SB4}	Automatic CE Power Down Current – TTL Inputs	V_{DD} = Max, Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = 0	4 ns cycle, 250 MHz	–	135	mA

Capacitance

Parameter [15]	Description	Test Conditions	165-ball FBGA Package	Unit
$C_{ADDRESS}$	Address Input Capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 2.5 V	6	pF
C_{DATA}	Data Input Capacitance		5	pF
C_{CTRL}	Control Input Capacitance		8	pF
C_{CLK}	Clock Input Capacitance		6	pF
C_{IO}	Input/Output Capacitance		5	pF

Thermal Resistance

Parameter [15]	Description	Test Conditions	165-ball FBGA Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	16.3	°C/W
Θ_{JC}	Thermal resistance (junction to case)		2.1	°C/W

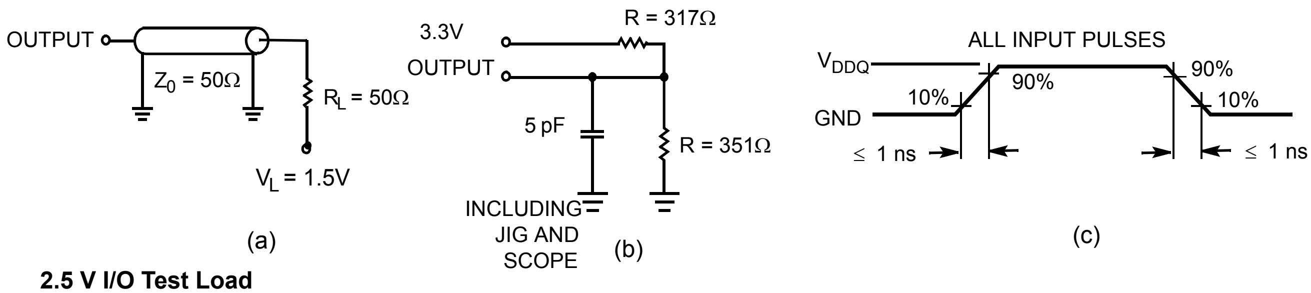
Note

15. Tested initially and after any design or process change that may affect these parameters.

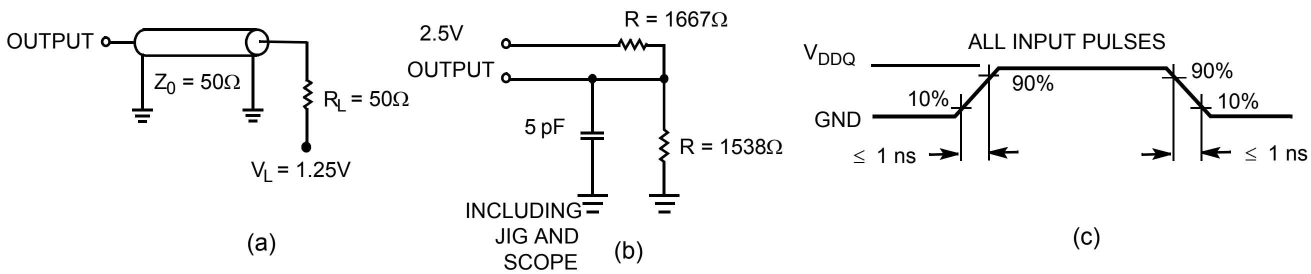
AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms

3.3 V I/O Test Load



2.5 V I/O Test Load



Switching Characteristics

Over the Operating Range

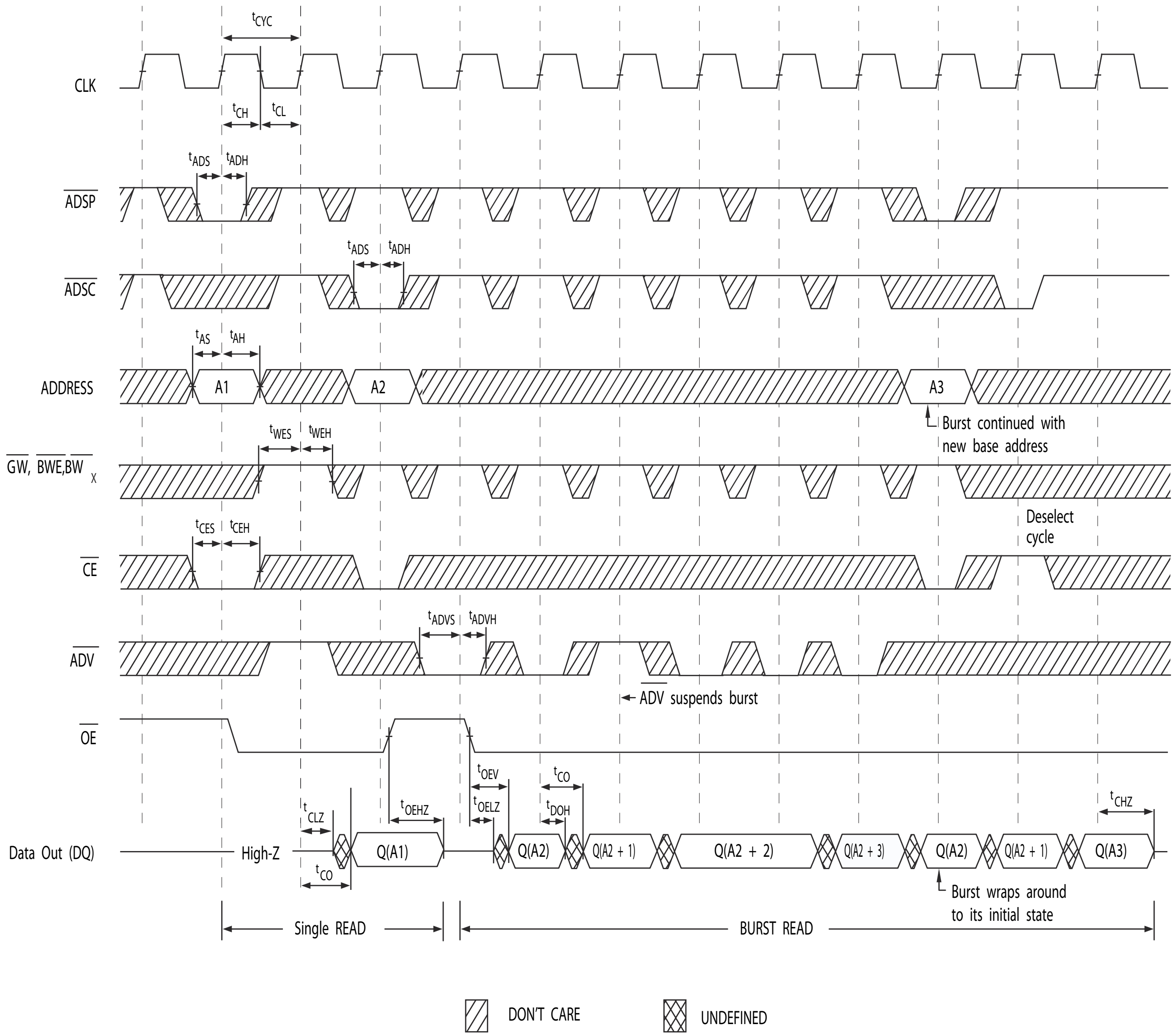
Parameter [16, 17]	Description	250 MHz		Unit
		Min	Max	
t_{POWER}	V_{DD}(typical) to the First Access [18]	1	–	ms
Clock				
t_{CYC}	Clock Cycle Time	4	–	ns
t_{CH}	Clock HIGH	2.0	–	ns
t_{CL}	Clock LOW	2.0	–	ns
Output Times				
t_{CO}	Data Output Valid After CLK Rise	–	3.0	ns
t_{DOH}	Data Output Hold After CLK Rise	1.3	–	ns
t_{CLZ}	Clock to Low Z [19, 20, 21]	1.3	–	ns
t_{CHZ}	Clock to High Z [19, 20, 21]	–	3.0	ns
t_{OEV}	$\overline{OE}$ LOW to Output Valid	–	3.0	ns
t_{OELZ}	$\overline{OE}$ LOW to Output Low Z [19, 20, 21]	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to Output High Z [19, 20, 21]	–	3.0	ns
Setup Times				
t_{AS}	Address Setup Before CLK Rise	1.4	–	ns
t_{ADS}	$\overline{ADSC}$, $\overline{ADSP}$ Setup Before CLK Rise	1.4	–	ns
t_{ADVS}	$\overline{ADV}$ Setup Before CLK Rise	1.4	–	ns
t_{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ Setup Before CLK Rise	1.4	–	ns
t_{DS}	Data Input Setup Before CLK Rise	1.4	–	ns
t_{CES}	Chip Enable Setup Before CLK Rise	1.4	–	ns
Hold Times				
t_{AH}	Address Hold After CLK Rise	0.4	–	ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.4	–	ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.4	–	ns
t_{WEH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ Hold After CLK Rise	0.4	–	ns
t_{DH}	Data Input Hold After CLK Rise	0.4	–	ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.4	–	ns

Notes

16. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
17. Test conditions shown in (a) of Figure 3 on page 20 unless otherwise noted.
18. This part has an internal voltage regulator; t_{POWER} is the time that the power is supplied above $V_{DD(minimum)}$ initially before a read or write operation can be initiated.
19. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of Figure 3 on page 20. Transition is measured ±200 mV from steady-state voltage.
20. At any supplied voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z before Low Z under the same system conditions.
21. This parameter is sampled and not 100% tested.

Switching Waveforms

Figure 4. Read Cycle Timing [22]

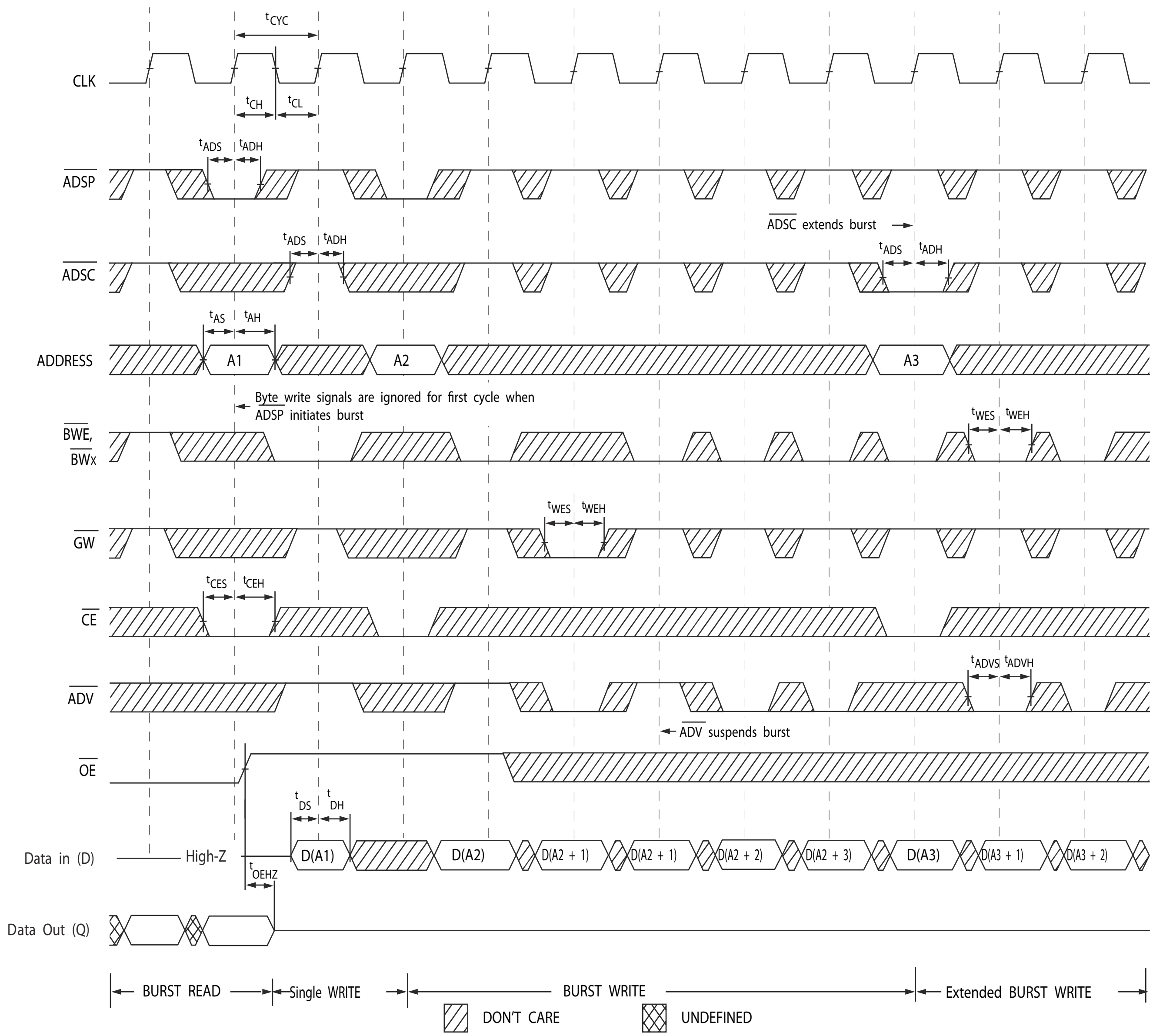


Note

22. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH, and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH, CE_2 is LOW, or $\overline{CE}_3$ is HIGH.

Switching Waveforms (continued)

Figure 5. Write Cycle Timing [23, 24]

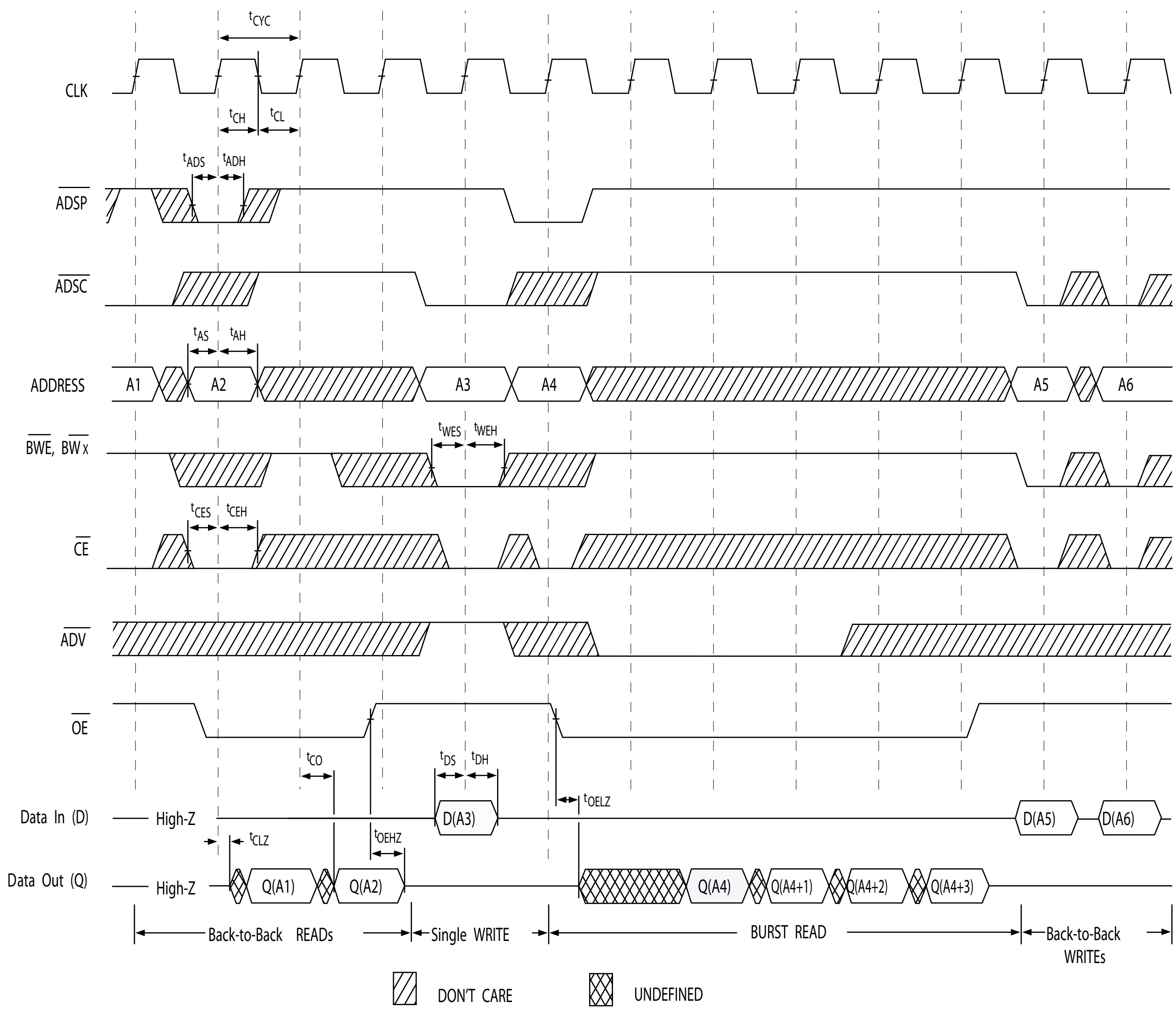


Notes

23. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH, and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH, CE_2 is LOW, or $\overline{CE}_3$ is HIGH.
24. Full width write is initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW, and $\overline{BW}_X$ LOW.

Switching Waveforms (continued)

Figure 6. Read/Write Cycle Timing [25, 26, 27]

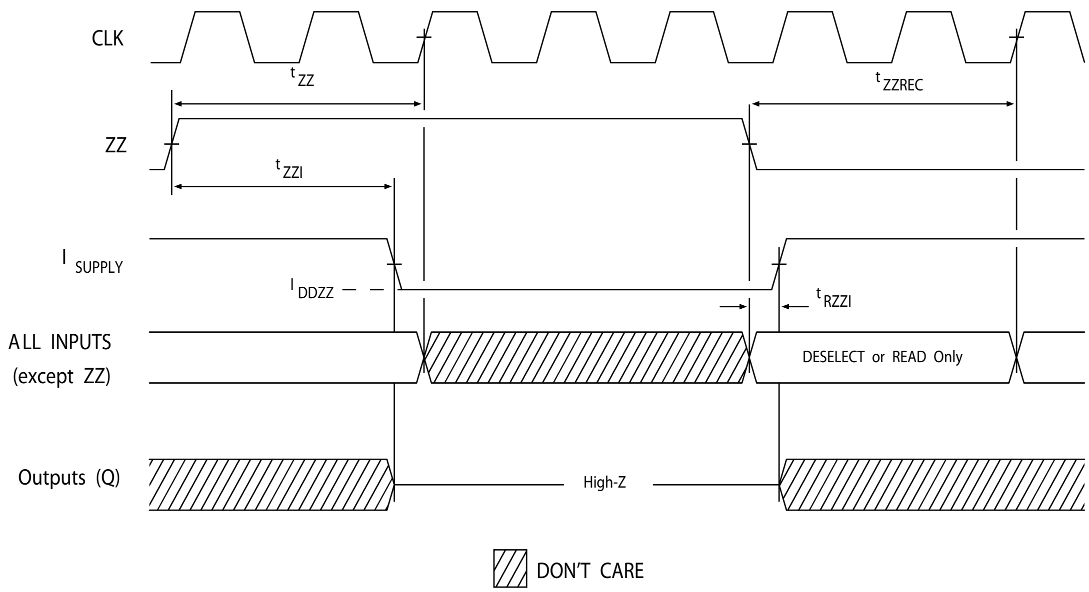


Notes

25. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE_1}$ is LOW, CE_2 is HIGH, and $\overline{CE_3}$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE_1}$ is HIGH, CE_2 is LOW, or $\overline{CE_3}$ is HIGH.
26. The data bus (Q) remains in High Z following a write cycle unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
27. $\overline{GW}$ is HIGH.

Switching Waveforms (continued)

Figure 7. ZZ Mode Timing [28, 29]



Notes

28. Device must be deselected when entering ZZ mode. See Truth Table on page 8 for all possible signal conditions to deselect the device.
29. DQs are in High Z when exiting ZZ sleep mode.

Ordering Information

Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
250	CY7C1484BV33-250BZXC	51-85165	165-ball FBGA (15 × 17 × 1.4 mm) Pb-free	Commercial

Ordering Code Definitions

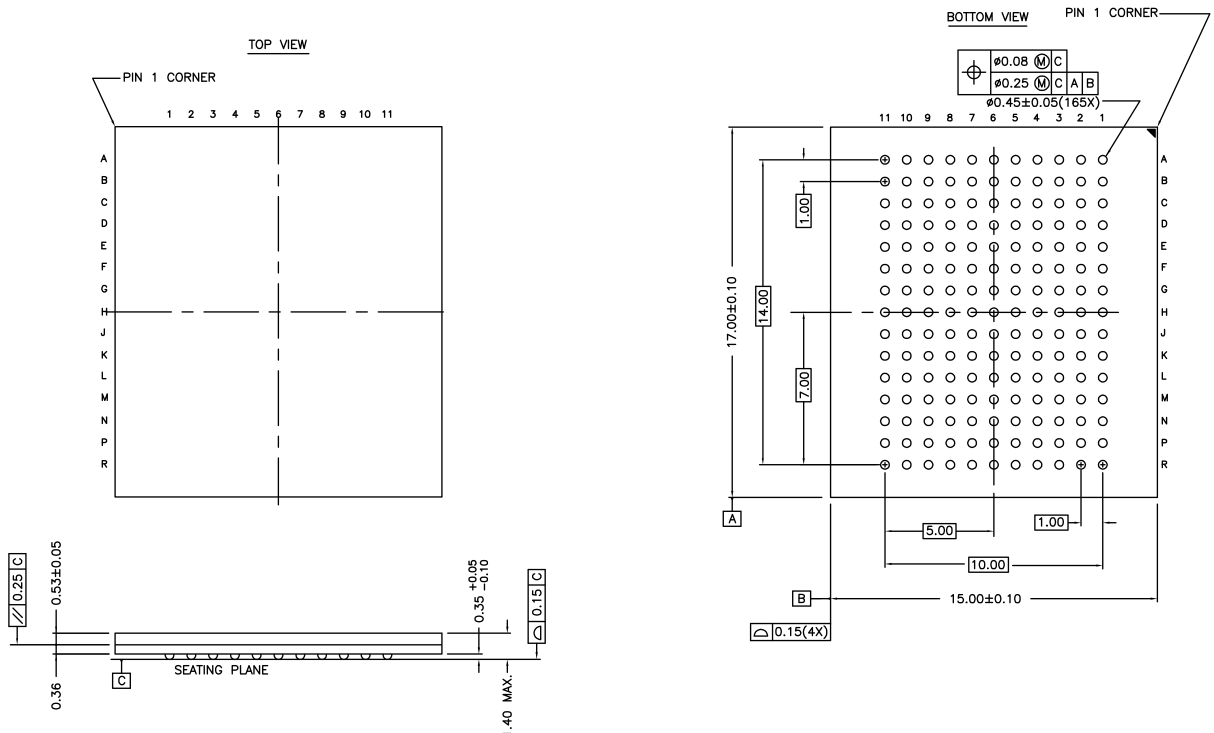
CY 7 C 1484 B V33 - 250 BZ X C

- Temperature range: C = Commercial = 0 °C to +70 °C
- X = Pb-free
- Package Type: BZ = 165-ball FBGA
- Speed Grade: 250 MHz
- V33 = 3.3 V
- Process Technology: B ≥ errata fix PCN084636
- Part Identifier: 1484 = DCD, 2 M × 36 (72 Mb)
- Technology Code: C = CMOS
- Marketing Code: 7 = SRAM
- Company ID: CY = Cypress

Package Diagrams

Figure 8. 165-ball FBGA (15 × 17 × 1.40 mm) (0.45 Ball Diameter) Package Outline, 51-85165

NOTES:
SOLDER PAD TYPE: SOLDER MASK DEFINED (SMD)
PACKAGE WEIGHT: 0.60g
JEDEC REFERENCE: MO-216 / ISSUE E
PACKAGE CODES: BB0AA / BW0AG



51-85165 *D

Acronyms

Acronym	Description
$\overline{CE}$	chip enable
CMOS	complementary metal-oxide-semiconductor
EIA	electronic industries alliance
FBGA	fine-pitch ball grid array
I/O	input/output
JEDEC	joint electron devices engineering council
JTAG	joint test action group
LSB	least significant bit
MSB	most significant bit
$\overline{OE}$	output enable
SRAM	static random access memory
TAP	test access port
TCK	test clock
TDI	test data-in
TDO	test data-out
TMS	test mode select
TTL	transistor-transistor logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

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**	3478707	01/17/2012	GOPA	New data sheet.
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