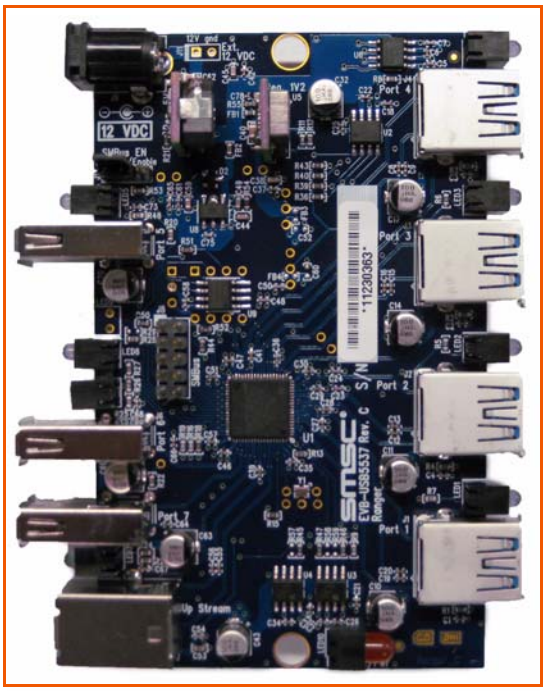
EVB-USB5537 Evaluation Board Revision C User Manual



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Chapter 1 Overview

EVB-USB5537 Revision C Evaluation Board is for the SMSC USB5537 Hi-Speed 7-port USB hub solution. The hub is fully compliant with the *USB 3.0 USB Specification* and supports SuperSpeed (SS), Hi-Speed (HS), Full-Speed (FS), and Low-Speed (LS) USB signalling for complete coverage of all defined USB operating speeds. Additionally, it provides an upstream port compliant to both the USB 2.0 and 3.0 specifications. All seven of the downstream ports are USB 2.0 compliant, while four of the downstream ports are also USB 3.0 compliant. All LED and port control signal pins are under firmware control in order to allow for maximum operational flexibility, and are available as GPIOs for customer-specific use. The EVB-USB5537 demonstrates driver compatibility with Microsoft Windows 7, WinXP, Mac OS X 10.4+ and Linux Hub Drivers.

1.1 Features

- Features the USB5537 in a 72-pin QFN RoHS compliant package
- USB 3.0 compliant (SS, HS, FS, and LS operation), USB pins are 5 V tolerant
- One USB 2.0/3.0 upstream hub port
- Self powered operation
- Seven downstream USB 2.0 ports, with four of the downstream ports supporting USB 3.0
- All downstream ports support individual port power
- Four downstream ports (1-4) support individual over current sense
- Optional onboard SPI Flash for external downloadable firmware
- Low-cost 4-layer space saving design
- Operates from one single voltage (+12.0 V, regulated) 'wall wart' external power supply
- Two GPIO LED indicators (LED0 and LED1)
- Single 25 MHz crystal or external clock input
- Single onboard +3.3 V, 1.5 Amp regulator
- Single onboard +1.2 V, 3 Amp regulator
- +3.3 V and port power LED indicators

1.2 General Description

The EVB-USB5537 is a demonstration and evaluation platform featuring the USB5537 Ultra Fast seven port hub on a 4-layer RoHS-compliant printed circuit board. It supports the legacy USB speeds (HS/FS/LS) through an included USB 2.0 hub controller which operates in parallel with the new SuperSpeed (SS) hub controller. This parallel hub operation keeps the SuperSpeed data transfers from being affected by the slower USB 2.0 traffic. The USB5537 is configured for operation through internal default settings and supports custom configurations through an optional external 8-Mbit SPI Flash device, U9.

Figure 1.1 shows the top and bottom level silk screen and copper layer.

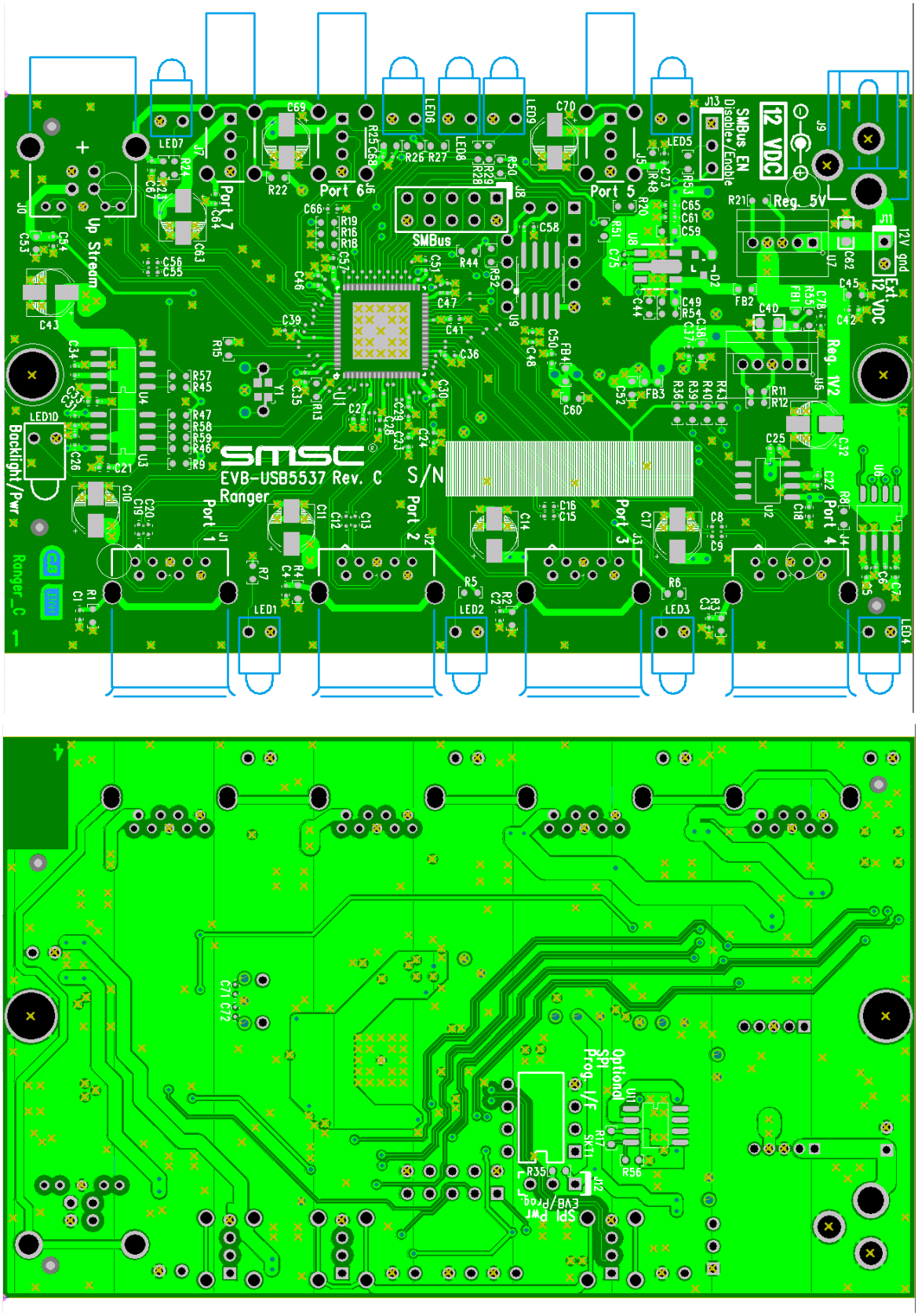

Figure 1.1 Top and Bottom Level Silk Screen and Copper Layers

Chapter 2 Getting Started

The EVB-USB5537 is configured by internal default registers. In this configuration it operates as a USB 3.0/USB 2.0 hub device with a seven port USB HUB and SMSC's standard VID/PID/DID settings.

2.1 Configuration

The SMSC EVB-USB5537 is designed for flexible configuration solutions. It can be configured with default internal register settings, through downloadable external firmware to an onboard SPI Flash, or through SMBus.

2.1.1 Configuration Source - Internal Default

When the USB5537 does not detect a valid SPI Flash image or SMBus configuration upon power-up, the EVB-USB5537 uses internal default register settings. It also sets the Vendor ID, Product ID, Language ID, and Device ID, and additional settings from internal ROM code.

2.1.2 Configuration Source - External SPI Flash and SMBus

Upon power-up the USB5537 first looks for an external SPI Flash device. If one is found, the external ROM is enabled and code execution is then initiated from the external SPI device. If a SPI Flash device is not found, the firmware checks to see whether SMBus is enabled. To enable SMBus, pins 2 and 3 must be shorted on the J13 *SMBus EN* header which pulls **SM_CLK** high. This header has pins 1 and 2 shorted by default which disables SMBus by pulling **SM_CLK** low. When SMBus is enabled, the firmware configures the GPIOs to act as an SMBus slave. As an SMBus slave, the firmware will wait indefinitely for the SMBus configuration. The SMBus can operate in either legacy mode (USB 2.0 only) or advanced mode (access to both USB 2.0 and USB 3.0 registers). SMBus data and clock can be controlled via the onboard SMBus header, J8. If the SMBus is not enabled, the USB5537 will then look to load the configuration from an external I^2C EEPROM. If no external options are detected, the USB5537 will operate from the internal OTP memory.

By default, the SPI Flash chip U9 is populated. The 10 kΩ pull-up resistors R50, R51, and R52 must also be populated. Finally, the 0 Ω resistor R35 must also be populated in order to supply +3.3V to the SPI chip. There is an alternative SPI programming interface available as well that is not populated by default. The SPI chip can be programmed via the 8-pin DIP socket SKT1. When using this programming socket, the *SPI Power* header J12 must now be populated and the 0 Ω resistor R35 must be removed: the SPI chip is now powered through the J12 power select header. The default is to have pins 1 and 2 shorted together which allows the onboard +3.3 V to power the SPI chip. However, if the SPI chip is being programmed via the SKT1 socket, then the chip should be powered by the programmer. Therefore, pins 2 and 3 should be shorted together on J12 which passes power from the SPI programmer to the SPI chip instead of using onboard power.

If the USB5537 does not detect an SMBus interface, it will then check for an I^2C EEPROM. For I^2C communciation, the SMBus header J8 can be used to access the **SCL** and **SDA** signals on the USB5537. In order to assure proper operation, the external 10 kΩ pull-up resistor R44 on **SM_DAT** must be populated and pins 2 and 3 on the *SMBus EN* header must be shorted so that **SM_CLK** has a 10 kΩ pull-up resistor (R53) on it.

2.1.3 Configuration Source - 25MHz Crystal

By default, a 2 mm x 1.6 mm Murata 25 MHz crystal, Y1, is populated on the evaluation board. External load capacitance is not required when this crystal is used. If a surface mount HCM49 crystal is used on the EVB instead, two 18 pF load capacitors C71 and C72 must be populated.

2.1.4 Power Source - Self-Powered

The EVB-USB5537 only supports self-powered operation, and is powered through one +12.0 V regulated 'wall wart' external power supply. The +12.0 V ‘wall wart’ plugs into the 2.5 mm connector J9 on the board. Alternatively, an external voltage can be injected onto the *J11 Ext.* 12 V header, which is not populated by default. The +12.0 V feeds a 6 A regulator which outputs +5.0 V across the board. This +5.0 V output controls the +3.3 V and +1.3 V onboard regulators.

2.1.5 Downstream Port Power Control

The USB 3.0 downstream port powers (ports 1 through 4) are controlled via two 1 A port power devices (AP2176S) and the USB 2.0 downstream port powers (ports 5 through 7) are controlled via two 500 mA port power devices (MIC2026). The MIC2026 devices, U3 and U4, are permanently enabled through a 10 kΩ pull-up resistor on the Enable input pins. The AP2176S devices, U2 and U6, are enabled via the **PRT_CTL[4:1]** pins. Downstream ports 1 through 4 have individual over current sensing available and all sensing signals are pulled high to +3.3 V through external 10 kΩ resistors. Downstream ports 5 through 7 have their over current sense signals mux’d with the port power control signals. In order to view over current sensing on the port power signals, the 0 Ω resistors R57, R58, and R59 must be populated. These resistors are not populated by default so that over current sensing is not possible on the **PRT_CTL[7:5]** pins. By default, **PRT_CTL5** is used as the **SM_DAT** pin and **PRT_CTL[7:6]** are floating pins.