FIR Filter Generator

Overview

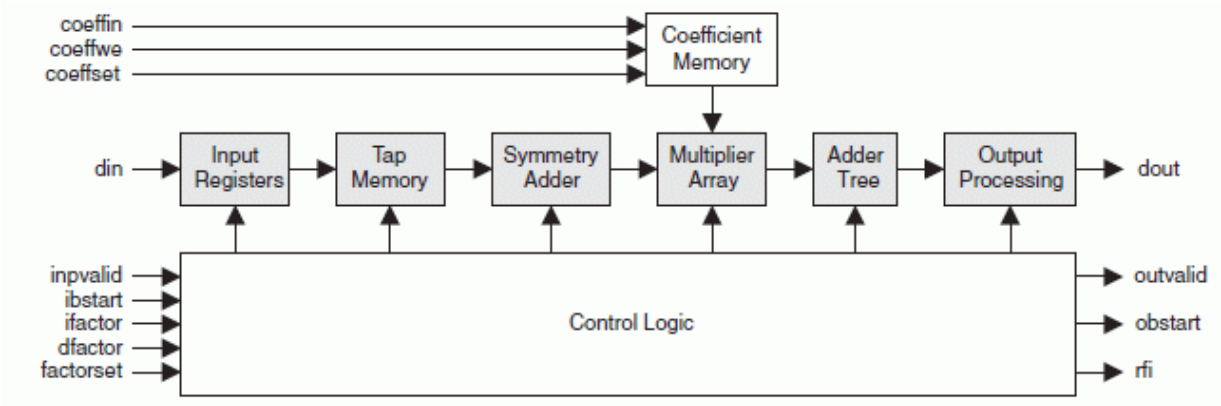
A **Finite Impulse Response (FIR) filter** performs a convolution of an input data sequence with the filter's impulse response (the discrete-time inverse Fourier transform of its desired frequency response), which is stored in memory. The equation for performing the convolution is given by

$$y_n = \sum_{i=0}^{N-1} x_{n-i} h_i$$

where y_n is the filter output at sample n, x_{n-i} is the value of the filter input i samples in the past, and h_i is the ith value of the filter impulse response.

The Lattice FIR (Finite Impulse Response) Filter IP core is a **widely configurable, multi-channel FIR filter, implemented using high performance sysDSP™ blocks** available in Lattice devices. In addition to **single rate filters**, the IP core also supports a range of **polyphase decimation** and **interpolation filters**. The utilization versus throughput trade-off can be controlled by specifying the number of multipliers used for implementing the filter. The FIR Filter IP core supports as high as 256 channels, with each having up to 2048 taps. The input data, coefficient and output data widths are configurable over a wide range. The IP core uses full internal precision while allowing variable output precision with several choices for saturation and rounding. The coefficients of the filter can be specified at generation time and/or re-loadable during run-time through input ports.

Functional Block Diagram of the FIR Filter IP Core



Features

- Variable number of taps up to 2048
- Input and coefficients widths of 4 to 32 bits
- Multi-channel support for up to 256 channels
- Decimation and Interpolation ratios from 2 to 256
- Support for half-band filter
- Configurable parallelism from fully parallel to serial
- Signed or unsigned data and coefficients
- Re-loadable coefficients support
- Full precision arithmetic
- Selectable output width and precision
- Selectable overflow: wrap-around or saturation
- Selectable rounding: truncation, round towards zero, round away from zero, round to nearest and convergent rounding
- Width and precision specified using fixed point notations

- Coefficients symmetry and negative symmetry optimization
- Handshake signals to facilitate smooth interfacing

Performance and Resource Utilization

LatticeECP3[1]

Mode	SLICEs	LUTs	Registers	18x18 Multipliers	sysMEM EBRs	fMAX (MHz)
4 channels, 64 taps, 1 multiplier	127	112	188	2	2	340
1 channel, 32 taps, 32 multipliers	454	805	636	32	-	298
1 channel, 32 taps, 8 multiplies	479	498	687	10	-	221

1. Performance and utilization data are generated targeting an LFE3-70E-8FN672CES device using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP3 family.

LatticeECP2M[1]

Mode	SLICEs	LUTs	Registers	18x18 Multipliers	sysMEM EBRs	fMAX (MHz)
4 channels, 64 taps, 1 multiplier	169	127	244	1	2	297
1 channel, 32 taps, 32 multipliers	417	268	806	32	-	283
1 channel, 32 taps, 8 multiplies	414	532	629	8	-	307

1. Performance and utilization data are generated targeting an LFE2M50E-7F672C device using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2M/S family.

LatticeECP2[1]

Mode	SLICEs	LUTs	Registers	18x18 Multipliers	sysMEM EBRs	fMAX (MHz)
4 channels, 64 taps, 1 multiplier	169	127	244	1	2	349
1 channel, 32 taps, 32 multipliers	417	268	806	32	-	235
1 channel, 32 taps, 8 multiplies	414	532	629	8	-	308

1. Performance and utilization data are generated targeting an LFE2-50E-7F672C device using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2/S family.

LatticeECP[1]

Mode	SLICEs	LUTs	Registers	18x18 Multipliers	sysMEM EBRs	fMAX (MHz)
4 channels, 64 taps, 1 multiplier	166	118	245	1	2	216
1 channel, 32 taps, 32 multipliers	415	264	806	32	-	180
1 channel, 32 taps, 8 multiplies	481	662	633	8	-	175

D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP family.

LatticeXP2[1]

Mode	SLICEs	LUTs	Registers	18x18 Multipliers	sysMEM EBRs	fMAX (MHz)
4 channels, 64 taps, 1 multiplier	169	127	244	1	2	303
1 channel, 32 taps, 32 multipliers	417	268	806	32	-	266
1 channel, 32 taps, 8 multiplies	414	532	629	8	-	292

1. Performance and utilization data are generated targeting an LFXP2-40E-7F672C device using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeXP2 family.

High Performance ECP3 DSP Based Filter Designs

Lattice has developed the following **Reference Designs** to highlight the **powerful DSP capability** of the LatticeECP3 FPGA.

Direct Form 64-Tap FIR Filter: In the direct form FIR filter, the input samples are shifted into a shift register queue and each shift register is connected to a multiplier. The products from the multipliers are added together to get the FIR filter's output sample. This example shows a 64-tap FIR filter using 16 sysDSP blocks and approximately 512 slices in the LatticeECP3 FPGA.

128-Tap Long Asymmetrical Filters Using Ladder Architecture: Using the ladder architecture, the FIR filter is split into sections each having the same coefficient set as if it was a single continuous filter chain. Instead of connecting the shifted data and the result outputs from the first section to the corresponding input of the next section, the ladder network connects a delayed version of the first stage input data to the second stage input data and sums a delayed version of the first stage sum output with the second stage sum output.

256-Tap Long Symmetrical Filters Using Ladder Architecture: The impulse response for most FIR filters is symmetric. This symmetry can generally be exploited to reduce the arithmetic requirements and produce area-efficient filter realizations. It is possible to use only half the multipliers for symmetric coefficients compared to that used for a similar filter with non-symmetric coefficients. An implementation for symmetric coefficients is shown in the figure below. The 256-tap long symmetrical filter example uses only 32 sysDSP slices, 2EBR and 3.5K slices.

Polyphase Interpolator FIR Filter Designs: The polyphase interpolation filter implements the computationally efficient 1-to-P interpolation filter where P is an integer greater than 1. The example below shows a design with an interpolation by 16 that uses 128 taps. This requires 8 polyphase filters (sub-filters) with 16 coefficients each.

Ordering Information

Family	Part Numbers
LatticeECP3	FIR-COMP-E3-U4
LatticeECP2M	FIR-COMP-PM-U4
LatticeECP2	FIR-COMP-P2-U4
LatticeECP	FIR-COMP-E2-U4
LatticeXP2	FIR-COMP-X2-U4

IP Express Version: 4.2
Evaluate: To download a full evaluation version of this IP, please go to the Lattice IP Server tab in the IPexpress Main Window. All LatticeCORE IP modules available for download are visible on this tab.
Purchase: To find out how to purchase the FIR Filter Generator IP Core, please contact your **local Lattice Sales Office**.