

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type(U-MOS-V)

SSM6P41FE

○ Power Management Switches

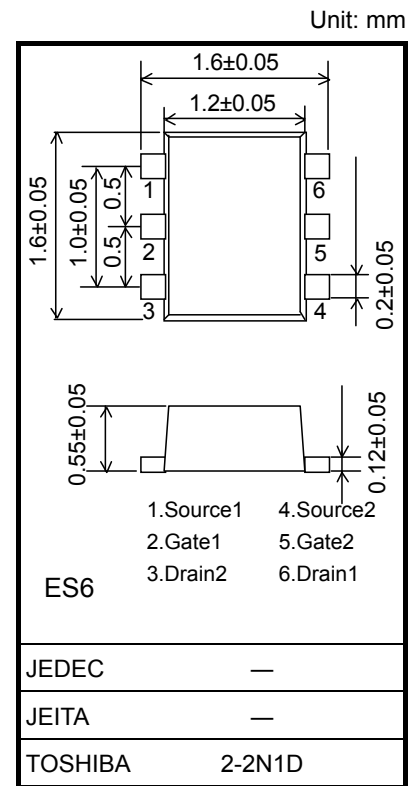
- 1.5-V drive
- Low on-resistance : $R_{DS(ON)} = 1.04 \Omega$ (max) (@ $V_{GS} = -1.5 V$)
 : $R_{DS(ON)} = 0.67 \Omega$ (max) (@ $V_{GS} = -1.8 V$)
 : $R_{DS(ON)} = 0.44 \Omega$ (max) (@ $V_{GS} = -2.5 V$)
 : $R_{DS(ON)} = 0.30 \Omega$ (max) (@ $V_{GS} = -4.5 V$)

Absolute Maximum Ratings (Ta = 25 °C) (Q1, Q2 Common)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	-20	V
Gate-source voltage	V_{GSS}	± 8	V
Drain current	DC	I_D	-720
	Pulse	I_{DP}	-1440
Power dissipation	P_D (Note1)	150	mW
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	-55 to 150	°C

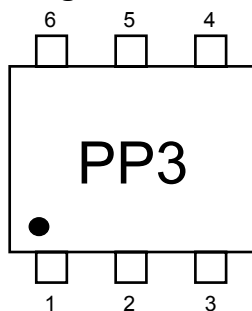
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
 Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Total rating
 Mounted on an FR4 board
 (25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.135 mm² × 6)

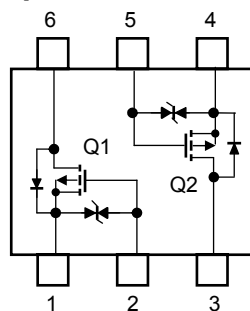


Weight: 3.0 mg (typ.)

Marking



Equivalent Circuit (top view)



Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Start of commercial production
 2009-04

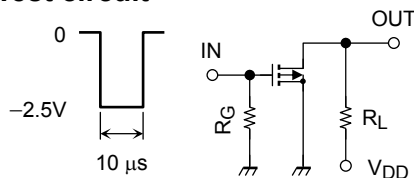
Electrical Characteristics (Ta = 25°C) (Q1, Q2 Common)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = -1 \text{ mA}, V_{GS} = 0 \text{ V}$	-20	—	—	V	
	$V_{(BR)DSX}$	$I_D = -1 \text{ mA}, V_{GS} = 8 \text{ V}$	-12	—	—		
Drain cutoff current	I_{DSS}	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	-10	μA	
Gate leakage current	I_{GSS}	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	± 1	μA	
Gate threshold voltage	V_{th}	$V_{DS} = -3 \text{ V}, I_D = -1 \text{ mA}$	-0.3	—	-1.0	V	
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = -3 \text{ V}, I_D = -400 \text{ mA}$ (Note2)	850	—	—	mS	
Drain-source on-resistance	$R_{DS(ON)}$	$I_D = -400 \text{ mA}, V_{GS} = -4.5 \text{ V}$ (Note2)	—	0.25	0.30	Ω	
		$I_D = -200 \text{ mA}, V_{GS} = -2.5 \text{ V}$ (Note2)	—	0.34	0.44		
		$I_D = -100 \text{ mA}, V_{GS} = -1.8 \text{ V}$ (Note2)	—	0.44	0.67		
		$I_D = -50 \text{ mA}, V_{GS} = -1.5 \text{ V}$ (Note2)	—	0.55	1.04		
Input capacitance	C_{iss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	110	—	pF	
Output capacitance	C_{oss}		—	28	—		
Reverse transfer capacitance	C_{rss}		—	20	—		
Total Gate Charge	Q_g	$V_{DD} = -10 \text{ V}, I_D = -720 \text{ mA}$ $V_{GS} = -4.5 \text{ V}$	—	1.76	—	nC	
Gate-Source Charge	Q_{gs}		—	1.22	—		
Gate-Drain Charge	Q_{gd}		—	0.54	—		
Switching time	Turn-on time	t_{on}	$V_{DD} = -10 \text{ V}, I_D = -100 \text{ mA}$ $V_{GS} = 0 \text{ to } -2.5 \text{ V}, R_G = 50 \Omega$	—	11	—	ns
	Turn-off time	t_{off}		—	38	—	
Drain-source forward voltage	V_{DSF}	$I_D = 720 \text{ mA}, V_{GS} = 0 \text{ V}$ (Note2)	—	0.85	1.2	V	

Note2: Pulse test

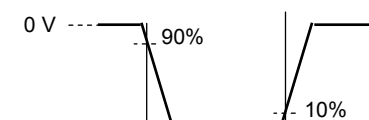
Switching Time Test Circuit

(a) Test circuit

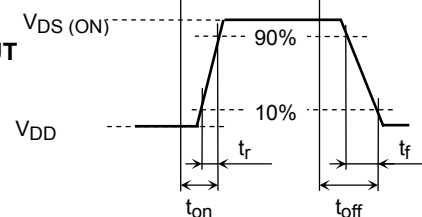


$V_{DD} = -10 \text{ V}$
 $R_G = 50 \Omega$
 Duty $\leq 1\%$
 $V_{IN}: t_r, t_f < 5 \text{ ns}$
 $(Z_{out} = 50 \Omega)$
 Common Source
 $T_a = 25^\circ\text{C}$

(b) V_{IN}



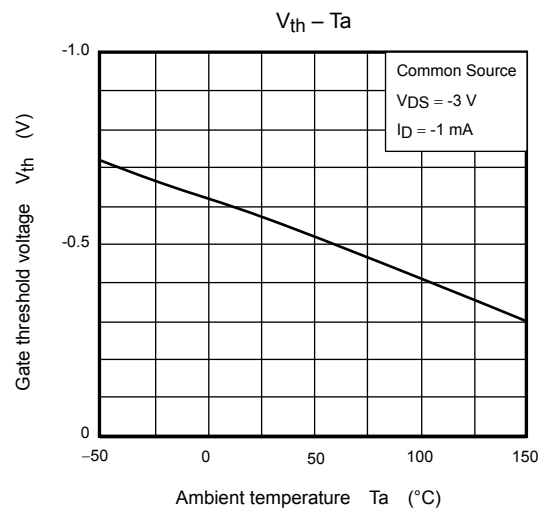
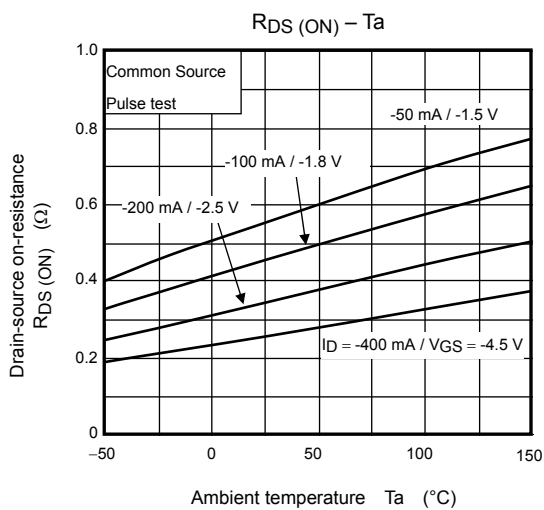
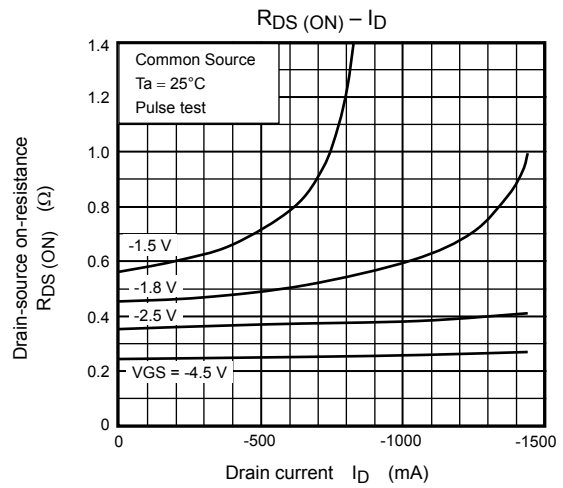
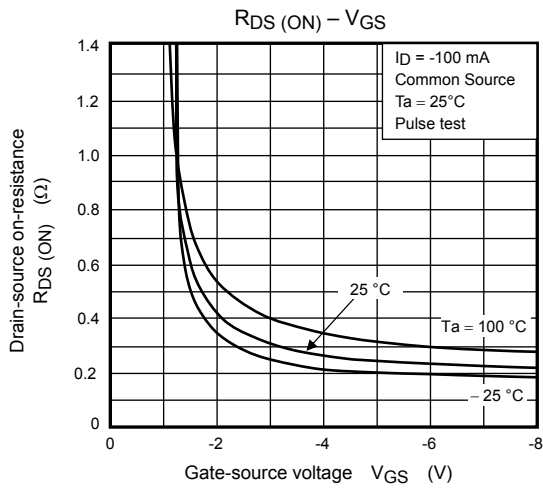
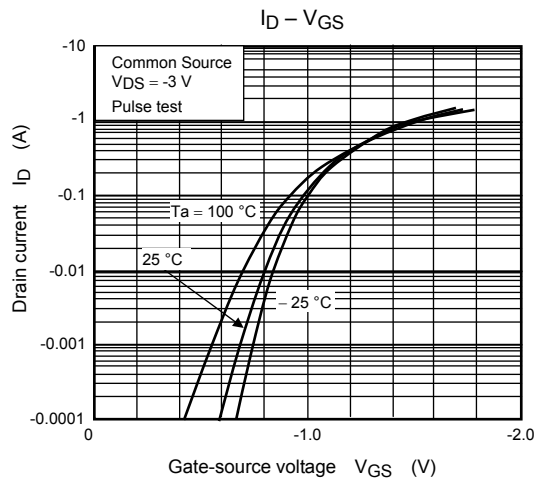
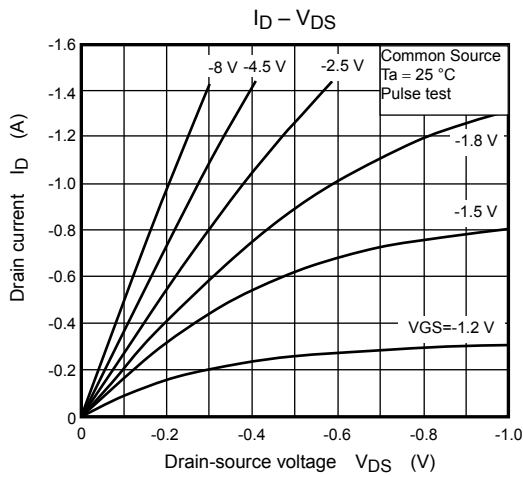
(c) V_{OUT}

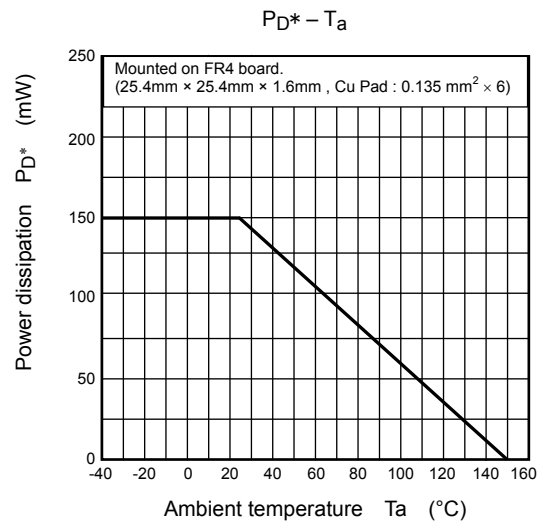
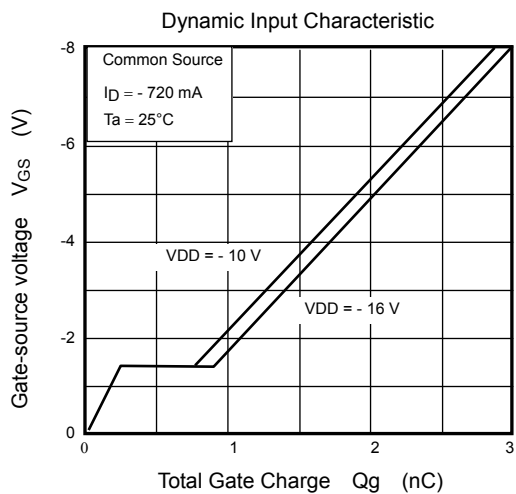
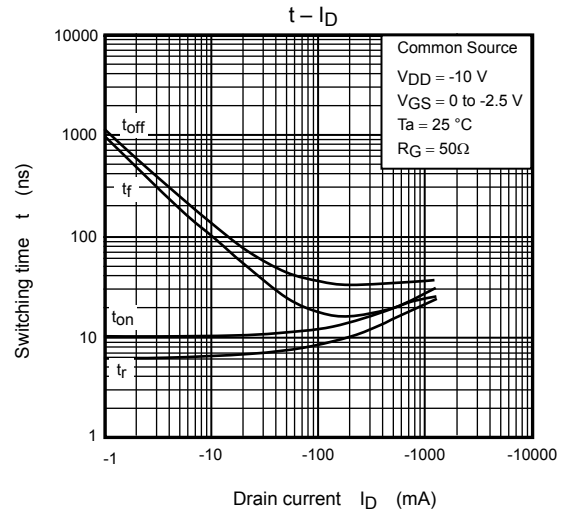
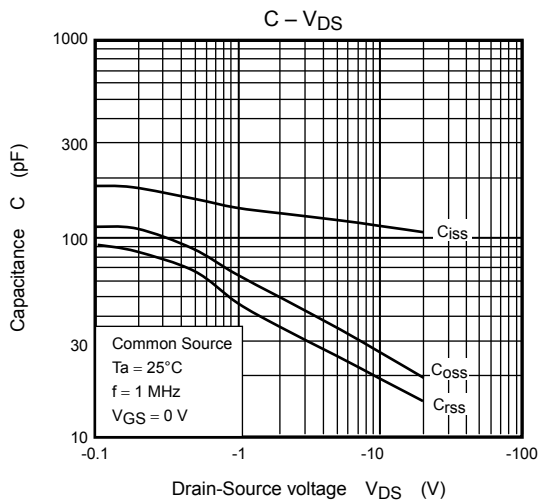
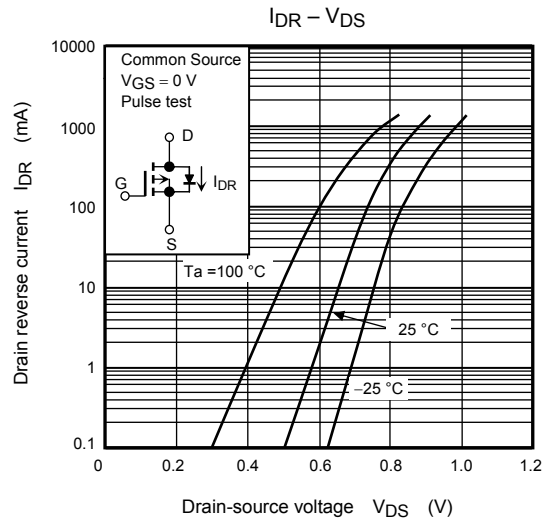
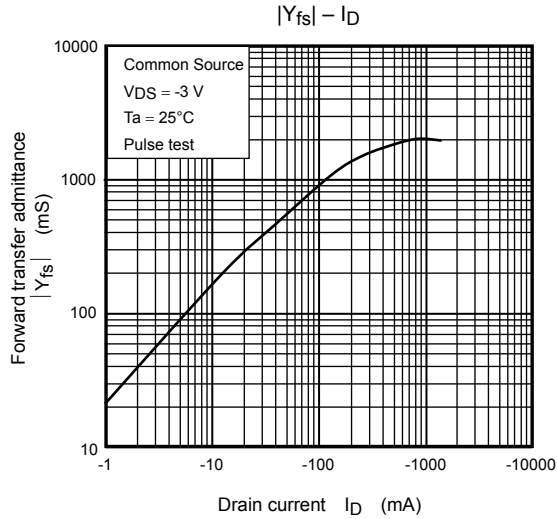


Precaution

Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be low (-1mA for the SSM6P41FE). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th} , and $V_{GS(off)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

Take this into consideration when using the device.





*:Total Rating

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