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Cypress (NASDAQ: CY) delivers high-performance, high-quality solutions at the heart of today's most advanced embedded systems, from automotive, industrial and networking platforms to highly interactive consumer and mobile devices. With a broad, differentiated product portfolio that includes NOR flash memories, F-RAM™ and SRAM, Traveo™ microcontrollers, the industry's only PSoC® programmable system-on-chip solutions, analog and PMIC Power Management ICs, CapSense® capacitive touch-sensing controllers, and Wireless BLE Bluetooth® Low-Energy and USB connectivity solutions, Cypress is committed to providing its customers worldwide with consistent innovation, best-in-class support and exceptional system value.

8-bit Microcontrollers

CMOS

New 8FX MB95310L/370L Series

MB95F314E/F314L/F316E/F316L/F318E/F318L
MB95F374E/F374L/F376E/F376L/F378E/F378L

■ DESCRIPTION

MB95310L/370L is a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of this series contain a variety of peripheral resources.

■ FEATURES

- F²MC-8FX CPU core

Instruction set optimized for controllers

- Multiplication and division instructions
- 16-bit arithmetic operations
- Bit test branch instructions
- Bit manipulation instructions, etc.

Note: F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

- Clock

- Selectable main clock source

Main OSC clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)

External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)

Main CR clock (1/8/10/12.5 MHz \pm 2%, maximum machine clock frequency: 12.5 MHz)

Main PLL clock (up to 16.25 MHz, maximum machine clock frequency: 16.25 MHz)

- Selectable subclock source

Sub-OSC clock (32.768 kHz)

External clock (32.768 kHz)

Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 200 kHz)

- Timer

- 8/16-bit composite timer
- 8/16-bit PPG
- 16-bit reload timer
- Event counter
- Time-base timer
- Watch prescaler

- UART-SIO

- Capable of clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer
- Full duplex double buffer

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For the information for microcontroller supports, see the following website.

<http://edevic.fujitsu.com/micom/en-support/>

MB95310L/370L Series

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- I²C
 - Built-in wake-up function
- External interrupt
 - Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
 - Can be used to wake up the device from different low power consumption (standby) modes
- 8/10-bit A/D converter
 - 8-bit or 10-bit resolution can be selected
- LCD controller (LCDC)
 - 40 SEG × 4 COM (MB95F314E/F314L/F316E/F316L/F318E/F318L)
 - 32 SEG × 4 COM (MB95F374E/F374L/F376E/F376L/F378E/F378L)
 - Internal divider resistor
 - With blinking function
- Low power consumption (standby) modes
 - Stop mode
 - Sleep mode
 - Watch mode
 - Time-base timer mode
- I/O port
 - MB95F314E/F314L/F316E/F316L/F318E/F318L (maximum no. of I/O ports: 71)
 - General-purpose I/O ports (N-ch open drain) : 3
 - General-purpose I/O ports (CMOS I/O) : 68
 - MB95F374E/F374L/F376E/F376L/F378E/F378L (maximum no. of I/O ports: 55)
 - General-purpose I/O ports (N-ch open drain) : 3
 - General-purpose I/O ports (CMOS I/O) : 52
- On-chip debug
 - 1-wire serial control
 - Serial writing supported (asynchronous mode)
- Hardware/software watchdog timer
 - Built-in hardware watchdog timer
 - Built-in software watchdog timer
- Low-voltage detection reset circuit
 - Built-in low-voltage detector
 - Three configurable low-voltage detection levels for generating reset
 - Five configurable low-voltage detection levels for generating interrupts
- Clock supervisor counter
 - Built-in clock supervisor counter function
- Programmable port input voltage level
 - CMOS input level / hysteresis input level
- Dual operation Flash memory
 - The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.
- Flash memory security function
 - Protects the content of the Flash memory

MB95310L/370L Series

■ PRODUCT LINE-UP

• MB95310L Series

| Part number | MB95F314E | MB95F316E | MB95F318E | MB95F314L | MB95F316L | MB95F318L |
|----------------------------------|--|------------|------------|-----------|------------|------------|
| Parameter | | | | | | |
| Type | Flash memory product | | | | | |
| Clock supervisor counter | It supervises the main clock oscillation. | | | | | |
| Flash memory capacity | 20 Kbyte | 36 Kbyte | 60 Kbyte | 20 Kbyte | 36 Kbyte | 60 Kbyte |
| RAM capacity | 496 bytes | 1008 bytes | 2032 bytes | 496 bytes | 1008 bytes | 2032 bytes |
| Low-voltage detection reset | Yes | | | No | | |
| Reset input | Dedicated | | | | | |
| CPU functions | <ul style="list-style-type: none"> • Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 μs (machine clock frequency = 16.25 MHz) | | | | | |
| General-purpose I/O | <ul style="list-style-type: none"> • I/O ports (Max) : 71 • CMOS I/O : 68 • N-ch open drain: 3 | | | | | |
| Time-base timer | Interval time: 0.256 ms - 8.3 s (external clock frequency = 4 MHz) | | | | | |
| Hardware/software watchdog timer | <ul style="list-style-type: none"> • Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-CR clock can be used as the source clock of the hardware watchdog timer. | | | | | |
| Wild register | It can be used to replace three bytes of data. | | | | | |
| I ² C | 1 channel | | | | | |
| | <ul style="list-style-type: none"> • Master/Slave sending and receiving • Bus error function and arbitration function • Detecting transmitting direction function • Start condition repeated generation and detection functions • Built-in wake-up function | | | | | |
| UART/SIO | 2 channels | | | | | |
| | <ul style="list-style-type: none"> • Data transfer with UART/SIO is enabled. • It has a full duplex double buffer, variable data length (5/6/7/8 bits), a built-in baud rate generator and an error detection function. • It uses the NRZ type transfer format. • LSB-first data transfer and MSB-first data transfer are available to use. • Clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer is enabled. | | | | | |
| 8/10-bit A/D converter | 4 channels | | | | | |
| | 8-bit or 10-bit resolution can be selected. | | | | | |

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MB95310L/370L Series

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| Part number | MB95F314E | MB95F316E | MB95F318E | MB95F314L | MB95F316L | MB95F318L |
|--------------------------|--|-----------|-----------|-----------|-----------|-----------|
| Parameter | | | | | | |
| 8/16-bit composite timer | 2 channels <ul style="list-style-type: none"> Each timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". It has built-in timer function, PWC function, PWM function and input capture function. Count clock: it can be selected from internal clocks (seven types) and external clocks. It can output square wave. | | | | | |
| LCD controller (LCDC) | <ul style="list-style-type: none"> COM output: 4 (Max) SEG output: 40 (Max) LCD drive power supply (bias) pin: 4 (Max) 40 SEG × 4 COM: 160 pixels can be displayed Duty LCD mode Operate in LCD standby mode Blinking function Internal divider resistor for LCD drive | | | | | |
| 16-bit reload timer | 1 channel <ul style="list-style-type: none"> Two clock modes and two counter operating modes can be selected Square waveform output Count clock: it can be selected from internal clocks (seven types) and external clocks. Counter operating mode: reload mode or one-shot mode can be selected | | | | | |
| Event counter | By configuring the 16-bit reload timer and the 8/16-bit composite timer ch. 1, event counter function can be implemented. When the event counter function is used, the 16-bit reload timer and the 8/16-bit composite timer ch. 1 are unavailable. | | | | | |
| 8/16-bit PPG | 2 channels <ul style="list-style-type: none"> Each channel of the PPG can be used as "8-bit PPG × 2 channels" or "16-bit PPG × 1 channel" Counter operating clock: Eight selectable clock sources | | | | | |
| Watch counter | <ul style="list-style-type: none"> Count clock: Four selectable clock sources (125 ms, 250 ms, 500 ms or 1 s) Counter value can be set from 0 to 63. (Capable of counting for 1 minute when selecting clock source of 1 second and setting counter value to 60) | | | | | |
| External interrupt | 8 channels <ul style="list-style-type: none"> Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) It can be used to wake up the device from the standby mode. | | | | | |
| On-chip debug | <ul style="list-style-type: none"> 1-wire serial control It supports serial writing. (asynchronous mode) | | | | | |
| Watch prescaler | Eight different time intervals can be selected. (62.5 ms, 125 ms, 250 ms, 500 ms, 1 s, 2 s, 4 s, 8 s) | | | | | |
| Flash memory | <ul style="list-style-type: none"> It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. It has a flag indicating the completion of the operation of Embedded Algorithm. Number of program/erase cycles: 100000 Data retention time: 20 years Flash security feature for protecting the content of the Flash memory | | | | | |
| Standby mode | Sleep mode, stop mode, watch mode, time-base timer mode | | | | | |
| Package | FPT-80P-M37 | | | | | |

MB95310L/370L Series

• MB95370L Series

| Part number | MB95F374E | MB95F376E | MB95F378E | MB95F374L | MB95F376L | MB95F378L |
|----------------------------------|--|------------|------------|-----------|------------|------------|
| Parameter | | | | | | |
| Type | Flash memory product | | | | | |
| Clock supervisor counter | It supervises the main clock oscillation. | | | | | |
| Flash memory capacity | 20 Kbyte | 36 Kbyte | 60 Kbyte | 20 Kbyte | 36 Kbyte | 60 Kbyte |
| RAM capacity | 496 bytes | 1008 bytes | 2032 bytes | 496 bytes | 1008 bytes | 2032 bytes |
| Low-voltage detection reset | Yes | | | No | | |
| Reset input | Dedicated | | | | | |
| CPU functions | <ul style="list-style-type: none"> • Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 μs (machine clock frequency = 16.25 MHz) | | | | | |
| General-purpose I/O | <ul style="list-style-type: none"> • I/O ports (Max): 55 • CMOS I/O: 52 • N-ch open drain: 3 | | | | | |
| Time-base timer | Interval time: 0.256 ms - 8.3 s (external clock frequency = 4 MHz) | | | | | |
| Hardware/software watchdog timer | <ul style="list-style-type: none"> • Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-CR clock can be used as the source clock of the hardware watchdog timer. | | | | | |
| Wild register | It can be used to replace three bytes of data. | | | | | |
| I ² C | 1 channel | | | | | |
| | <ul style="list-style-type: none"> • Master/Slave sending and receiving • Bus error function and arbitration function • Detecting transmitting direction function • Start condition repeated generation and detection functions • Built-in wake-up function | | | | | |
| UART/SIO | 2 channels | | | | | |
| | <ul style="list-style-type: none"> • Data transfer with UART/SIO is enabled. • It has a full duplex double buffer, variable data length (5/6/7/8 bits), a built-in baud rate generator and an error detection function. • It uses the NRZ type transfer format. • LSB-first data transfer and MSB-first data transfer are available to use. • Clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer is enabled. | | | | | |
| 8/10-bit A/D converter | 4 channels | | | | | |
| | 8-bit or 10-bit resolution can be selected. | | | | | |
| 8/16-bit composite timer | 2 channels | | | | | |
| | <ul style="list-style-type: none"> • Each timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has built-in timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave. | | | | | |

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MB95310L/370L Series

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| Part number | MB95F374E | MB95F376E | MB95F378E | MB95F374L | MB95F376L | MB95F378L |
|-----------------------|--|-----------|-----------|-----------|-----------|-----------|
| Parameter | | | | | | |
| LCD controller (LCDC) | <ul style="list-style-type: none"> • COM output: 4 (Max) • SEG output: 32 (Max) • LCD drive power supply (bias) pin: 3 (Max) • 32 SEG × 4 COM: 128 pixels can be displayed | | | | | |
| | <ul style="list-style-type: none"> • Duty LCD mode • Operate in LCD standby mode • Blinking function • Internal divider resistor for LCD drive | | | | | |
| 16-bit reload timer | 1 channel | | | | | |
| | <ul style="list-style-type: none"> • Two clock modes and two counter operating modes can be selected • Square waveform output • Count clock: it can be selected from internal clocks (seven types) and external clocks. • Counter operating mode: reload mode or one-shot mode can be selected | | | | | |
| Event counter | By configuring the 16-bit reload timer and the 8/16-bit composite timer ch. 1, event counter function can be implemented. When the event counter function is used, the 16-bit reload timer and the 8/16-bit composite timer ch. 1 are unavailable. | | | | | |
| 8/16-bit PPG | 2 channels | | | | | |
| | <ul style="list-style-type: none"> • Each channel of the PPG can be used as “8-bit PPG × 2 channels” or “16-bit PPG × 1 channel” • Counter operating clock: Eight selectable clock sources | | | | | |
| Watch counter | <ul style="list-style-type: none"> • Count clock: Four selectable clock sources (125 ms, 250 ms, 500 ms or 1 s) • Counter value can be set from 0 to 63. (Capable of counting for 1 minute when selecting clock source of 1 second and setting counter value to 60) | | | | | |
| External interrupt | 8 channels | | | | | |
| | <ul style="list-style-type: none"> • Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from the standby mode. | | | | | |
| On-chip debug | <ul style="list-style-type: none"> • 1-wire serial control • It supports serial writing. (asynchronous mode) | | | | | |
| Watch prescaler | Eight different time intervals can be selected. (62.5 ms, 125 ms, 250 ms, 500 ms, 1 s, 2 s, 4 s, 8 s) | | | | | |
| Flash memory | <ul style="list-style-type: none"> • It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of program/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory | | | | | |
| Standby mode | Sleep mode, stop mode, watch mode, time-base timer mode | | | | | |
| Package | FPT-64P-M38 FPT-64P-M39 | | | | | |

MB95310L/370L Series

■ OSCILLATION STABILIZATION WAIT TIME

The main CR clock oscillation stabilization wait time is fixed to the maximum value. Below is the maximum value.

| Oscillation stabilization wait time | Remarks |
|-------------------------------------|---|
| $(2^{10} - 2) / F_{CRH}$ | Approx. 128 μ s (when the main CR clock is 8 MHz) |

The main PLL clock oscillation stabilization wait time is fixed to the maximum value. Below is the maximum value.

| Oscillation stabilization wait time | Remarks |
|-------------------------------------|--|
| $(2^{14} - 2) / F_{CH}$ | Approx. 14.1 ms (when the main PLL clock is 4 MHz) |

■ PACKAGES AND CORRESPONDING PRODUCTS

| Part number | MB95F314E | MB95F316E | MB95F318E | MB95F314L | MB95F316L | MB95F318L |
|----------------|-----------|-----------|-----------|-----------|-----------|-----------|
| Package | | | | | | |
| FPT-80P-M37 | | | | O | | |
| FPT-64P-M38 | | | | X | | |
| FPT-64P-M39 | | | | X | | |

| Part number | MB95F374E | MB95F376E | MB95F378E | MB95F374L | MB95F376L | MB95F378L |
|----------------|-----------|-----------|-----------|-----------|-----------|-----------|
| Package | | | | | | |
| FPT-80P-M37 | | | | X | | |
| FPT-64P-M38 | | | | O | | |
| FPT-64P-M39 | | | | O | | |

O: Available

X: Unavailable

■ DIFFERENCES AMONG PRODUCTS AND NOTES ON PRODUCT SELECTION

- Current consumption

When using the on-chip debug function, take account of the current consumption of flash erase/write.

For details of current consumption, see “■ ELECTRICAL CHARACTERISTICS”.

- Package

For details of information on each package, see “■ PACKAGES AND CORRESPONDING PRODUCTS” and “■ PACKAGE DIMENSION”.

- Operating voltage

The operating voltage varies, depending on whether the on-chip debug function is used or not.

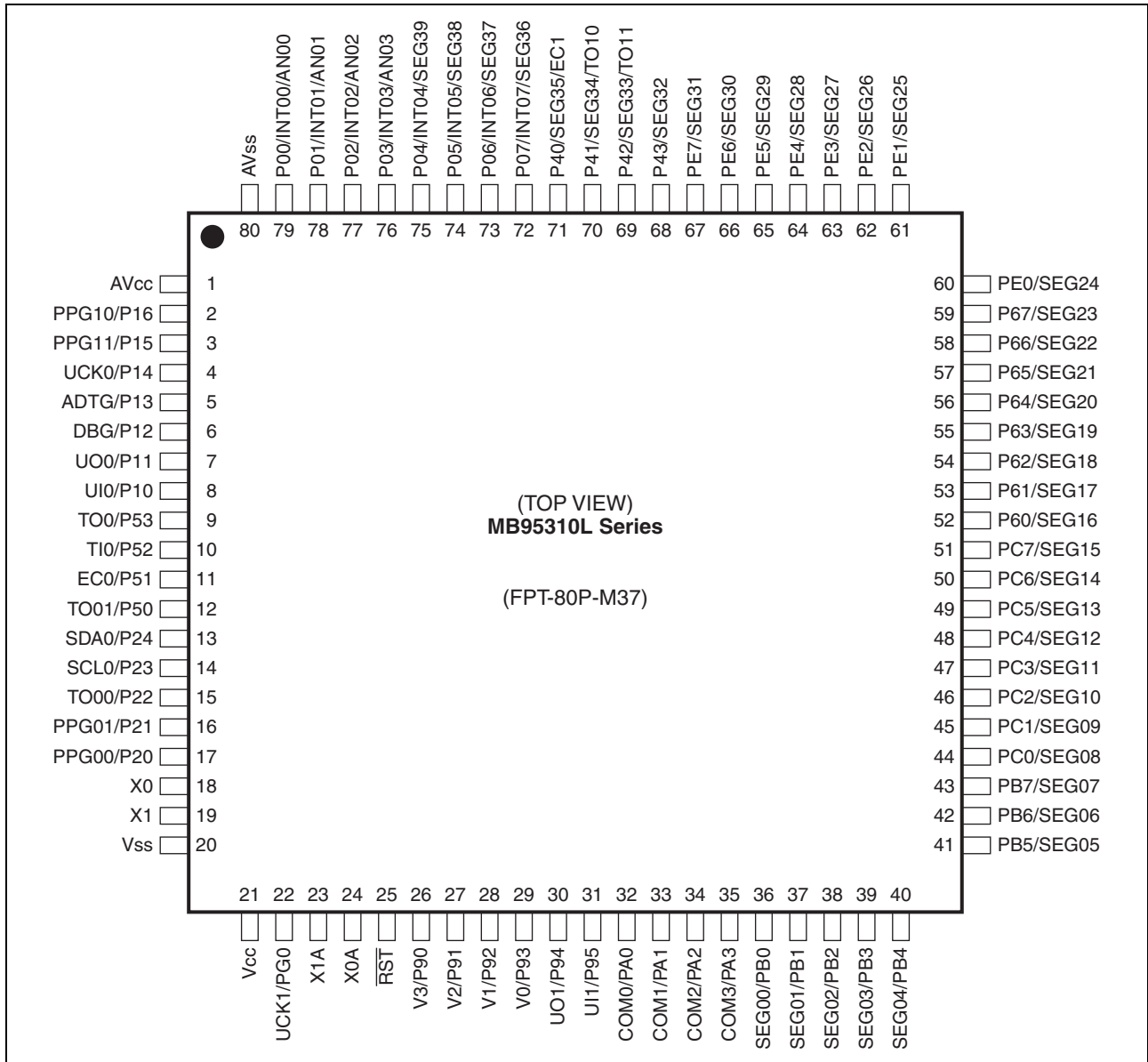
For details of the operating voltage, see “■ ELECTRICAL CHARACTERISTICS”.

- On-chip debug function

The on-chip debug function requires that V_{CC} , V_{SS} and 1 serial-wire be connected to an evaluation tool. For details of the connection method, refer to “CHAPTER 31 EXAMPLE OF SERIAL PROGRAMMING CONNECTION” in the hardware manual of the MB95310L/370L Series.

MB95310L/370L Series

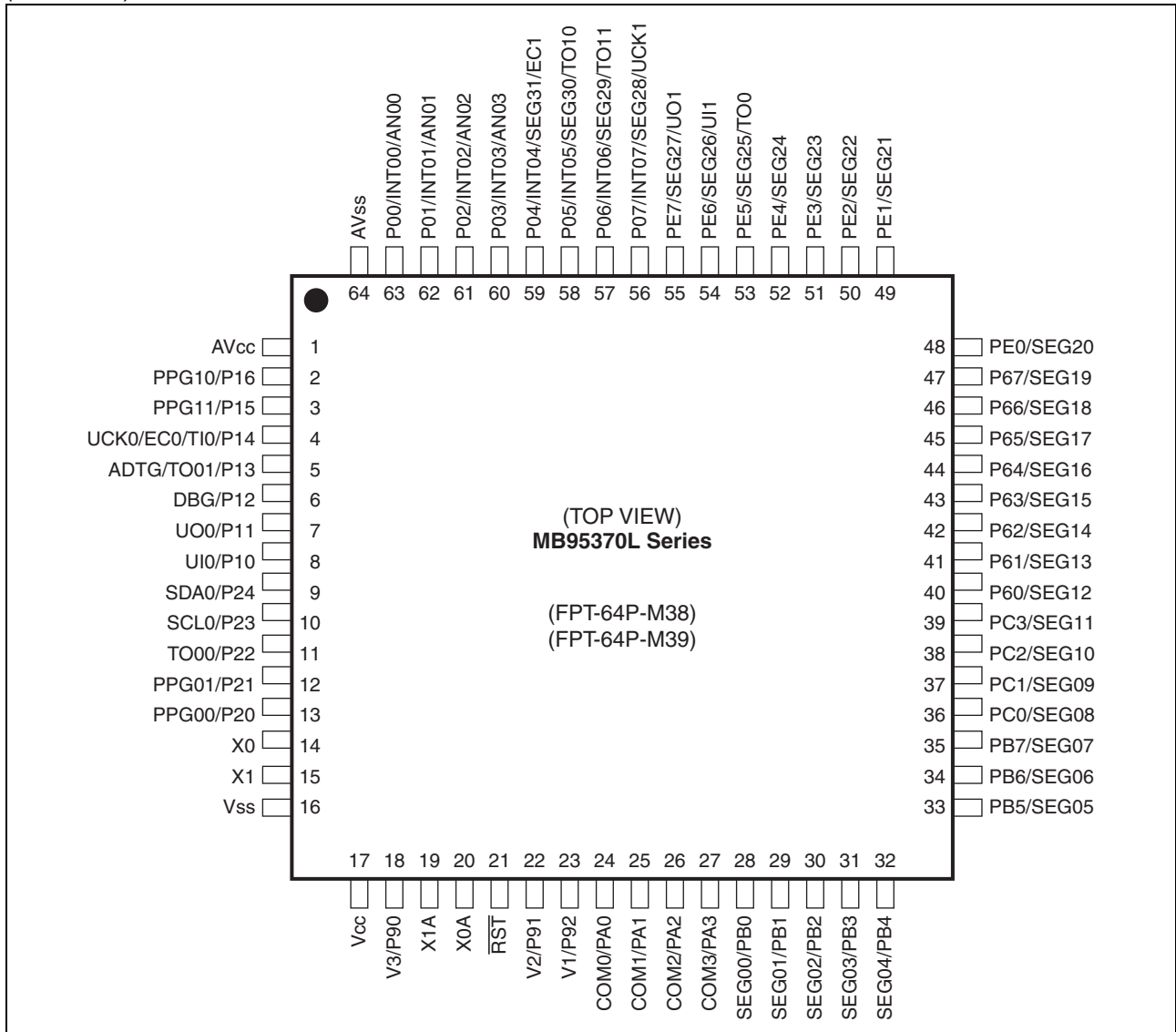
PIN ASSIGNMENT



(Continued)

MB95310L/370L Series

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MB95310L/370L Series

■ PIN DESCRIPTION (MB95310L Series)

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|------------------|-------------------|---|
| 1 | AV _{cc} | — | A/D converter power supply pin |
| 2 | P16 | H | General-purpose I/O port |
| | PPG10 | | 8/16-bit PPG ch. 1 output pin |
| 3 | P15 | H | General-purpose I/O port |
| | PPG11 | | 8/16-bit PPG ch. 1 output pin |
| 4 | P14 | H | General-purpose I/O port |
| | UCK0 | | UART/SIO ch. 0 clock I/O pin |
| 5 | P13 | H | General-purpose I/O port |
| | ADTG | | A/D trigger input (ADTG) pin |
| 6 | P12 | C | General-purpose I/O port |
| | DBG | | DBG input pin |
| 7 | P11 | H | General-purpose I/O port |
| | UO0 | | UART/SIO ch. 0 data output pin |
| 8 | P10 | G | General-purpose I/O port |
| | UI0 | | UART/SIO ch. 0 data input pin |
| 9 | P53 | H | General-purpose I/O port |
| | TO0 | | 16-bit reload timer ch. 0 output pin |
| 10 | P52 | H | General-purpose I/O port |
| | TI0 | | 16-bit reload timer ch. 0 input pin The pin can also be used as the event counter input pin when the event counter function is used. |
| 11 | P51 | H | General-purpose I/O port |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| 12 | P50 | H | General-purpose I/O port |
| | TO01 | | 8/16-bit composite timer ch. 0 output pin |
| 13 | P24 | I | General-purpose I/O port |
| | SDA0 | | I ² C data I/O pin |
| 14 | P23 | I | General-purpose I/O port |
| | SCL0 | | I ² C clock I/O pin |
| 15 | P22 | H | General-purpose I/O port |
| | TO00 | | 8/16-bit composite timer ch. 0 output pin |
| 16 | P21 | H | General-purpose I/O port |
| | PPG01 | | 8/16-bit PPG ch. 0 output pin |
| 17 | P20 | H | General-purpose I/O port |
| | PPG00 | | 8/16-bit PPG ch. 0 output pin |
| 18 | X0 | A | Main clock oscillation pin |
| 19 | X1 | A | Main clock oscillation pin |

(Continued)

MB95310L/370L Series

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|-------------------------|-------------------|-----------------------------------|
| 20 | V _{ss} | — | Power supply pin (GND) |
| 21 | V _{cc} | — | Power supply pin |
| 22 | PG0 | H | General-purpose I/O port |
| | UCK1 | | UART/SIO ch. 1 clock I/O pin |
| 23 | X1A | A | Subclock oscillation pin (32 kHz) |
| 24 | X0A | A | Subclock oscillation pin (32 kHz) |
| 25 | $\overline{\text{RST}}$ | B | Reset pin |
| 26 | P90 | R | General-purpose I/O port |
| | V3 | | LCDC drive power supply pin |
| 27 | P91 | R | General-purpose I/O port |
| | V2 | | LCDC drive power supply pin |
| 28 | P92 | R | General-purpose I/O port |
| | V1 | | LCDC drive power supply pin |
| 29 | P93 | R | General-purpose I/O port |
| | V0 | | LCDC drive power supply pin |
| 30 | P94 | H | General-purpose I/O port |
| | UO1 | | UART/SIO ch. 0 data output pin |
| 31 | P95 | G | General-purpose I/O port |
| | UI1 | | UART/SIO ch. 0 data input pin |
| 32 | PA0 | M | General-purpose I/O port |
| | COM0 | | LCDC COM output pin |
| 33 | PA1 | M | General-purpose I/O port |
| | COM1 | | LCDC COM output pin |
| 34 | PA2 | M | General-purpose I/O port |
| | COM2 | | LCDC COM output pin |
| 35 | PA3 | M | General-purpose I/O port |
| | COM3 | | LCDC COM output pin |
| 36 | PB0 | M | General-purpose I/O port |
| | SEG00 | | LCDC SEG output pin |
| 37 | PB1 | M | General-purpose I/O port |
| | SEG01 | | LCDC SEG output pin |
| 38 | PB2 | M | General-purpose I/O port |
| | SEG02 | | LCDC SEG output pin |
| 39 | PB3 | M | General-purpose I/O port |
| | SEG03 | | LCDC SEG output pin |
| 40 | PB4 | M | General-purpose I/O port |
| | SEG04 | | LCDC SEG output pin |

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MB95310L/370L Series

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|----------|-------------------|--------------------------|
| 41 | PB5 | M | General-purpose I/O port |
| | SEG05 | | LCDC SEG output pin |
| 42 | PB6 | M | General-purpose I/O port |
| | SEG06 | | LCDC SEG output pin |
| 43 | PB7 | M | General-purpose I/O port |
| | SEG07 | | LCDC SEG output pin |
| 44 | PC0 | M | General-purpose I/O port |
| | SEG08 | | LCDC SEG output pin |
| 45 | PC1 | M | General-purpose I/O port |
| | SEG09 | | LCDC SEG output pin |
| 46 | PC2 | M | General-purpose I/O port |
| | SEG10 | | LCDC SEG output pin |
| 47 | PC3 | M | General-purpose I/O port |
| | SEG11 | | LCDC SEG output pin |
| 48 | PC4 | M | General-purpose I/O port |
| | SEG12 | | LCDC SEG output pin |
| 49 | PC5 | M | General-purpose I/O port |
| | SEG13 | | LCDC SEG output pin |
| 50 | PC6 | M | General-purpose I/O port |
| | SEG14 | | LCDC SEG output pin |
| 51 | PC7 | M | General-purpose I/O port |
| | SEG15 | | LCDC SEG output pin |
| 52 | P60 | M | General-purpose I/O port |
| | SEG16 | | LCDC SEG output pin |
| 53 | P61 | M | General-purpose I/O port |
| | SEG17 | | LCDC SEG output pin |
| 54 | P62 | M | General-purpose I/O port |
| | SEG18 | | LCDC SEG output pin |
| 55 | P63 | M | General-purpose I/O port |
| | SEG19 | | LCDC SEG output pin |
| 56 | P64 | M | General-purpose I/O port |
| | SEG20 | | LCDC SEG output pin |
| 57 | P65 | M | General-purpose I/O port |
| | SEG21 | | LCDC SEG output pin |
| 58 | P66 | M | General-purpose I/O port |
| | SEG22 | | LCDC SEG output pin |

(Continued)

MB95310L/370L Series

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|----------|-------------------|--|
| 59 | P67 | M | General-purpose I/O port |
| | SEG23 | | LCDC SEG output pin |
| 60 | PE0 | M | General-purpose I/O port |
| | SEG24 | | LCDC SEG output pin |
| 61 | PE1 | M | General-purpose I/O port |
| | SEG25 | | LCDC SEG output pin |
| 62 | PE2 | M | General-purpose I/O port |
| | SEG26 | | LCDC SEG output pin |
| 63 | PE3 | M | General-purpose I/O port |
| | SEG27 | | LCDC SEG output pin |
| 64 | PE4 | M | General-purpose I/O port |
| | SEG28 | | LCDC SEG output pin |
| 65 | PE5 | M | General-purpose I/O port |
| | SEG29 | | LCDC SEG output pin |
| 66 | PE6 | N | General-purpose I/O port |
| | SEG30 | | LCDC SEG output pin |
| 67 | PE7 | M | General-purpose I/O port |
| | SEG31 | | LCDC SEG output pin |
| 68 | P43 | M | General-purpose I/O port |
| | SEG32 | | LCDC SEG output pin |
| 69 | P42 | M | General-purpose I/O port |
| | SEG33 | | LCDC SEG output pin |
| | TO11 | | 8/16-bit composite timer ch. 1 output pin |
| 70 | P41 | M | General-purpose I/O port |
| | SEG34 | | LCDC SEG output pin |
| | TO10 | | 8/16-bit composite timer ch. 1 output pin |
| 71 | P40 | M | General-purpose I/O port |
| | SEG35 | | LCDC SEG output pin |
| | EC1 | | 8/16-bit composite timer ch. 1 clock input pin |
| 72 | P07 | Q | General-purpose I/O port |
| | INT07 | | External interrupt input pin |
| | SEG36 | | LCDC SEG output pin |
| 73 | P06 | Q | General-purpose I/O port |
| | INT06 | | External interrupt input pin |
| | SEG37 | | LCDC SEG output pin |

(Continued)

MB95310L/370L Series

(Continued)

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|------------------|-------------------|--------------------------------------|
| 74 | P05 | Q | General-purpose I/O port |
| | INT05 | | External interrupt input pin |
| | SEG38 | | LCDC SEG output pin |
| 75 | P04 | Q | General-purpose I/O port |
| | INT04 | | External interrupt input pin |
| | SEG39 | | LCDC SEG output pin |
| 76 | P03 | J | General-purpose I/O port |
| | INT03 | | External interrupt input pin |
| | AN03 | | A/D analog input pin |
| 77 | P02 | J | General-purpose I/O port |
| | INT02 | | External interrupt input pin |
| | AN02 | | A/D analog input pin |
| 78 | P01 | J | General-purpose I/O port |
| | INT01 | | External interrupt input pin |
| | AN01 | | A/D analog input pin |
| 79 | P00 | J | General-purpose I/O port |
| | INT00 | | External interrupt input pin |
| | AN00 | | A/D analog input pin |
| 80 | AV _{ss} | — | A/D converter power supply pin (GND) |

*: For the I/O circuit types, see “■ I/O CIRCUIT TYPE”.

MB95310L/370L Series

■ PIN DESCRIPTION (MB95370L Series)

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|------------------|-------------------|--|
| 1 | AV _{cc} | — | A/D converter power supply pin |
| 2 | P16 | H | General-purpose I/O port |
| | PPG10 | | 8/16-bit PPG ch. 1 output pin |
| 3 | P15 | H | General-purpose I/O port |
| | PPG11 | | 8/16-bit PPG ch. 1 output pin |
| 4 | P14 | H | General-purpose I/O port |
| | UCK0 | | UART/SIO ch. 0 clock I/O pin |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin The pin can also be used as the event counter input pin when the event counter function is used. |
| | TI0 | | 16-bit reload timer ch. 0 input pin |
| 5 | P13 | H | General-purpose I/O port |
| | ADTG | | A/D trigger input (ADTG) pin |
| | TO01 | | 8/16-bit composite timer ch. 0 output pin |
| 6 | P12 | C | General-purpose I/O port |
| | DBG | | DBG input pin |
| 7 | P11 | H | General-purpose I/O port |
| | UO0 | | UART/SIO ch. 0 data output pin |
| 8 | P10 | G | General-purpose I/O port |
| | UI0 | | UART/SIO ch. 0 data input pin |
| 9 | P24 | I | General-purpose I/O port |
| | SDA0 | | I ² C data I/O pin |
| 10 | P23 | I | General-purpose I/O port |
| | SCL0 | | I ² C clock I/O pin |
| 11 | P22 | H | General-purpose I/O port |
| | TO00 | | 8/16-bit composite timer ch. 0 output pin |
| 12 | P21 | H | General-purpose I/O port |
| | PPG01 | | 8/16-bit PPG ch. 0 output pin |
| 13 | P20 | H | General-purpose I/O port |
| | PPG00 | | 8/16-bit PPG ch. 0 output pin |
| 14 | X0 | A | Main clock oscillation pin |
| 15 | X1 | A | Main clock oscillation pin |
| 16 | V _{ss} | — | Power supply pin (GND) |
| 17 | V _{cc} | — | Power supply pin |
| 18 | P90 | R | General-purpose I/O port |
| | V3 | | LCDC drive power supply pin |

(Continued)

MB95310L/370L Series

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|------------------|-------------------|-----------------------------------|
| 19 | X1A | A | Subclock oscillation pin (32 kHz) |
| 20 | X0A | | Subclock oscillation pin (32 kHz) |
| 21 | \overline{RST} | B | Reset pin |
| 22 | P91 | R | General-purpose I/O port |
| | V2 | | LCDC drive power supply pin |
| 23 | P92 | R | General-purpose I/O port |
| | V1 | | LCDC drive power supply pin |
| 24 | PA0 | M | General-purpose I/O port |
| | COM0 | | LCDC COM output pin |
| 25 | PA1 | M | General-purpose I/O port |
| | COM1 | | LCDC COM output pin |
| 26 | PA2 | M | General-purpose I/O port |
| | COM2 | | LCDC COM output pin |
| 27 | PA3 | M | General-purpose I/O port |
| | COM3 | | LCDC COM output pin |
| 28 | PB0 | M | General-purpose I/O port |
| | SEG00 | | LCDC SEG output pin |
| 29 | PB1 | M | General-purpose I/O port |
| | SEG01 | | LCDC SEG output pin |
| 30 | PB2 | M | General-purpose I/O port |
| | SEG02 | | LCDC SEG output pin |
| 31 | PB3 | M | General-purpose I/O port |
| | SEG03 | | LCDC SEG output pin |
| 32 | PB4 | M | General-purpose I/O port |
| | SEG04 | | LCDC SEG output pin |
| 33 | PB5 | M | General-purpose I/O port |
| | SEG05 | | LCDC SEG output pin |
| 34 | PB6 | M | General-purpose I/O port |
| | SEG06 | | LCDC SEG output pin |
| 35 | PB7 | M | General-purpose I/O port |
| | SEG07 | | LCDC SEG output pin |
| 36 | PC0 | M | General-purpose I/O port |
| | SEG08 | | LCDC SEG output pin |
| 37 | PC1 | M | General-purpose I/O port |
| | SEG09 | | LCDC SEG output pin |
| 38 | PC2 | M | General-purpose I/O port |
| | SEG10 | | LCDC SEG output pin |

(Continued)

MB95310L/370L Series

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|----------|-------------------|--------------------------------------|
| 39 | PC3 | M | General-purpose I/O port |
| | SEG11 | | LCDC SEG output pin |
| 40 | P60 | M | General-purpose I/O port |
| | SEG12 | | LCDC SEG output pin |
| 41 | P61 | M | General-purpose I/O port |
| | SEG13 | | LCDC SEG output pin |
| 42 | P62 | M | General-purpose I/O port |
| | SEG14 | | LCDC SEG output pin |
| 43 | P63 | M | General-purpose I/O port |
| | SEG15 | | LCDC SEG output pin |
| 44 | P64 | M | General-purpose I/O port |
| | SEG16 | | LCDC SEG output pin |
| 45 | P65 | M | General-purpose I/O port |
| | SEG17 | | LCDC SEG output pin |
| 46 | P66 | M | General-purpose I/O port |
| | SEG18 | | LCDC SEG output pin |
| 47 | P67 | M | General-purpose I/O port |
| | SEG19 | | LCDC SEG output pin |
| 48 | PE0 | M | General-purpose I/O port |
| | SEG20 | | LCDC SEG output pin |
| 49 | PE1 | M | General-purpose I/O port |
| | SEG21 | | LCDC SEG output pin |
| 50 | PE2 | M | General-purpose I/O port |
| | SEG22 | | LCDC SEG output pin |
| 51 | PE3 | M | General-purpose I/O port |
| | SEG23 | | LCDC SEG output pin |
| 52 | PE4 | M | General-purpose I/O port |
| | SEG24 | | LCDC SEG output pin |
| 53 | PE5 | M | General-purpose I/O port |
| | SEG25 | | LCDC SEG output pin |
| | TO0 | | 16-bit reload timer ch. 0 output pin |
| 54 | PE6 | N | General-purpose I/O port |
| | SEG26 | | LCDC SEG output pin |
| | UI1 | | UART/SIO ch. 1 data input pin |
| 55 | PE7 | M | General-purpose I/O port |
| | SEG27 | | LCDC SEG output pin |
| | UO1 | | UART/SIO ch. 1 data output pin |

(Continued)

MB95310L/370L Series

(Continued)

| Pin no. | Pin name | I/O circuit type* | Function |
|---------|------------------|-------------------|--|
| 56 | P07 | Q | General-purpose I/O port |
| | INT07 | | External interrupt input pin |
| | SEG28 | | LCDC SEG output pin |
| | UCK1 | | UART/SIO ch. 1 clock I/O pin |
| 57 | P06 | Q | General-purpose I/O port |
| | INT06 | | External interrupt input pin |
| | SEG29 | | LCDC SEG output pin |
| | TO11 | | 8/16-bit composite timer ch. 1 output pin |
| 58 | P05 | Q | General-purpose I/O port |
| | INT05 | | External interrupt input pin |
| | SEG30 | | LCDC SEG output pin |
| | TO10 | | 8/16-bit composite timer ch. 1 output pin |
| 59 | P04 | Q | General-purpose I/O port |
| | INT04 | | External interrupt input pin |
| | SEG31 | | LCDC SEG output pin |
| | EC1 | | 8/16-bit composite timer ch. 1 clock input pin |
| 60 | P03 | J | General-purpose I/O port |
| | INT03 | | External interrupt input pin |
| | AN03 | | A/D analog input pin |
| 61 | P02 | J | General-purpose I/O port |
| | INT02 | | External interrupt input pin |
| | AN02 | | A/D analog input pin |
| 62 | P01 | J | General-purpose I/O port |
| | INT01 | | External interrupt input pin |
| | AN01 | | A/D analog input pin |
| 63 | P00 | J | General-purpose I/O port |
| | INT00 | | External interrupt input pin |
| | AN00 | | A/D analog input pin |
| 64 | AV _{ss} | — | A/D converter power supply pin (GND) |

*: For the I/O circuit types, see “■ I/O CIRCUIT TYPE”.

MB95310L/370L Series

■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|------|---------|--|
| A | | <ul style="list-style-type: none"> • Oscillation circuit • High-speed side Feedback resistance: approx. 1 MΩ • Low-speed side Feedback resistance: approx. 24 MΩ Dumping resistance: approx. 144 kΩ |
| B | | Reset input |
| C | | <ul style="list-style-type: none"> • N-ch open drain output • Hysteresis input |
| G | | <ul style="list-style-type: none"> • CMOS output • Hysteresis input • CMOS input • Pull-up control available |
| H | | <ul style="list-style-type: none"> • CMOS output • Hysteresis input • Pull-up control available |

(Continued)

MB95310L/370L Series

| Type | Circuit | Remarks |
|------|---------|--|
| I | | <ul style="list-style-type: none"> • N-ch open drain output • CMOS input • Hysteresis input |
| J | | <ul style="list-style-type: none"> • CMOS output • Hysteresis input • Analog input • Pull-up control available |
| M | | <ul style="list-style-type: none"> • CMOS output • LCD output • Hysteresis input |
| N | | <ul style="list-style-type: none"> • CMOS output • LCD output • Hysteresis input • CMOS input |

(Continued)

MB95310L/370L Series

(Continued)

| Type | Circuit | Remarks |
|------|---------|---|
| Q | | <ul style="list-style-type: none"> • CMOS output • LCD output • Hysteresis input |
| R | | <ul style="list-style-type: none"> • CMOS output • LCD power supply • Hysteresis input |

■ NOTES ON DEVICE HANDLING

- Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.

In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in “1. Absolute Maximum Ratings” of “■ ELECTRICAL CHARACTERISTICS” is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.

When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

- Stabilizing supply voltage

Supply voltage must be stabilized.

A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.

As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

- Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

■ PIN CONNECTION

- Treatment of unused input pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 k Ω . Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

- Notes on handling the external clock pins while using the CR clock

Connect the X0 pin and the X0A pin to the V_{SS} pin and leave the X1 pin and the X1A pin unconnected.

- Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.

It is also advisable to connect a ceramic capacitor of approximately 0.1 μ F as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

- DBG pin

Connect the DBG pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the debug mode due to noise, minimize the distance between the DBG pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.

The DBG pin should not stay at “L” level after power-on until the reset output is released.

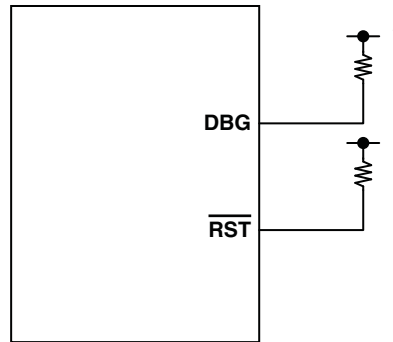
- \overline{RST} pin

Connect the \overline{RST} pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the reset mode due to noise, minimize the distance between the \overline{RST} pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.

MB95310L/370L Series

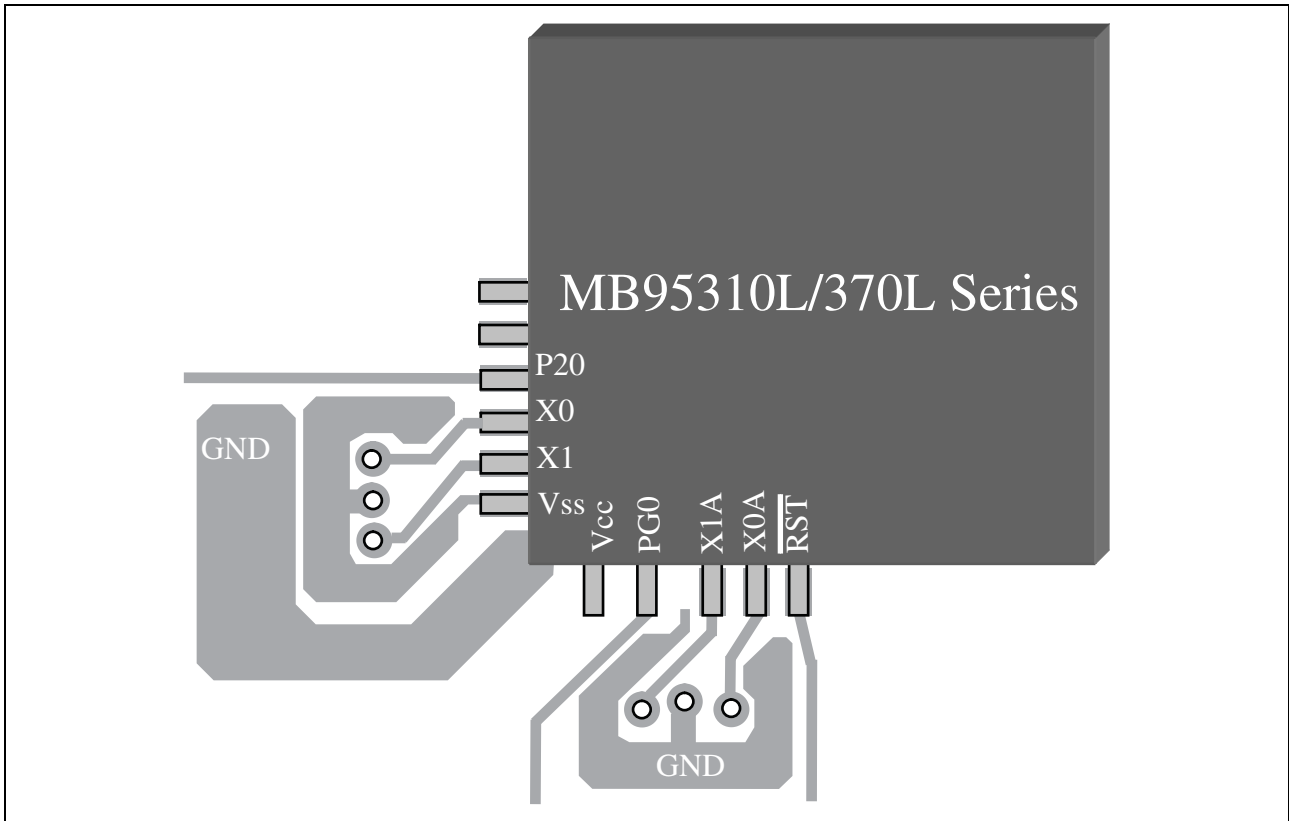
- DBG/ $\overline{\text{RST}}$ pins connection diagram



*: Since the DBG input pin becomes a communication pin in on-chip debug mode, set a pull-up resistor value suiting the input/output specifications of P12/DBG.

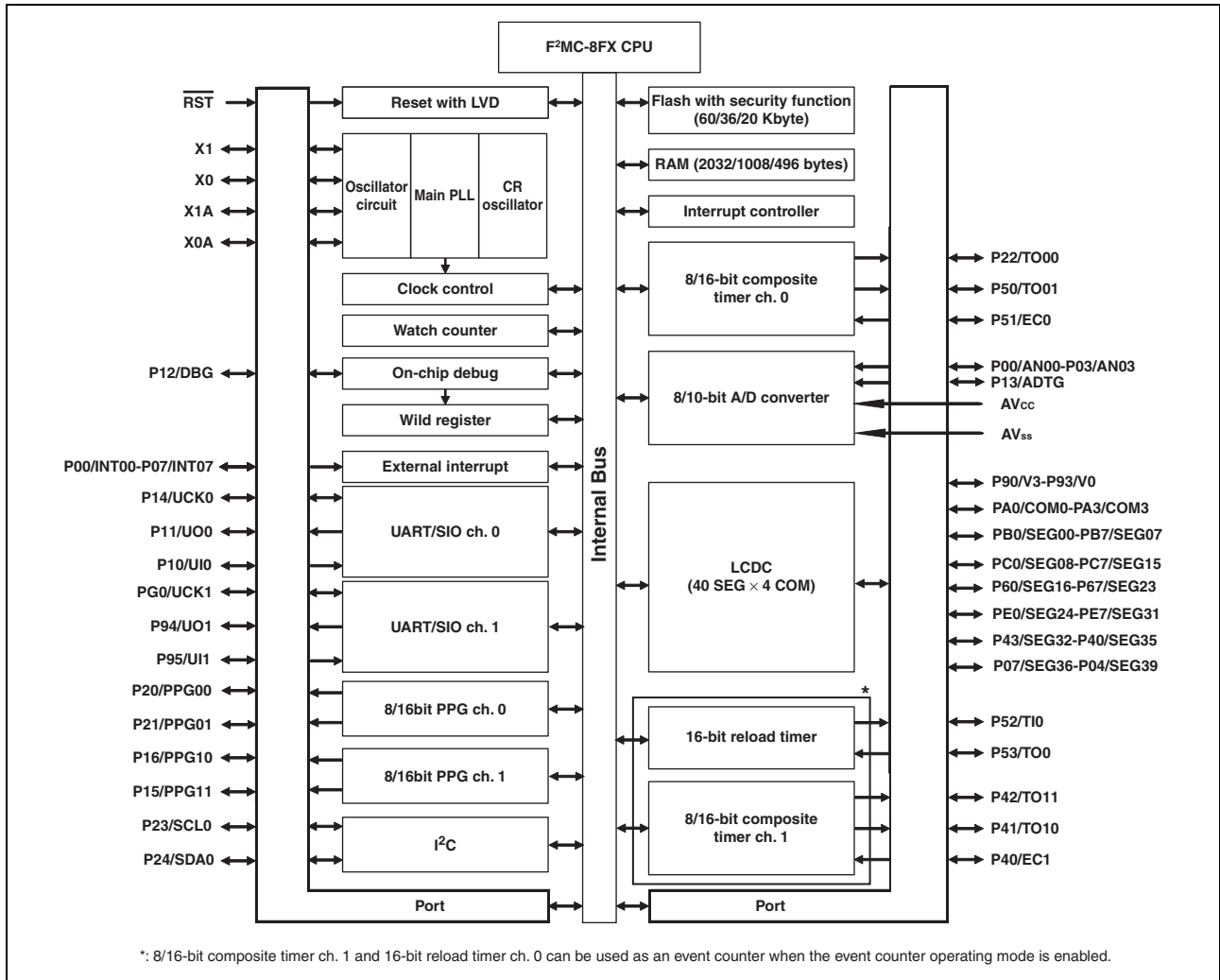
■ RECOMMENDED LAYOUT

- GND wire should be placed around X0, X1, X0A and X1A
The recommended layout method illustrated in following diagram aims to avoid noise coupled between the oscillator pins and GPIO, which may cause the main oscillator or the suboscillator to malfunction.

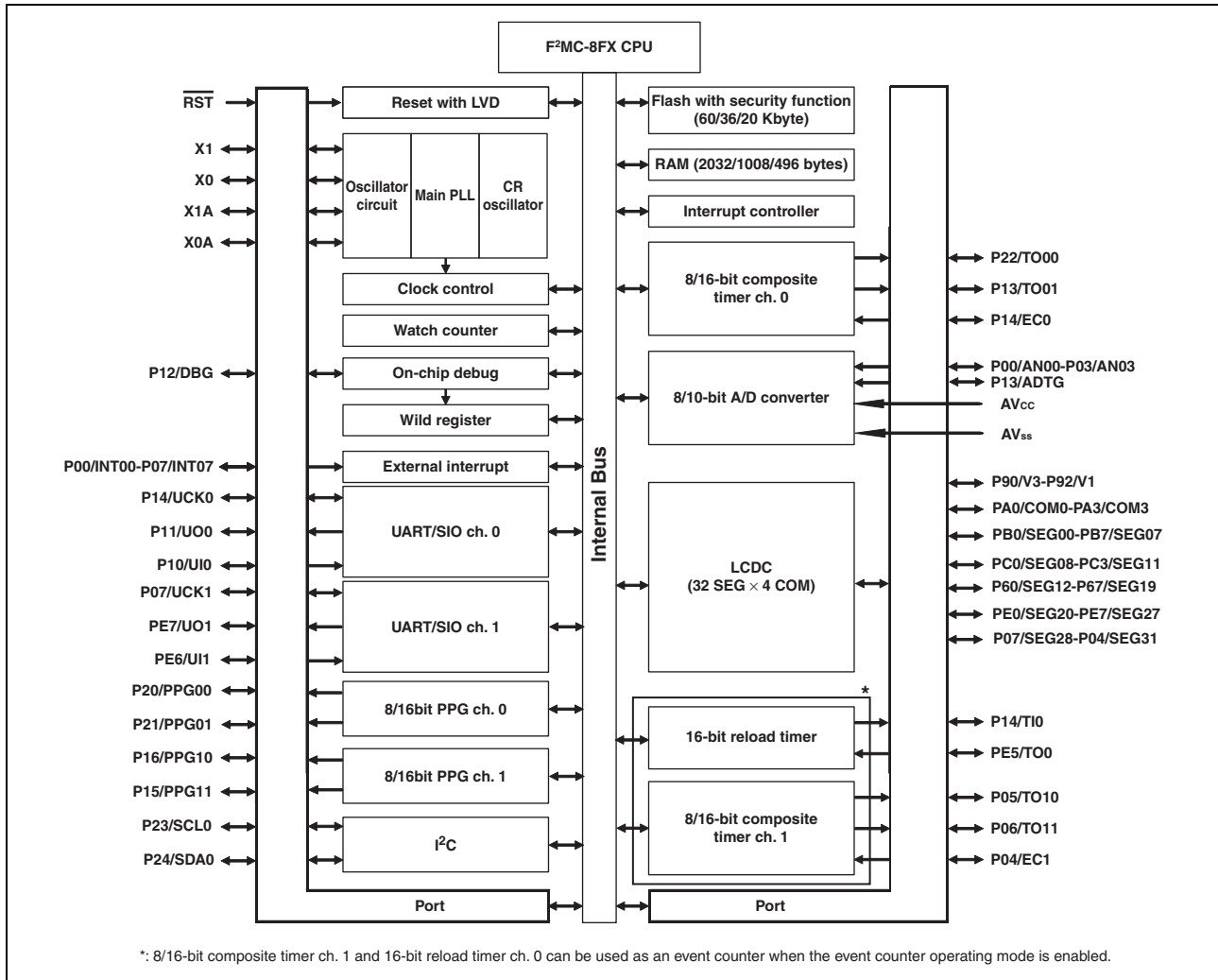


MB95310L/370L Series

■ BLOCK DIAGRAM (MB95310L Series)



■ BLOCK DIAGRAM (MB95370L Series)



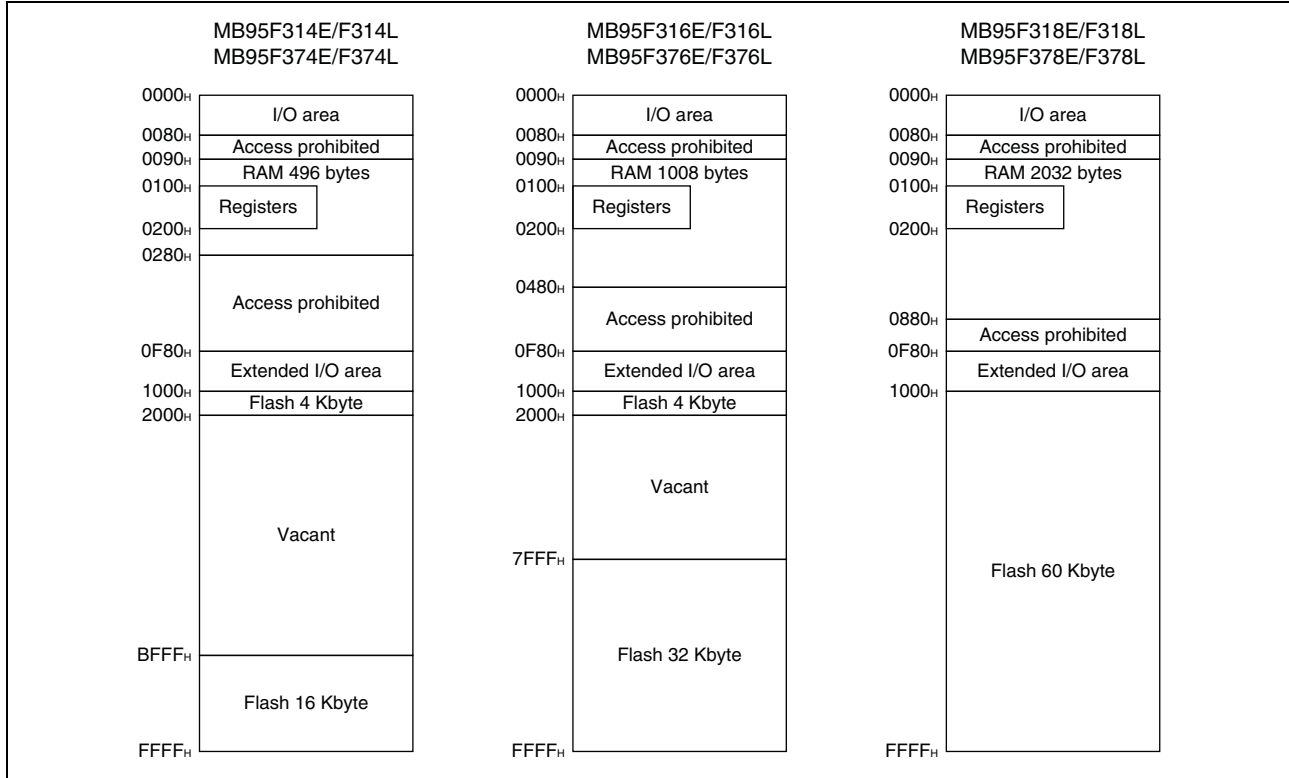
MB95310L/370L Series

■ CPU CORE

• Memory Space

The memory space of the MB95310L/370L Series is 64 Kbyte in size, and consists of an I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95310L/370L Series are shown below.

• Memory Maps



MB95310L/370L Series

■ I/O MAP (MB95310L Series)

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|--|-----|-----------------------|
| 0000 _H | PDR0 | Port 0 data register | R/W | 00000000 _B |
| 0001 _H | DDR0 | Port 0 direction register | R/W | 00000000 _B |
| 0002 _H | PDR1 | Port 1 data register | R/W | 00000000 _B |
| 0003 _H | DDR1 | Port 1 direction register | R/W | 00000000 _B |
| 0004 _H | — | (Disabled) | — | — |
| 0005 _H | WATR | Oscillation stabilization wait time setting register | R/W | 11111111 _B |
| 0006 _H | PLLC | PLL control register | R/W | 00000000 _B |
| 0007 _H | SYCC | System clock control register | R/W | XXXXXX11 _B |
| 0008 _H | STBC | Standby control register | R/W | 0000XXX _B |
| 0009 _H | RSRR | Reset source register | R/W | 000XXXX _B |
| 000A _H | TBTC | Time-base timer control register | R/W | 00000000 _B |
| 000B _H | WPCR | Watch prescaler control register | R/W | 00000000 _B |
| 000C _H | WDTC | Watchdog timer control register | R/W | 00000000 _B |
| 000D _H | SYCC2 | System clock control register 2 | R/W | XX100011 _B |
| 000E _H | PDR2 | Port 2 data register | R/W | 00000000 _B |
| 000F _H | DDR2 | Port 2 direction register | R/W | 00000000 _B |
| 0010 _H , 0011 _H | — | (Disabled) | — | — |
| 0012 _H | PDR4 | Port 4 data register | R/W | 00000000 _B |
| 0013 _H | DDR4 | Port 4 direction register | R/W | 00000000 _B |
| 0014 _H | PDR5 | Port 5 data register | R/W | 00000000 _B |
| 0015 _H | DDR5 | Port 5 direction register | R/W | 00000000 _B |
| 0016 _H | PDR6 | Port 6 data register | R/W | 00000000 _B |
| 0017 _H | DDR6 | Port 6 direction register | R/W | 00000000 _B |
| 0018 _H to 001B _H | — | (Disabled) | — | — |
| 001C _H | PDR9 | Port 9 data register | R/W | 00000000 _B |
| 001D _H | DDR9 | Port 9 direction register | R/W | 00000000 _B |
| 001E _H | PDRA | Port A data register | R/W | 00000000 _B |
| 001F _H | DDRA | Port A direction register | R/W | 00000000 _B |
| 0020 _H | PDRB | Port B data register | R/W | 00000000 _B |
| 0021 _H | DDRB | Port B direction register | R/W | 00000000 _B |
| 0022 _H | PDRC | Port C data register | R/W | 00000000 _B |
| 0023 _H | DDRC | Port C direction register | R/W | 00000000 _B |
| 0024 _H , 0025 _H | — | (Disabled) | — | — |

(Continued)

MB95310L/370L Series

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|---|-----|-----------------------|
| 0026 _H | PDRE | Port E data register | R/W | 00000000 _B |
| 0027 _H | DDRE | Port E direction register | R/W | 00000000 _B |
| 0028 _H , 0029 _H | — | (Disabled) | — | — |
| 002A _H | PDRG | Port G data register | R/W | 00000000 _B |
| 002B _H | DDRG | Port G direction register | R/W | 00000000 _B |
| 002C _H | PUL0 | Port 0 pull-up register | R/W | 00000000 _B |
| 002D _H | PUL1 | Port 1 pull-up register | R/W | 00000000 _B |
| 002E _H | PUL2 | Port 2 pull-up register | R/W | 00000000 _B |
| 002F _H , 0030 _H | — | (Disabled) | — | — |
| 0031 _H | PUL5 | Port 5 pull-up register | R/W | 00000000 _B |
| 0032 _H , 0033 _H | — | (Disabled) | — | — |
| 0034 _H | PUL9 | Port 9 pull-up register | R/W | 00000000 _B |
| 0035 _H | PULG | Port G pull-up register | R/W | 00000000 _B |
| 0036 _H | T01CR1 | 8/16-bit composite timer 01 status control register 1 ch. 0 | R/W | 00000000 _B |
| 0037 _H | T00CR1 | 8/16-bit composite timer 00 status control register 1 ch. 0 | R/W | 00000000 _B |
| 0038 _H | T11CR1 | 8/16-bit composite timer 11 status control register 1 ch. 1 | R/W | 00000000 _B |
| 0039 _H | T10CR1 | 8/16-bit composite timer 10 status control register 1 ch. 1 | R/W | 00000000 _B |
| 003A _H | PC01 | 8/16-bit PPG01 control register ch. 0 | R/W | 00000000 _B |
| 003B _H | PC00 | 8/16-bit PPG00 control register ch. 0 | R/W | 00000000 _B |
| 003C _H | PC11 | 8/16-bit PPG11 control register ch. 1 | R/W | 00000000 _B |
| 003D _H | PC10 | 8/16-bit PPG10 control register ch. 1 | R/W | 00000000 _B |
| 003E _H | TMCSRH | 16-bit reload timer control status register upper ch. 0 | R/W | 00000000 _B |
| 003F _H | TMCSRL | 16-bit reload timer control status register lower ch. 0 | R/W | 00000000 _B |
| 0040 _H to 0047 _H | — | (Disabled) | — | — |
| 0048 _H | EIC00 | External interrupt circuit control register ch. 0/ch. 1 | R/W | 00000000 _B |
| 0049 _H | EIC10 | External interrupt circuit control register ch. 2/ch. 3 | R/W | 00000000 _B |
| 004A _H | EIC20 | External interrupt circuit control register ch. 4/ch. 5 | R/W | 00000000 _B |
| 004B _H | EIC30 | External interrupt circuit control register ch. 6/ch. 7 | R/W | 00000000 _B |
| 004C _H , 004D _H | — | (Disabled) | — | — |
| 004E _H | LVDR | LVD reset voltage selection ID register | R/W | 00000000 _B |
| 004F _H | LVDC | LVD control register | R/W | X000000X _B |
| 0050 _H to 0055 _H | — | (Disabled) | — | — |

(Continued)

MB95310L/370L Series

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|---|-----|-----------------------|
| 0056 _H | SMC10 | UART/SIO serial mode control register 1 ch. 0 | R/W | 00000000 _B |
| 0057 _H | SMC20 | UART/SIO serial mode control register 2 ch. 0 | R/W | 00100000 _B |
| 0058 _H | SSR0 | UART/SIO serial status register ch. 0 | R/W | 00000001 _B |
| 0059 _H | TDR0 | UART/SIO output data register ch. 0 | R/W | 00000000 _B |
| 005A _H | RDR0 | UART/SIO input data register ch. 0 | R | 00000000 _B |
| 005B _H | SMC11 | UART/SIO serial mode control register 1 ch. 1 | R/W | 00000000 _B |
| 005C _H | SMC21 | UART/SIO serial mode control register 2 ch. 1 | R/W | 00100000 _B |
| 005D _H | SSR1 | UART/SIO serial status register ch. 1 | R/W | 00000001 _B |
| 005E _H | TDR1 | UART/SIO output data register ch. 1 | R/W | 00000000 _B |
| 005F _H | RDR1 | UART/SIO input data register ch. 1 | R | 00000000 _B |
| 0060 _H | IBCR00 | I ² C bus control register 0 | R/W | 00000001 _B |
| 0061 _H | IBCR10 | I ² C bus control register 1 | R/W | 00000000 _B |
| 0062 _H | IBCR0 | I ² C bus status register | R | 00000000 _B |
| 0063 _H | IDDR0 | I ² C data register | R/W | 00000000 _B |
| 0064 _H | IAAR0 | I ² C address register | R/W | 00000000 _B |
| 0065 _H | ICCR0 | I ² C clock control register | R/W | 00000000 _B |
| 0066 _H to 006B _H | — | (Disabled) | — | — |
| 006C _H | ADC1 | 8/10-bit A/D converter control register 1 | R/W | 00000000 _B |
| 006D _H | ADC2 | 8/10-bit A/D converter control register 2 | R/W | 00000000 _B |
| 006E _H | ADDH | 8/10-bit A/D converter data register upper | R/W | 00000000 _B |
| 006F _H | ADDL | 8/10-bit A/D converter data register lower | R/W | 00000000 _B |
| 0070 _H | WCSR | Watch counter status register | R/W | 00000000 _B |
| 0071 _H | FSR2 | Flash memory status register 2 | R/W | 00000000 _B |
| 0072 _H | FSR | Flash memory status register | R/W | 000X0000 _B |
| 0073 _H | SWRE0 | Flash memory sector write control register 0 | R/W | 00000000 _B |
| 0074 _H | FSR3 | Flash memory status register 3 | R | 00000000 _B |
| 0075 _H | — | (Disabled) | — | — |
| 0076 _H | WREN | Wild register address compare enable register | R/W | 00000000 _B |
| 0077 _H | WROR | Wild register data test setting register | R/W | 00000000 _B |
| 0078 _H | — | Mirror of register bank pointer (RP) and direct bank pointer (DP) | — | — |

(Continued)

MB95310L/370L Series

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|--|-----|-----------------------|
| 0079 _H | ILR0 | Interrupt level setting register 0 | R/W | 11111111 _B |
| 007A _H | ILR1 | Interrupt level setting register 1 | R/W | 11111111 _B |
| 007B _H | ILR2 | Interrupt level setting register 2 | R/W | 11111111 _B |
| 007C _H | ILR3 | Interrupt level setting register 3 | R/W | 11111111 _B |
| 007D _H | ILR4 | Interrupt level setting register 4 | R/W | 11111111 _B |
| 007E _H | ILR5 | Interrupt level setting register 5 | R/W | 11111111 _B |
| 007F _H | — | (Disabled) | — | — |
| 0F80 _H | WRARH0 | Wild register address setting register (upper) ch. 0 | R/W | 00000000 _B |
| 0F81 _H | WRARL0 | Wild register address setting register (lower) ch. 0 | R/W | 00000000 _B |
| 0F82 _H | WRDR0 | Wild register data setting register ch. 0 | R/W | 00000000 _B |
| 0F83 _H | WRARH1 | Wild register address setting register (upper) ch. 1 | R/W | 00000000 _B |
| 0F84 _H | WRARL1 | Wild register address setting register (lower) ch. 1 | R/W | 00000000 _B |
| 0F85 _H | WRDR1 | Wild register data setting register ch. 1 | R/W | 00000000 _B |
| 0F86 _H | WRARH2 | Wild register address setting register (upper) ch. 2 | R/W | 00000000 _B |
| 0F87 _H | WRARL2 | Wild register address setting register (lower) ch. 2 | R/W | 00000000 _B |
| 0F88 _H | WRDR2 | Wild register data setting register ch. 2 | R/W | 00000000 _B |
| 0F89 _H to 0F91 _H | — | (Disabled) | — | — |
| 0F92 _H | T01CR0 | 8/16-bit composite timer 01 status control register 0 ch. 0 | R/W | 00000000 _B |
| 0F93 _H | T00CR0 | 8/16-bit composite timer 00 status control register 0 ch. 0 | R/W | 00000000 _B |
| 0F94 _H | T01DR | 8/16-bit composite timer 01 data register ch. 0 | R/W | 00000000 _B |
| 0F95 _H | T00DR | 8/16-bit composite timer 00 data register ch. 0 | R/W | 00000000 _B |
| 0F96 _H | TMCR0 | 8/16-bit composite timer 00/01 timer mode control register ch. 0 | R/W | 00000000 _B |
| 0F97 _H | T11CR0 | 8/16-bit composite timer 11 status control register 0 ch. 1 | R/W | 00000000 _B |
| 0F98 _H | T10CR0 | 8/16-bit composite timer 10 status control register 0 ch. 1 | R/W | 00000000 _B |
| 0F99 _H | T11DR | 8/16-bit composite timer 11 data register ch. 1 | R/W | 00000000 _B |
| 0F9A _H | T10DR | 8/16-bit composite timer 10 data register ch. 1 | R/W | 00000000 _B |
| 0F9B _H | TMCR1 | 8/16-bit composite timer 10/11 timer mode control register ch. 1 | R/W | 00000000 _B |
| 0F9C _H | PPS01 | 8/16-bit PPG01 cycle setting buffer register ch. 0 | R/W | 11111111 _B |
| 0F9D _H | PPS00 | 8/16-bit PPG00 cycle setting buffer register ch. 0 | R/W | 11111111 _B |
| 0F9E _H | PDS01 | 8/16-bit PPG01 duty setting buffer register ch. 0 | R/W | 11111111 _B |
| 0F9F _H | PDS00 | 8/16-bit PPG00 duty setting buffer register ch. 0 | R/W | 11111111 _B |
| 0FA0 _H | PPS11 | 8/16-bit PPG11 cycle setting buffer register ch. 1 | R/W | 11111111 _B |
| 0FA1 _H | PPS10 | 8/16-bit PPG10 cycle setting buffer register ch. 1 | R/W | 11111111 _B |
| 0FA2 _H | PDS11 | 8/16-bit PPG11 duty setting buffer register ch. 1 | R/W | 11111111 _B |
| 0FA3 _H | PDS10 | 8/16-bit PPG10 duty setting buffer register ch. 1 | R/W | 11111111 _B |

(Continued)

MB95310L/370L Series

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|---|-----|-----------------------|
| 0FA4 _H | PPGS | 8/16-bit PPG start register | R/W | 00000000 _B |
| 0FA5 _H | REVC | 8/16-bit PPG output inversion register | R/W | 00000000 _B |
| 0FA6 _H | TMRH0 | 16-bit reload timer timer register upper | R/W | 00000000 _B |
| | TMRLRH0 | 16-bit reload timer reload register upper | R/W | 00000000 _B |
| 0FA7 _H | TMRL0 | 16-bit reload timer timer register lower | R/W | 00000000 _B |
| | TMRLRL0 | 16-bit reload timer reload register lower | R/W | 00000000 _B |
| 0FA8 _H to 0FBD _H | — | (Disabled) | — | — |
| 0FBE _H | PSSR0 | UART/SIO dedicated baud rate generator prescaler selecting register ch. 0 | R/W | 00000000 _B |
| 0FBF _H | BRSR0 | UART/SIO dedicated baud rate generator baud rate setting register ch. 0 | R/W | 00000000 _B |
| 0FC0 _H | PSSR1 | UART/SIO dedicated baud rate generator prescaler selecting register ch. 1 | R/W | 00000000 _B |
| 0FC1 _H | BRSR1 | UART/SIO dedicated baud rate generator baud rate setting register ch. 1 | R/W | 00000000 _B |
| 0FC2 _H | — | (Disabled) | — | — |
| 0FC3 _H | AIDRL | A/D input disable register (lower) | R/W | 00000000 _B |
| 0FC4 _H | LCDC | LCDC control register | R/W | 00010000 _B |
| 0FC5 _H | LCDCE1 | LCDC enable register 1 | R/W | 00110000 _B |
| 0FC6 _H | LCDCE2 | LCDC enable register 2 | R/W | 00000000 _B |
| 0FC7 _H | LCDCE3 | LCDC enable register 3 | R/W | 00000000 _B |
| 0FC8 _H | LCDCE4 | LCDC enable register 4 | R/W | 00000000 _B |
| 0FC9 _H | LCDCE5 | LCDC enable register 5 | R/W | 00000000 _B |
| 0FCA _H | LCDCE6 | LCDC enable register 6 | R/W | 00000000 _B |
| 0FCB _H | LCDCB1 | LCDC blinking setting register 1 | R/W | 00000000 _B |
| 0FCC _H | LCDCB2 | LCDC blinking setting register 2 | R/W | 00000000 _B |
| 0FCD _H to 0FE0 _H | LCDRAM | LCDC display RAM | R/W | 00000000 _B |
| 0FE1 _H | — | (Disabled) | — | — |
| 0FE2 _H | EVCR | Event counter control register | R/W | 00000000 _B |
| 0FE3 _H | WCDR | Watch counter data register | R/W | 00111111 _B |
| 0FE4 _H | CRTH | Main CR clock trimming register (upper) | R/W | 0XXXXXXX _B |
| 0FE5 _H | CRTL | Main CR clock trimming register (lower) | R/W | 00XXXXXX _B |
| 0FE6 _H to 0FE8 _H | — | (Disabled) | — | — |
| 0FE9 _H | CMCR | Clock monitoring control register | R/W | XX000000 _B |
| 0FEA _H | CMDR | Clock monitoring data register | R | 00000000 _B |

(Continued)

MB95310L/370L Series

(Continued)

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|--|-----|-----------------------|
| 0FEB _H | WDTH | Watchdog timer selection ID register (upper) | R | XXXXXXXX _B |
| 0FEC _H | WDTL | Watchdog timer selection ID register (lower) | R | XXXXXXXX _B |
| 0FED _H | — | (Disabled) | — | — |
| 0FEE _H | ILSR | Input level select register | R/W | 00000000 _B |
| 0FEF _H | WICR | Interrupt pin control register | R/W | 01000000 _B |
| 0FF0 _H to 0FFF _H | — | (Disabled) | — | — |

- R/W access symbols

R/W : Readable / Writable

R : Read only

- Initial value symbols

0 : The initial value of this bit is “0”.

1 : The initial value of this bit is “1”.

X : The initial value of this bit is indeterminate.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

MB95310L/370L Series

■ I/O MAP (MB95370L Series)

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|--|-----|-----------------------|
| 0000 _H | PDR0 | Port 0 data register | R/W | 00000000 _B |
| 0001 _H | DDR0 | Port 0 direction register | R/W | 00000000 _B |
| 0002 _H | PDR1 | Port 1 data register | R/W | 00000000 _B |
| 0003 _H | DDR1 | Port 1 direction register | R/W | 00000000 _B |
| 0004 _H | — | (Disabled) | — | — |
| 0005 _H | WATR | Oscillation stabilization wait time setting register | R/W | 11111111 _B |
| 0006 _H | PLLC | PLL control register | R/W | 00000000 _B |
| 0007 _H | SYCC | System clock control register | R/W | XXXXXX11 _B |
| 0008 _H | STBC | Standby control register | R/W | 0000XXX _B |
| 0009 _H | RSRR | Reset source register | R/W | 000XXXX _B |
| 000A _H | TBTC | Time-base timer control register | R/W | 00000000 _B |
| 000B _H | WPCR | Watch prescaler control register | R/W | 00000000 _B |
| 000C _H | WDTC | Watchdog timer control register | R/W | 00000000 _B |
| 000D _H | SYCC2 | System clock control register 2 | R/W | XX100011 _B |
| 000E _H | PDR2 | Port 2 data register | R/W | 00000000 _B |
| 000F _H | DDR2 | Port 2 direction register | R/W | 00000000 _B |
| 0010 _H to 0015 _H | — | (Disabled) | — | — |
| 0016 _H | PDR6 | Port 6 data register | R/W | 00000000 _B |
| 0017 _H | DDR6 | Port 6 direction register | R/W | 00000000 _B |
| 0018 _H to 001B _H | — | (Disabled) | — | — |
| 001C _H | PDR9 | Port 9 data register | R/W | 00000000 _B |
| 001D _H | DDR9 | Port 9 direction register | R/W | 00000000 _B |
| 001E _H | PDRA | Port A data register | R/W | 00000000 _B |
| 001F _H | DDRA | Port A direction register | R/W | 00000000 _B |
| 0020 _H | PDRB | Port B data register | R/W | 00000000 _B |
| 0021 _H | DDRB | Port B direction register | R/W | 00000000 _B |
| 0022 _H | PDRC | Port C data register | R/W | 00000000 _B |
| 0023 _H | DDRC | Port C direction register | R/W | 00000000 _B |
| 0024 _H , 0025 _H | — | (Disabled) | — | — |
| 0026 _H | PDRE | Port E data register | R/W | 00000000 _B |
| 0027 _H | DDRE | Port E direction register | R/W | 00000000 _B |
| 0028 _H to 002B _H | — | (Disabled) | — | — |
| 002C _H | PUL0 | Port 0 pull-up register | R/W | 00000000 _B |
| 002D _H | PUL1 | Port 1 pull-up register | R/W | 00000000 _B |
| 002E _H | PUL2 | Port 2 pull-up register | R/W | 00000000 _B |

(Continued)

MB95310L/370L Series

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|---|-----|------------------------|
| 002F _H to 0033 _H | — | (Disabled) | — | — |
| 0034 _H | PUL9 | Port 9 pull-up register | R/W | 00000000 _B |
| 0035 _H | — | (Disabled) | — | — |
| 0036 _H | T01CR1 | 8/16-bit composite timer 01 status control register 1 ch. 0 | R/W | 00000000 _B |
| 0037 _H | T00CR1 | 8/16-bit composite timer 00 status control register 1 ch. 0 | R/W | 00000000 _B |
| 0038 _H | T11CR1 | 8/16-bit composite timer 11 status control register 1 ch. 1 | R/W | 00000000 _B |
| 0039 _H | T10CR1 | 8/16-bit composite timer 10 status control register 1 ch. 1 | R/W | 00000000 _B |
| 003A _H | PC01 | 8/16-bit PPG01 control register ch. 0 | R/W | 00000000 _B |
| 003B _H | PC00 | 8/16-bit PPG00 control register ch. 0 | R/W | 00000000 _B |
| 003C _H | PC11 | 8/16-bit PPG11 control register ch. 1 | R/W | 00000000 _B |
| 003D _H | PC10 | 8/16-bit PPG10 control register ch. 1 | R/W | 00000000 _B |
| 003E _H | TMCSRH | 16-bit reload timer control status register upper ch. 0 | R/W | 00000000 _B |
| 003F _H | TMCSRL | 16-bit reload timer control status register lower ch. 0 | R/W | 00000000 _B |
| 0040 _H to 0047 _H | — | (Disabled) | — | — |
| 0048 _H | EIC00 | External interrupt circuit control register ch. 0/ch. 1 | R/W | 00000000 _B |
| 0049 _H | EIC10 | External interrupt circuit control register ch. 2/ch. 3 | R/W | 00000000 _B |
| 004A _H | EIC20 | External interrupt circuit control register ch. 4/ch. 5 | R/W | 00000000 _B |
| 004B _H | EIC30 | External interrupt circuit control register ch. 6/ch. 7 | R/W | 00000000 _B |
| 004C _H , 004D _H | — | (Disabled) | — | — |
| 004E _H | LVDR | LVD reset voltage selection ID register | R/W | 00000000 _B |
| 004F _H | LVDC | LVD control register | R/W | X0000000X _B |
| 0050 _H to 0055 _H | — | (Disabled) | — | — |
| 0056 _H | SMC10 | UART/SIO serial mode control register 1 ch. 0 | R/W | 00000000 _B |
| 0057 _H | SMC20 | UART/SIO serial mode control register 2 ch. 0 | R/W | 00100000 _B |
| 0058 _H | SSR0 | UART/SIO serial status register ch. 0 | R/W | 00000001 _B |
| 0059 _H | TDR0 | UART/SIO output data register ch. 0 | R/W | 00000000 _B |
| 005A _H | RDR0 | UART/SIO input data register ch. 0 | R | 00000000 _B |
| 005B _H | SMC11 | UART/SIO serial mode control register 1 ch. 1 | R/W | 00000000 _B |
| 005C _H | SMC21 | UART/SIO serial mode control register 2 ch. 1 | R/W | 00100000 _B |
| 005D _H | SSR1 | UART/SIO serial status register ch. 1 | R/W | 00000001 _B |
| 005E _H | TDR1 | UART/SIO output data register ch. 1 | R/W | 00000000 _B |
| 005F _H | RDR1 | UART/SIO input data register ch. 1 | R | 00000000 _B |

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MB95310L/370L Series

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|---|-----|-----------------------|
| 0060 _H | IBCR00 | I ² C bus control register 0 | R/W | 00000001 _B |
| 0061 _H | IBCR10 | I ² C bus control register 1 | R/W | 00000000 _B |
| 0062 _H | IBCR0 | I ² C bus status register | R | 00000000 _B |
| 0063 _H | IDDR0 | I ² C data register | R/W | 00000000 _B |
| 0064 _H | IAAR0 | I ² C address register | R/W | 00000000 _B |
| 0065 _H | ICCR0 | I ² C clock control register | R/W | 00000000 _B |
| 0066 _H to 006B _H | — | (Disabled) | — | — |
| 006C _H | ADC1 | 8/10-bit A/D converter control register 1 | R/W | 00000000 _B |
| 006D _H | ADC2 | 8/10-bit A/D converter control register 2 | R/W | 00000000 _B |
| 006E _H | ADDH | 8/10-bit A/D converter data register upper | R/W | 00000000 _B |
| 006F _H | ADDL | 8/10-bit A/D converter data register lower | R/W | 00000000 _B |
| 0070 _H | WCSR | Watch counter status register | R/W | 00000000 _B |
| 0071 _H | FSR2 | Flash memory status register 2 | R/W | 00000000 _B |
| 0072 _H | FSR | Flash memory status register | R/W | 000X0000 _B |
| 0073 _H | SWRE0 | Flash memory sector write control register 0 | R/W | 00000000 _B |
| 0074 _H | FSR3 | Flash memory status register 3 | R | 00000000 _B |
| 0075 _H | — | (Disabled) | — | — |
| 0076 _H | WREN | Wild register address compare enable register | R/W | 00000000 _B |
| 0077 _H | WROR | Wild register data test setting register | R/W | 00000000 _B |
| 0078 _H | — | Mirror of register bank pointer (RP) and direct bank pointer (DP) | — | — |
| 0079 _H | ILR0 | Interrupt level setting register 0 | R/W | 11111111 _B |
| 007A _H | ILR1 | Interrupt level setting register 1 | R/W | 11111111 _B |
| 007B _H | ILR2 | Interrupt level setting register 2 | R/W | 11111111 _B |
| 007C _H | ILR3 | Interrupt level setting register 3 | R/W | 11111111 _B |
| 007D _H | ILR4 | Interrupt level setting register 4 | R/W | 11111111 _B |
| 007E _H | ILR5 | Interrupt level setting register 5 | R/W | 11111111 _B |
| 007F _H | — | (Disabled) | — | — |
| 0F80 _H | WRARH0 | Wild register address setting register (upper) ch. 0 | R/W | 00000000 _B |
| 0F81 _H | WRARL0 | Wild register address setting register (lower) ch. 0 | R/W | 00000000 _B |
| 0F82 _H | WRDR0 | Wild register data setting register ch. 0 | R/W | 00000000 _B |
| 0F83 _H | WRARH1 | Wild register address setting register (upper) ch. 1 | R/W | 00000000 _B |
| 0F84 _H | WRARL1 | Wild register address setting register (lower) ch. 1 | R/W | 00000000 _B |
| 0F85 _H | WRDR1 | Wild register data setting register ch. 1 | R/W | 00000000 _B |
| 0F86 _H | WRARH2 | Wild register address setting register (upper) ch. 2 | R/W | 00000000 _B |
| 0F87 _H | WRARL2 | Wild register address setting register (lower) ch. 2 | R/W | 00000000 _B |
| 0F88 _H | WRDR2 | Wild register data setting register ch. 2 | R/W | 00000000 _B |

(Continued)

MB95310L/370L Series

| Address | Register abbreviation | Register name | R/W | Initial value |
|----------------------|-----------------------|---|-----|-----------------------|
| 0F89H to 0F91H | — | (Disabled) | — | — |
| 0F92H | T01CR0 | 8/16-bit composite timer 01 status control register 0 ch. 0 | R/W | 00000000 _B |
| 0F93H | T00CR0 | 8/16-bit composite timer 00 status control register 0 ch. 0 | R/W | 00000000 _B |
| 0F94H | T01DR | 8/16-bit composite timer 01 data register ch. 0 | R/W | 00000000 _B |
| 0F95H | T00DR | 8/16-bit composite timer 00 data register ch. 0 | R/W | 00000000 _B |
| 0F96H | TMCR0 | 8/16-bit composite timer 00/01 timer mode control register ch. 0 | R/W | 00000000 _B |
| 0F97H | T11CR0 | 8/16-bit composite timer 11 status control register 0 ch. 1 | R/W | 00000000 _B |
| 0F98H | T10CR0 | 8/16-bit composite timer 10 status control register 0 ch. 1 | R/W | 00000000 _B |
| 0F99H | T11DR | 8/16-bit composite timer 11 data register ch. 1 | R/W | 00000000 _B |
| 0F9AH | T10DR | 8/16-bit composite timer 10 data register ch. 1 | R/W | 00000000 _B |
| 0F9BH | TMCR1 | 8/16-bit composite timer 10/11 timer mode control register ch. 1 | R/W | 00000000 _B |
| 0F9CH | PPS01 | 8/16-bit PPG01 cycle setting buffer register ch. 0 | R/W | 11111111 _B |
| 0F9DH | PPS00 | 8/16-bit PPG00 cycle setting buffer register ch. 0 | R/W | 11111111 _B |
| 0F9EH | PDS01 | 8/16-bit PPG01 duty setting buffer register ch. 0 | R/W | 11111111 _B |
| 0F9FH | PDS00 | 8/16-bit PPG00 duty setting buffer register ch. 0 | R/W | 11111111 _B |
| 0FA0H | PPS11 | 8/16-bit PPG11 cycle setting buffer register ch. 1 | R/W | 11111111 _B |
| 0FA1H | PPS10 | 8/16-bit PPG10 cycle setting buffer register ch. 1 | R/W | 11111111 _B |
| 0FA2H | PDS11 | 8/16-bit PPG11 duty setting buffer register ch. 1 | R/W | 11111111 _B |
| 0FA3H | PDS10 | 8/16-bit PPG10 duty setting buffer register ch. 1 | R/W | 11111111 _B |
| 0FA4H | PPGS | 8/16-bit PPG start register | R/W | 00000000 _B |
| 0FA5H | REVC | 8/16-bit PPG output inversion register | R/W | 00000000 _B |
| 0FA6H | TMRH0 | 16-bit reload timer timer register upper | R/W | 00000000 _B |
| | TMRLRH0 | 16-bit reload timer reload register upper | R/W | 00000000 _B |
| 0FA7H | TMRL0 | 16-bit reload timer timer register lower | R/W | 00000000 _B |
| | TMRLRL0 | 16-bit reload timer reload register lower | R/W | 00000000 _B |
| 0FA8H to 0FBDH | — | (Disabled) | — | — |
| 0FBEH | PSSR0 | UART/SIO dedicated baud rate generator prescaler selecting register ch. 0 | R/W | 00000000 _B |
| 0FBFH | BRSR0 | UART/SIO dedicated baud rate generator baud rate setting register ch. 0 | R/W | 00000000 _B |
| 0FC0H | PSSR1 | UART/SIO dedicated baud rate generator prescaler selecting register ch. 1 | R/W | 00000000 _B |
| 0FC1H | BRSR1 | UART/SIO dedicated baud rate generator baud rate setting register ch. 1 | R/W | 00000000 _B |
| 0FC2H | — | (Disabled) | — | — |
| 0FC3H | AIDRL | A/D input disable register (lower) | R/W | 00000000 _B |
| 0FC4H | LCDC | LCDC control register | R/W | 00010000 _B |

(Continued)

MB95310L/370L Series

(Continued)

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|--|-----|-------------------------|
| 0FC5 _H | LCDCE1 | LCDC enable register 1 | R/W | 00110000 _B |
| 0FC6 _H | LCDCE2 | LCDC enable register 2 | R/W | 00000000 _B |
| 0FC7 _H | LCDCE3 | LCDC enable register 3 | R/W | 00000000 _B |
| 0FC8 _H | LCDCE4 | LCDC enable register 4 | R/W | 00000000 _B |
| 0FC9 _H | LCDCE5 | LCDC enable register 5 | R/W | 00000000 _B |
| 0FCA _H | — | (Disabled) | — | — |
| 0FCB _H | LCDCB1 | LCDC blinking setting register 1 | R/W | 00000000 _B |
| 0FCC _H | LCDCB2 | LCDC blinking setting register 2 | R/W | 00000000 _B |
| 0FCD _H to 0FDC _H | LCDRAM | LCDC display RAM | R/W | 00000000 _B |
| 0FDD _H to 0FE1 _H | — | (Disabled) | — | — |
| 0FE2 _H | EVCR | Event counter control register | R/W | 00000000 _B |
| 0FE3 _H | WCDR | Watch counter data register | R/W | 00111111 _B |
| 0FE4 _H | CRTH | Main CR clock trimming register (upper) | R/W | 0XXXXXXXX _B |
| 0FE5 _H | CRTL | Main CR clock trimming register (lower) | R/W | 00XXXXXXXX _B |
| 0FE6 _H to 0FE8 _H | — | (Disabled) | — | — |
| 0FE9 _H | CMCR | Clock monitoring control register | R/W | XX000000 _B |
| 0FEA _H | CMDR | Clock monitoring data register | R | 00000000 _B |
| 0FEB _H | WDTH | Watchdog timer selection ID register (upper) | R | XXXXXXXX _B |
| 0FEC _H | WDTL | Watchdog timer selection ID register (lower) | R | XXXXXXXX _B |
| 0FED _H | — | (Disabled) | — | — |
| 0FEE _H | ILSR | Input level select register | R/W | 00000000 _B |
| 0FEF _H | WICR | Interrupt pin control register | R/W | 01000000 _B |
| 0FF0 _H to 0FFF _H | — | (Disabled) | — | — |

• R/W access symbols

R/W : Readable / Writable

R : Read only

• Initial value symbols

0 : The initial value of this bit is "0".



1 : The initial value of this bit is "1".

X : The initial value of this bit is indeterminate.

Note: Do not write to an address that is "(Disabled)". If a "(Disabled)" address is read, an indeterminate value is returned.

MB95310L/370L Series

■ INTERRUPT SOURCE TABLE

| Interrupt source | Interrupt request number | Vector table address | | Bit name of interrupt level setting register | Priority order of interrupt sources of the same level (occurring simultaneously) |
|--|--------------------------|----------------------|-------------------|--|---|
| | | Upper | Lower | | |
| External interrupt ch. 0 | IRQ00 | FFFA _H | FFFB _H | L00 [1:0] | High   Low |
| External interrupt ch. 4 | | | | | |
| External interrupt ch. 1 | IRQ01 | FFF8 _H | FFF9 _H | L01 [1:0] | |
| External interrupt ch. 5 | | | | | |
| External interrupt ch. 2 | IRQ02 | FFF6 _H | FFF7 _H | L02 [1:0] | |
| External interrupt ch. 6 | | | | | |
| External interrupt ch. 3 | IRQ03 | FFF4 _H | FFF5 _H | L03 [1:0] | |
| External interrupt ch. 7 | | | | | |
| UART/SIO ch. 0 | IRQ04 | FFF2 _H | FFF3 _H | L04 [1:0] | |
| Low-voltage detection reset circuit | | | | | |
| 8/16-bit composite timer ch. 0 (lower) | IRQ05 | FFF0 _H | FFF1 _H | L05 [1:0] | |
| 8/16-bit composite timer ch. 0 (upper) | IRQ06 | FFEE _H | FFEF _H | L06 [1:0] | |
| — | IRQ07 | FFEC _H | FFED _H | L07 [1:0] | |
| — | IRQ08 | FFEA _H | FFEB _H | L08 [1:0] | |
| 8/16-bit PPG ch. 1 (lower) | IRQ09 | FFE8 _H | FFE9 _H | L09 [1:0] | |
| UART/SIO ch. 1 | | | | | |
| 8/16-bit PPG ch. 1 (upper) | IRQ10 | FFE6 _H | FFE7 _H | L10 [1:0] | |
| 16-bit reload timer ch. 0 | IRQ11 | FFE4 _H | FFE5 _H | L11 [1:0] | |
| 8/16-bit PPG ch. 0 (upper) | IRQ12 | FFE2 _H | FFE3 _H | L12 [1:0] | |
| 8/16-bit PPG ch. 0 (lower) | IRQ13 | FFE0 _H | FFE1 _H | L13 [1:0] | |
| 8/16-bit composite timer ch. 1 (upper) | IRQ14 | FFDE _H | FFDF _H | L14 [1:0] | |
| — | IRQ15 | FFDC _H | FFDD _H | L15 [1:0] | |
| I ² C | IRQ16 | FFDA _H | FFDB _H | L16 [1:0] | |
| — | IRQ17 | FFD8 _H | FFD9 _H | L17 [1:0] | |
| 8/10-bit A/D converter | IRQ18 | FFD6 _H | FFD7 _H | L18 [1:0] | |
| Time-base timer | IRQ19 | FFD4 _H | FFD5 _H | L19 [1:0] | |
| Watch prescaler | IRQ20 | FFD2 _H | FFD3 _H | L20 [1:0] | |
| Watch counter | | | | | |
| — | IRQ21 | FFD0 _H | FFD1 _H | L21 [1:0] | |
| 8/16-bit composite timer ch. 1 (lower) | IRQ22 | FFCE _H | FFCF _H | L22 [1:0] | |
| Flash memory | IRQ23 | FFCC _H | FFCD _H | L23 [1:0] | |

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
|--|----------------------|----------------|----------------|------|--|
| | | Min | Max | | |
| Power supply voltage*1 | V_{CC}, AV_{CC} | $V_{SS} - 0.3$ | $V_{SS} + 4.0$ | V | *2 |
| Power supply voltage for LCD | V0 to V3 | $V_{SS} - 0.3$ | $V_{SS} + 4.0$ | V | Products with LCD internal division resistance*3 |
| Input voltage*1 | V_i | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V | P23,P24*4 |
| | | $V_{SS} - 0.3$ | $V_{SS} + 4.0$ | V | Other than P23,P24*4 |
| Output voltage*1 | V_o | $V_{SS} - 0.3$ | $V_{SS} + 4.0$ | V | *4 |
| Maximum clamp current | I_{CLAMP} | -2.0 | +2.0 | mA | Applicable to specific pins ⁵ |
| Total maximum clamp current | $\Sigma I_{CLAMP} $ | — | 20 | mA | Applicable to specific pins ⁵ |
| “L” level maximum output current | I_{OL} | — | 15 | mA | Applicable to specific pins ⁵ |
| “L” level average current | I_{OLAV} | — | 4 | mA | Applicable to specific pins ⁵ Average output current = operating current × operating ratio (1 pin) |
| “L” level total maximum output current | ΣI_{OL} | — | 100 | mA | |
| “L” level total average output current | ΣI_{OLAV} | — | 50 | mA | Total average output current = operating current × operating ratio (Total number of pins) |
| “H” level maximum output current | I_{OH} | — | -15 | mA | Applicable to specific pins ⁵ |
| “H” level average current | I_{OHAV} | — | -4 | mA | Applicable to specific pins ⁵ Average output current = operating current × operating ratio (1 pin) |
| “H” level total maximum output current | ΣI_{OH} | — | -100 | mA | |
| “H” level total average output current | ΣI_{OHAV} | — | -50 | mA | Total average output current = operating current × operating ratio (Total number of pins) |
| Power consumption | P_d | — | 320 | mW | |
| Operating temperature | T_A | -40 | +85 | °C | |
| Storage temperature | T_{stg} | -55 | +150 | °C | |

*1: These parameters are based on the condition that V_{SS} is 0.0 V.

*2: Apply equal potential to V_{CC} and AV_{CC} .

*3: V0 to V3 should not exceed $V_{CC} + 0.3$ V.

*4: V_i and V_o must not exceed $V_{CC} + 0.3$ V. V_i must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_i rating.

(Continued)

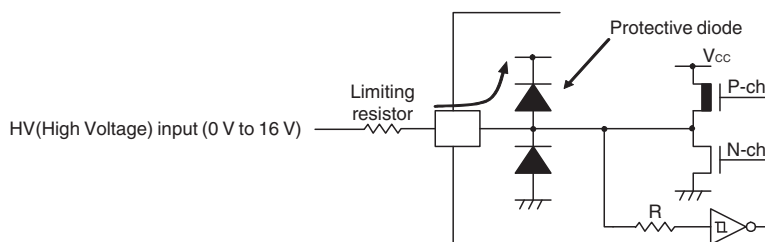
MB95310L/370L Series

(Continued)

*5: Applicable to the following pins: P00 to P07, P10, P11, P13 to P16, P20 to P22, P40 to P43, P50 to P53, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7, PE0 to PE7, PG0

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistance should be set so that when the HV (High Voltage) signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, and thus affects other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit

- Input/Output equivalent circuit



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

| Parameter | Symbol | Value | | Unit | Remarks | |
|-----------------------|---------------------------------------|-----------|-----|------|---|-------------------------------|
| | | Min | Max | | | |
| Power supply voltage | V _{CC} , AV _{CC} | 1.8*1*2*3 | 3.6 | V | In normal operation, T _A = -10°C to +85°C | Other than on-chip debug mode |
| | | 2.0 | 3.6 | | In normal operation, T _A = -40°C to +85°C | |
| | | 1.5 | 3.6 | | Hold condition in stop mode | |
| | | 3.10*3 | 3.6 | | T _A = +5°C to +35°C | On-chip debug mode |
| | | 1.5 | 3.6 | | Hold condition in stop mode | |
| Operating temperature | T _A | -40 | +85 | °C | Other than on-chip debug mode | |
| | | +5 | +35 | | On-chip debug mode | |

*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

*2: The value is initially 2.03 V when the low-voltage detection reset is used.

*3: The threshold voltage can be set to be 2.03 V, 2.55 V, 3.10 V by software.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

MB95310L/370L Series

3. DC Characteristics

($V_{CC} = 3.0 V \pm 10\%$, $V_{SS} = 0.0 V$, $T_A = -40^\circ C$ to $+85^\circ C$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|--------------------------|------------|--|---------------------------|----------------|------------------|----------------|------|---------------------------------|
| | | | | Min | Typ ⁵ | Max | | |
| "H" level input voltage | V_{IH1} | P10, P95 ¹ , PE6 ² | *3 | $0.7 V_{CC}$ | — | $V_{CC} + 0.3$ | V | When selecting CMOS input level |
| | V_{IH2} | P23, P24 | *3 | $0.7 V_{CC}$ | — | $V_{SS} + 5.5$ | V | |
| | V_{IHS1} | P00 to P07, P10 to P16, P20 to P22, P40 to P43 ¹ , P50 to P53 ¹ , P60 to P67, P90 to P92, P93 to P95 ¹ , PA0 to PA3, PB0 to PB7, PC0 to PC3, PC4 to PC7 ¹ , PE0 to PE7, PG0 ¹ | *3 | $0.8 V_{CC}$ | — | $V_{CC} + 0.3$ | V | Hysteresis input |
| | V_{IHS2} | P23, P24 | *3 | $0.8 V_{CC}$ | — | $V_{SS} + 5.5$ | V | |
| | V_{IHM} | \overline{RST} | — | $0.8 V_{CC}$ | — | $V_{CC} + 0.3$ | V | |
| "L" level input voltage | V_{IL} | P10, P23, P24, P95 ¹ , PE6 ² | *3 | $V_{SS} - 0.3$ | — | $0.3 V_{CC}$ | V | When selecting CMOS input level |
| | V_{ILS} | P00 to P07, P10 to P16, P20 to P24, P40 to P43 ¹ , P50 to P53 ¹ , P60 to P67, P90 to P92, P93 to P95 ¹ , PA0 to PA3, PB0 to PB7, PC0 to PC3, PC4 to PC7 ¹ , PE0 to PE7, PG0 ¹ | *3 | $V_{SS} - 0.3$ | — | $0.2 V_{CC}$ | V | Hysteresis input |
| | V_{ILM} | \overline{RST} | — | $V_{SS} - 0.3$ | — | $0.2 V_{CC}$ | V | |
| "H" level output voltage | V_{OH} | Output pin other than P12, P23, P24 | $I_{OH} = 4.0 \text{ mA}$ | $V_{CC} - 0.5$ | — | — | V | |
| "L" level output voltage | V_{OL} | Output pin other than \overline{RST} | $I_{OL} = 4.0 \text{ mA}$ | — | — | 0.4 | V | |

(Continued)

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($V_{CC} = 3.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|------------|---|---|-------|-------|------|------------------|--|
| | | | | Min | Typ*5 | Max | | |
| Input leakage current (Hi-Z output leakage current) | I_{LI} | Ports other than P12, P23, P24 | $0.0\text{ V} < V_I < V_{CC}$ | -5 | — | +5 | μA | When pull-up resistance is disabled |
| Open-drain output leakage voltage | I_{LIOD} | P12, P23, P24 | $0.0\text{ V} < V_I < V_{SS} + 5.5\text{ V}$ | — | — | 5 | μA | |
| Pull-up resistance | R_{PULL} | P00 to P03, P10, P11, P13 to P16, P20 to P22, P50 to P53*1, P94, P95*1, PG0*1 | $V_I = 0.0\text{ V}$ | 25 | 50 | 100 | $\text{k}\Omega$ | When pull-up resistance is enabled |
| Input capacitance | C_{IN} | Other than V_{CC} and V_{SS} | $f = 1\text{ MHz}$ | — | 5 | 15 | pF | |
| Power supply current*4 | I_{CC} | V_{CC} (External clock operation) | $F_{CH} = 32\text{ MHz}$ $F_{MP} = 16\text{ MHz}$ Main clock mode (divided by 2) | — | 16.5 | 27.7 | mA | Except during Flash memory programming and erasing |
| | | | $F_{CH} = 32\text{ MHz}$ $F_{MP} = 16\text{ MHz}$ Main sleep mode (divided by 2) | — | 38.1 | 44.9 | mA | During Flash memory programming and erasing |
| | I_{CCS} | | $F_{CH} = 32\text{ MHz}$ $F_{MP} = 16\text{ MHz}$ Main sleep mode (divided by 2) | — | 9 | 15.9 | mA | |
| | I_{CCL} | | $F_{CL} = 32\text{ kHz}$ $F_{MPL} = 16\text{ kHz}$ Subclock mode (divided by 2) $T_A = +25^\circ\text{C}$ | — | 22.6 | 37.9 | μA | |

(Continued)

MB95310L/370L Series

($V_{CC} = 3.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|------------------------|---------------------|---|--|-------|------------------|-------|------|---------|
| | | | | Min | Typ ⁵ | Max | | |
| Power supply current*4 | I _{CCLS} | V _{CC} (External clock operation) | F _{CL} = 32 kHz F _{MPL} = 16 kHz Subsleep mode (divided by 2) T _A = +25°C | — | 11.2 | 16.5 | μA | |
| | I _{CCCT} | | F _{CL} = 32 kHz Watch mode Main stop mode T _A = +25°C | — | 6.7 | 9 | μA | |
| | I _{CCMPLL} | | F _{CH} = 4 MHz F _{MP} = 10 MHz Main PLL mode (multiplied by 2.5) | — | 10.1 | 19.2 | mA | |
| | | | F _{CH} = 6.4 MHz F _{MP} = 16 MHz Main PLL mode (multiplied by 2.5) | — | 16.2 | 30.7 | mA | |
| | I _{CCMCR} | | F _{CRH} = 12.5 MHz F _{MP} = 12.5 MHz Main CR clock mode | — | 7.9 | 13.2 | mA | |
| | I _{CCSCR} | | Sub-CR clock mode (divided by 2) T _A = +25°C | — | 77.8 | 138.5 | μA | |
| | I _{CTS} | | F _{CH} = 32 MHz Time-base timer mode T _A = +25°C | — | 4.3 | 7.4 | mA | |
| | I _{CCH} | | Substop mode T _A = +25°C | — | 1 | 5 | μA | |
| | I _A | AV _{CC} | Current consumption for A/D conversion at 16 MHz | — | 0.8 | 1.9 | mA | |
| | I _{AH} | | Current consumption for stopping A/D conversion at 16 MHz | — | 1 | 5 | μA | |

(Continued)

MB95310L/370L Series

(Continued)

($V_{CC} = 3.0 \text{ V} \pm 10\%$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|----------------------------------|------------|--|--|-------|-------------------|-----|------------------|---------|
| | | | | Min | Typ ^{*5} | Max | | |
| Power supply current*4 | I_{LVD} | V_{CC} | Current consumption for the low-voltage detection reset circuit | — | 6 | 9.8 | μA | |
| | I_{CRH} | | Current consumption for the main CR oscillator | — | 0.5 | 0.6 | mA | |
| | I_{CRL} | | Current consumption for the sub-CR oscillator oscillating at 100 kHz | — | 20 | 72 | μA | |
| LCD internal division resistance | R_{LCD} | — | Between V_3 and V_{SS} | — | 300 | — | $\text{k}\Omega$ | |
| COM0 to COM3 output impedance | R_{VCOM} | COM0 to COM3 | V_1 to $V_3 = 3.6 \text{ V}$ | — | — | 5 | $\text{k}\Omega$ | |
| SEG00 to SEG39 output impedance | R_{VSEG} | SEG00 to SEG39 | | — | — | 7 | $\text{k}\Omega$ | |
| LCD leakage current | I_{LCDL} | V_0 to V_3 , COM0 to COM3, SEG00 to SEG39 | — | -1 | — | +1 | μA | |

*1: It is for MB95310L Series.

*2: It is for MB95370L Series.

*3: The input level can be switched between “CMOS input level” and “hysteresis input level”. The input level selection register (ILSR) is used to switch between the two input levels.

*4: • The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit (I_{LVD}) to one of the value from I_{CC} to I_{CCH} . In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators (I_{CRH} , I_{CRL}) and a specified value. In on-chip debug mode, the CR oscillator (I_{CRH}) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.

• See “4. AC Characteristics: (1) Clock Timing” for F_{CH} and F_{CL} .

• See “4. AC Characteristics: (2) Source Clock/Machine Clock” for F_{MP} and F_{MPL} .

*5: $V_{CC} = 3.0 \text{ V}$, $T_A = +25^\circ\text{C}$

MB95310L/370L Series

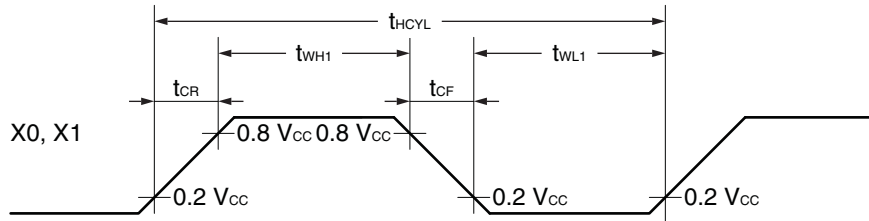
4. AC Characteristics

(1) Clock Timing

($V_{CC} = 3.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks | | |
|-------------------------------------|------------------------|----------|-----------|-------|--------|---------|---------------|--|---|-----|
| | | | | Min | Typ | Max | | | | |
| Clock frequency | F_{CH} | X0, X1 | — | 1.00 | — | 16.25 | MHz | When the main oscillation circuit is used | | |
| | | | | 1.00 | — | 32.50 | MHz | When the main external clock is used | | |
| | | | | 3.00 | — | 8.13 | MHz | Main PLL multiplied by 2 | | |
| | | | | 3.00 | — | 6.5 | MHz | Main PLL multiplied by 2.5 | | |
| | | | | 3.00 | — | 4.06 | MHz | Main PLL multiplied by 4 | | |
| | F_{CRH} | — | — | — | 12.25 | 12.5 | 12.75 | MHz | Operating conditions: • The main CR clock is used. • $T_A = -10^\circ\text{C}$ to $+85^\circ\text{C}$ | |
| | | | | | 9.8 | 10 | 10.2 | MHz | | |
| | | | | | 7.84 | 8 | 8.16 | MHz | | |
| | | | | | 0.98 | 1 | 1.02 | MHz | | |
| | | — | — | — | — | 12.1875 | 12.5 | 12.8125 | | MHz |
| | | | | | | 9.75 | 10 | 10.25 | | MHz |
| | | | | | | 7.8 | 8 | 8.2 | | MHz |
| | | | | | | 0.975 | 1 | 1.025 | | MHz |
| | F_{CL} | X0A, X1A | — | — | — | 32.768 | — | kHz | When the sub-oscillation circuit is used | |
| — | | | | | 32.768 | — | kHz | When the sub-external clock is used | | |
| 50 | | | | | 100 | 200 | kHz | When the sub-CR clock is used | | |
| Clock cycle time | t_{HCYL} | X0, X1 | — | 61.5 | — | 1000 | ns | When the main oscillation circuit is used | | |
| | | | | 30.8 | — | 1000 | ns | When the external clock is used | | |
| | t_{LCYL} | X0A, X1A | — | — | 30.5 | — | μs | When the subclock is used | | |
| Input clock pulse width | t_{WH1} t_{WL1} | X0 | — | 61.5 | — | — | ns | When using external clock and the duty ratio is about 30% to 70% | | |
| | t_{WH2} t_{WL2} | X0A | | — | 15.2 | — | μs | | | |
| Input clock rise time and fall time | t_{CR} t_{CF} | X0, X0A | X1: open | — | — | 5 | ns | When the external clock is used | | |
| CR oscillation start time | t_{CRHWK} | — | — | — | — | 150 | μs | When the main CR clock is used | | |
| | t_{CRLWK} | — | — | — | — | 10 | μs | When the sub-CR clock is used | | |

- Input waveform generated when an external clock (main clock) is used

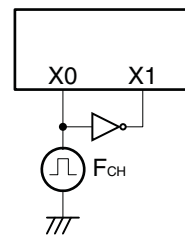
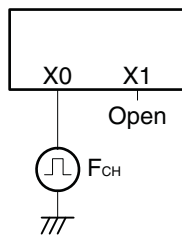
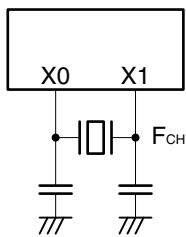


- Figure of main clock input port external connection

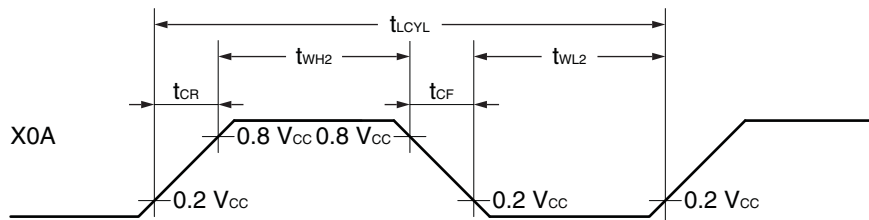
When a crystal oscillator or a ceramic oscillator is used

When the external clock is used (X1 is open)

When the external clock is used



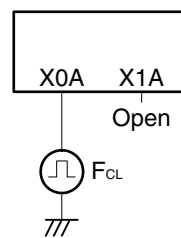
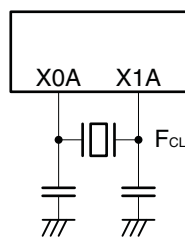
- Input waveform generated when an external clock (subclock) is used



- Figure of subclock input port external connection

When a crystal oscillator or a ceramic oscillator is used

When the external clock is used



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(2) Source Clock/Machine Clock

($V_{CC} = 3.0 V \pm 10\%$, $V_{SS} = 0.0 V$, $T_A = -40^\circ C$ to $+85^\circ C$)

| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|--|------------|------------|--------|------|--------|--|--|
| | | | Min | Typ | Max | | |
| Source clock cycle time*1 | t_{SCLK} | — | 61.5 | — | 2000 | ns | When the main oscillation clock is used Min: $F_{CH} = 8.125$ MHz, multiplied by the PLL multiplier of 2 Max: $F_{CH} = 1$ MHz, divided by 2 |
| | | | 80 | — | 1000 | ns | When the main CR clock is used Min: $F_{CRH} = 12.5$ MHz Max: $F_{CRH} = 1$ MHz |
| | | | — | 61 | — | μs | When the sub-oscillation clock is used $F_{CL} = 32.768$ kHz, divided by 2 |
| | | | — | 20 | — | μs | When the sub-CR clock is used $F_{CRL} = 100$ kHz, divided by 2 |
| Source clock frequency | F_{SP} | — | 0.50 | — | 16.25 | MHz | When the main oscillation clock is used |
| | | | 1 | — | 12.5 | MHz | When the main CR clock is used |
| | — | | 16.384 | — | kHz | When the sub-oscillation clock is used | |
| | F_{SPL} | | — | 50 | — | kHz | When the sub-CR clock is used $F_{CRL} = 100$ kHz, divided by 2 |
| Machine clock cycle time*2 (minimum instruction execution time) | | t_{MCLK} | — | 61.5 | — | 32000 | ns |
| | 80 | | | — | 16000 | ns | When the main CR clock is used Min: $F_{SP} = 12.5$ MHz Max: $F_{SP} = 1$ MHz, divided by 16 |
| | 61 | | | — | 976.5 | μs | When the sub-oscillation clock is used Min: $F_{SPL} = 16.393$ kHz, no division Max: $F_{SPL} = 16.393$ kHz, divided by 16 |
| | 20 | | | — | 320 | μs | When the sub-CR clock is used Min: $F_{SPL} = 50$ kHz, no division Max: $F_{SPL} = 50$ kHz, divided by 16 |
| Machine clock frequency | F_{MP} | — | 0.031 | — | 16.25 | MHz | When the main oscillation clock is used |
| | | | 0.0625 | — | 12.5 | MHz | When the main CR clock is used |
| | F_{MPL} | | 1.024 | — | 16.384 | kHz | When the sub-oscillation clock is used |
| | | | 3.125 | — | 50 | kHz | When the sub-CR clock is used $F_{CRL} = 100$ kHz |

*1: This is the clock before it is divided according to the division ratio set by the machine clock divide ratio select bits (SYCC:DIV1 and DIV0). This source clock is divided to become a machine clock according to the division ratio set by the machine clock divide ratio select bits (SYCC:DIV1 and DIV0). In addition, a source clock can be selected from the following.

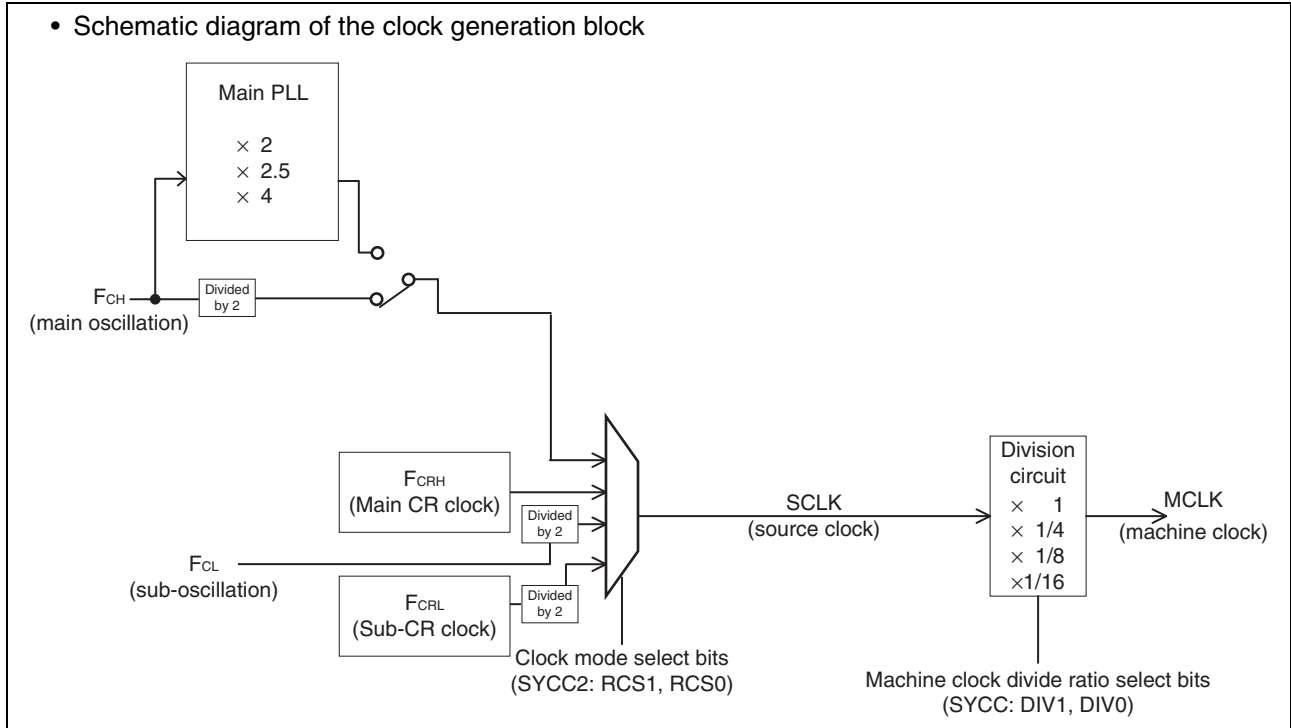
- Main clock divided by 2
- PLL multiplication of main clock (select from 2, 2.5, 4 multiplication)
- Main CR clock divided by 2
- Subclock divided by 2
- Sub-CR clock divided by 2

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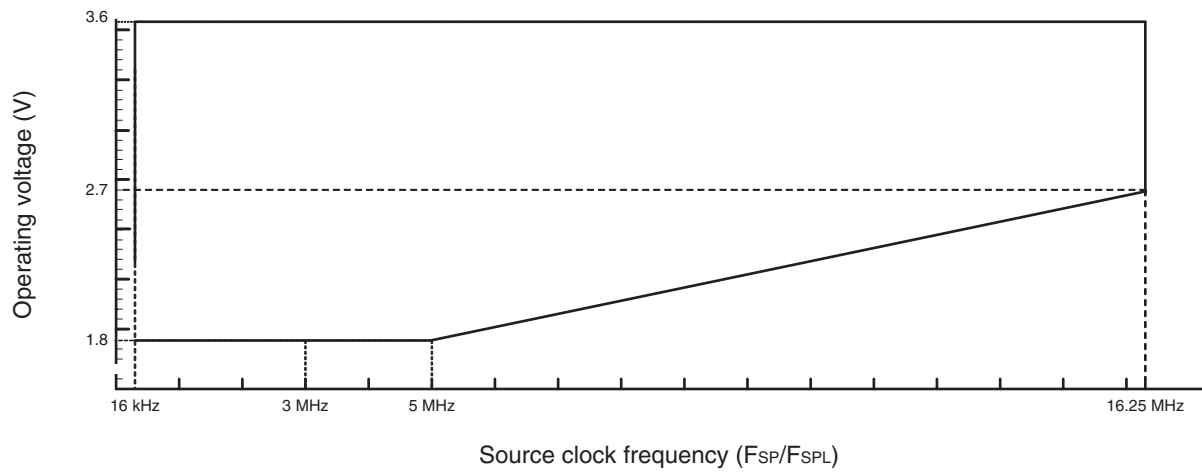
*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

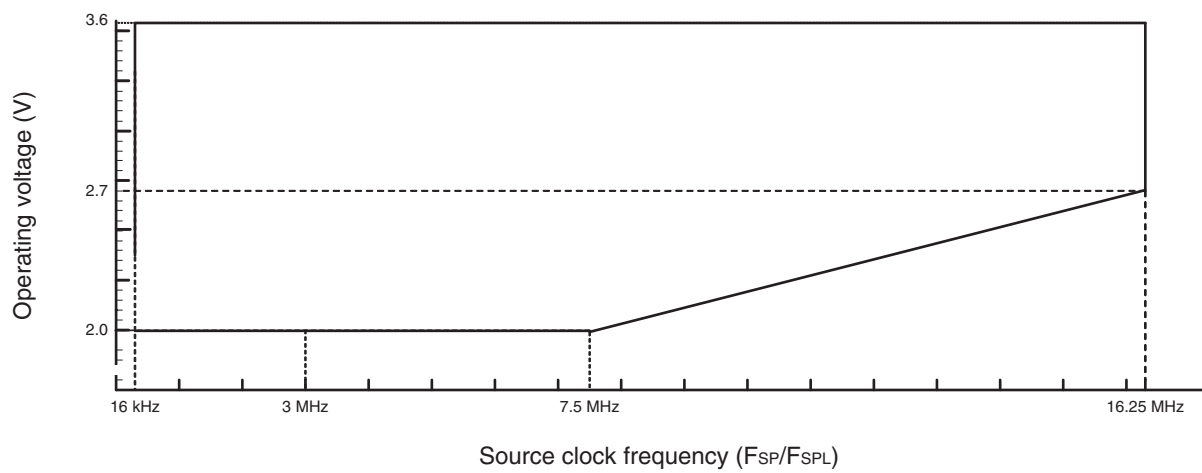


MB95310L/370L Series

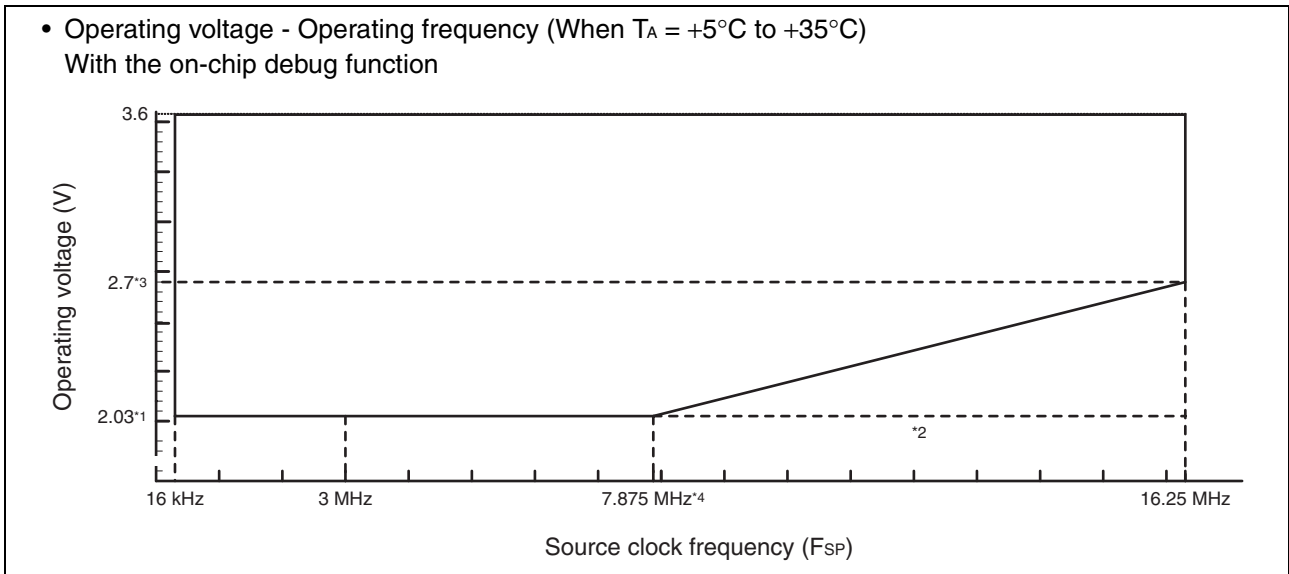
- Operating voltage - Operating frequency (When $T_A = -10^\circ\text{C}$ to $+85^\circ\text{C}$)
Without the on-chip debug function



- Operating voltage - Operating frequency (When $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)
Without the on-chip debug function



- Operating voltage - Operating frequency (When $T_A = +5^\circ\text{C}$ to $+35^\circ\text{C}$)
With the on-chip debug function



*1: This is the default LVD reset clear threshold: $1.93\text{ V} \pm 0.10\text{ V}$. It can also be set to $2.40\text{ V} \pm 0.15\text{ V}$ or $2.95\text{ V} \pm 0.15\text{ V}$.

*2: If the LVD reset clear threshold is set to $2.95\text{ V} \pm 0.15\text{ V}$, the slope from 10 MHz to 16.25 MHz should be a horizontal line.

*3: The operating voltage becomes 3.1 V if the LVD reset clear threshold is set to $2.95\text{ V} \pm 0.15\text{ V}$.

*4: The source clock frequency becomes 14.375 MHz if the LVD reset clear threshold is set to $2.40\text{ V} \pm 0.15\text{ V}$.

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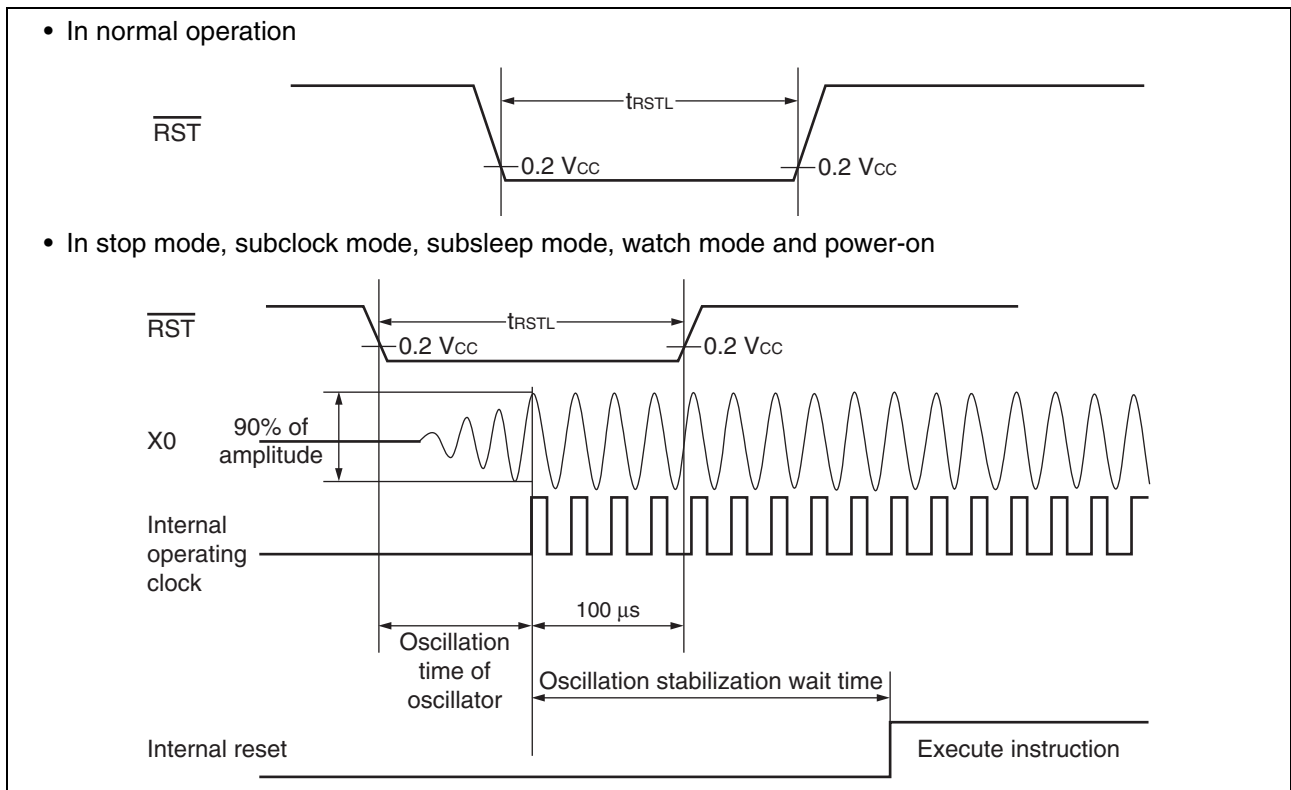
(3) External Reset

($V_{CC} = 3.0 V \pm 10\%$, $V_{SS} = 0.0 V$, $T_A = -40^\circ C$ to $+85^\circ C$)

| Parameter | Symbol | Value | | Unit | Remarks |
|--|------------|--|-----|---------|--|
| | | Min | Max | | |
| \overline{RST} "L" level pulse width | t_{RSTL} | $2 t_{MCLK}^{*1}$ | — | ns | In normal operation |
| | | Oscillation time of the oscillator ^{*2} + 100 | — | μs | In stop mode, subclock mode, subsleep mode, watch mode, and power-on |
| | | 100 | — | μs | In time-base timer mode |

*1: See "(2) Source Clock/Machine Clock" for t_{MCLK} .

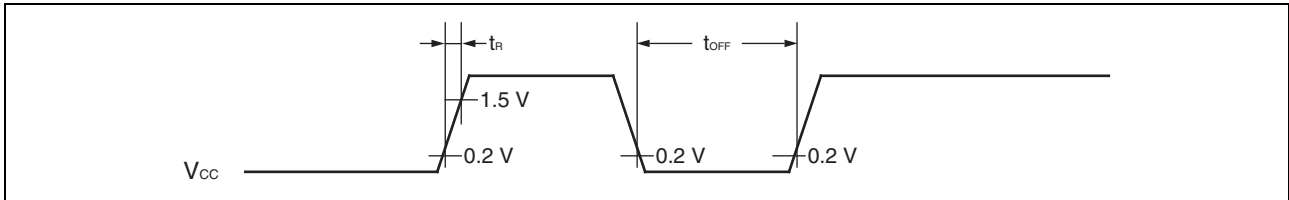
*2: The oscillation time of an oscillator is the time for it to reach 90% of its amplitude. The crystal oscillator has an oscillation time of between several ms and tens of ms. The ceramic oscillator has an oscillation time of between hundreds of μs and several ms. The external clock has an oscillation time of 0 ms. The CR oscillator clock has an oscillation time of between several μs and several ms.



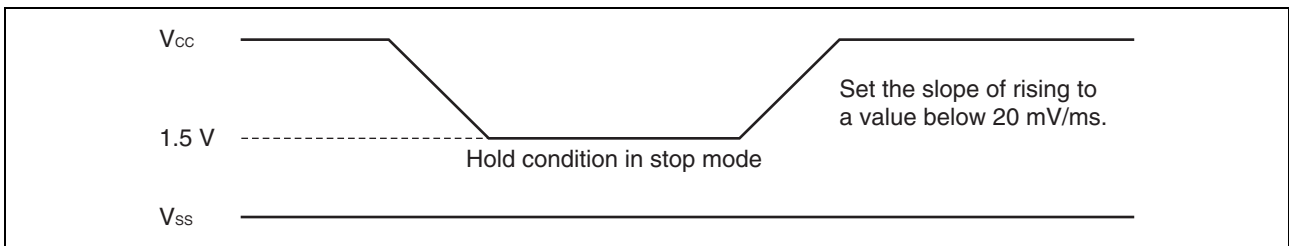
(4) Power-on Reset

($V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|--------------------------|-----------|-----------|-------|-----|------|--------------------------|
| | | | Min | Max | | |
| Power supply rising time | t_R | — | — | 50 | ms | |
| Power supply cutoff time | t_{OFF} | — | 1 | — | ms | Wait time until power-on |



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 20 mV/ms as shown below.



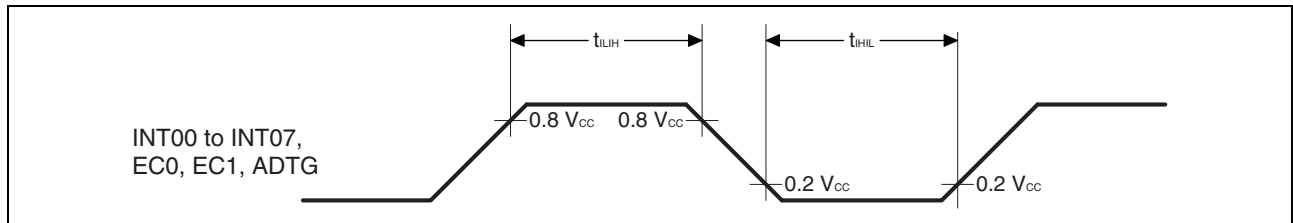
MB95310L/370L Series

(5) Peripheral Input Timing

($V_{CC} = 3.0 V \pm 10\%$, $V_{SS} = 0.0 V$, $T_A = -40^\circ C$ to $+85^\circ C$)

| Parameter | Symbol | Pin name | Value | | Unit |
|----------------------------------|----------|---------------------------|----------------|-----|------|
| | | | Min | Max | |
| Peripheral input "H" pulse width | t_{LH} | INT00 to INT07, EC0, EC1, | $2 t_{MCLK}^*$ | — | ns |
| Peripheral input "L" pulse width | t_{HL} | ADTG | $2 t_{MCLK}^*$ | — | ns |

*: See "(2) Source Clock/Machine Clock" for t_{MCLK} .

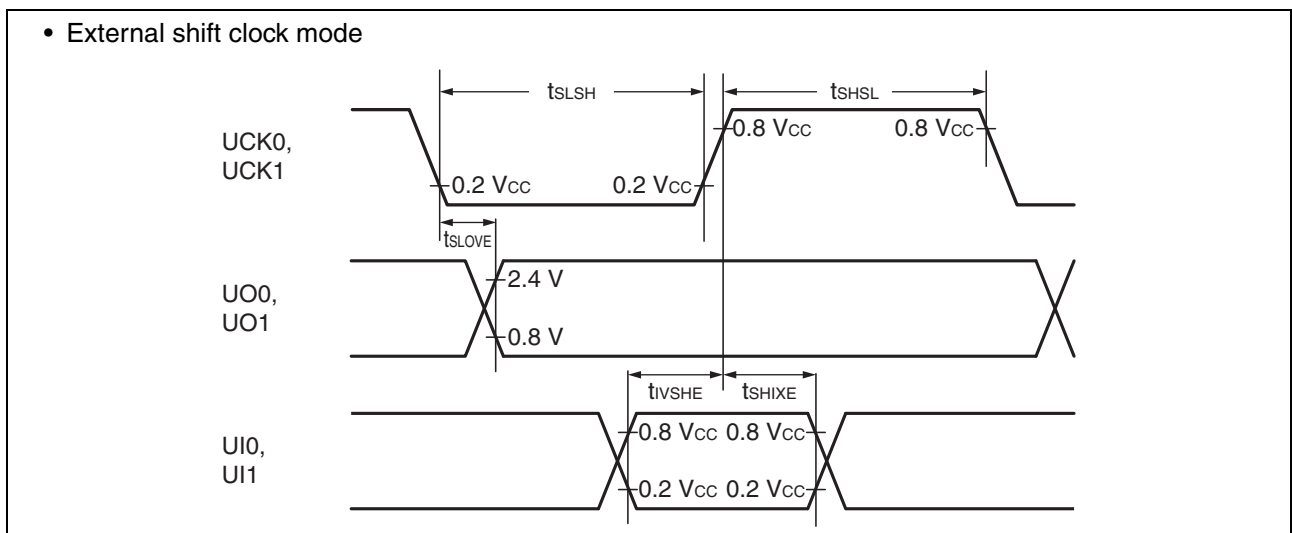
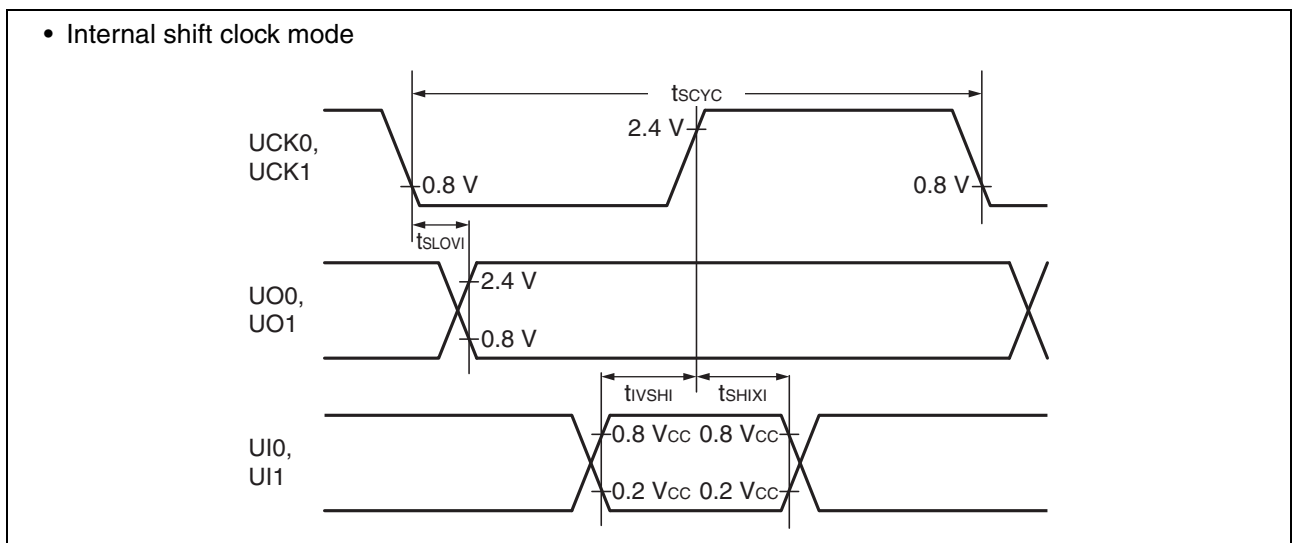


(6) UART/SIO, Serial I/O Timing

($V_{CC} = 3.0 V \pm 10\%$, $AV_{SS} = V_{SS} = 0.0 V$, $T_A = -40^\circ C$ to $+85^\circ C$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|------------------------------|-------------|-------------------------|--|----------------|------|------|
| | | | | Min | Max | |
| Serial clock cycle time | t_{SCYC} | UCK0, UCK1 | Internal clock operation output pin: $C_L = 80 \text{ pF} + 1 \text{ TTL}$ | $4 t_{MCLK}^*$ | — | ns |
| UCK ↓ → UO time | t_{SLOVI} | UCK0, UCK1, UO0, UO1 | | -190 | +190 | ns |
| Valid UI → UCK ↑ | t_{IVSHI} | UCK0, UCK1, UI0, UI1 | | $2 t_{MCLK}^*$ | — | ns |
| UCK ↑ → valid UI hold time | t_{SHIXI} | UCK0, UCK1, UI0, UI1 | | $2 t_{MCLK}^*$ | — | ns |
| Serial clock "H" pulse width | t_{SHSL} | UCK0, UCK1 | External clock operation output pin: $C_L = 80 \text{ pF} + 1 \text{ TTL}$ | $4 t_{MCLK}^*$ | — | ns |
| Serial clock "L" pulse width | t_{SLSH} | UCK0, UCK1 | | $4 t_{MCLK}^*$ | — | ns |
| UCK ↓ → UO time | t_{SLOVE} | UCK0, UCK1, UO0, UO1 | | — | 190 | ns |
| Valid UI → UCK ↑ | t_{IVSHE} | UCK0, UCK1, UI0, UI1 | | $2 t_{MCLK}^*$ | — | ns |
| UCK ↑ → valid UI hold time | t_{SHIXE} | UCK0, UCK1, UI0, UI1 | | $2 t_{MCLK}^*$ | — | ns |

*: See "(2) Source Clock/Machine Clock" for t_{MCLK} .



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(7) Low-voltage Detection

($V_{SS} = 0.0\text{ V}$, $V_{CC} = 1.8\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|-------------|-------|------|------|---------------|---|
| | | Min | Typ | Max | | |
| Power release voltage 0 | V_{PDL0+} | 1.83 | 1.93 | 2.03 | V | At power supply rise |
| Power detection voltage 0 | V_{PDL0-} | 1.80 | 1.90 | 2.00 | V | At power supply fall |
| Power release voltage 1 | V_{PDL1+} | 2.25 | 2.40 | 2.55 | V | At power supply rise |
| Power detection voltage 1 | V_{PDL1-} | 2.20 | 2.35 | 2.50 | V | At power supply fall |
| Power release voltage 2 | V_{PDL2+} | 2.80 | 2.95 | 3.10 | V | At power supply rise |
| Power detection voltage 2 | V_{PDL2-} | 2.70 | 2.85 | 3.00 | V | At power supply fall |
| Interrupt release voltage 0 | V_{IDL0+} | 2.03 | 2.18 | 2.33 | V | At power supply rise |
| Interrupt detection voltage 0 | V_{IDL0-} | 2.00 | 2.15 | 2.30 | V | At power supply fall |
| Interrupt release voltage 1 | V_{IDL1+} | 2.25 | 2.40 | 2.55 | V | At power supply rise |
| Interrupt detection voltage 1 | V_{IDL1-} | 2.20 | 2.35 | 2.50 | V | At power supply fall |
| Interrupt release voltage 2 | V_{IDL2+} | 2.46 | 2.61 | 2.76 | V | At power supply rise |
| Interrupt detection voltage 2 | V_{IDL2-} | 2.40 | 2.55 | 2.70 | V | At power supply fall |
| Interrupt release voltage 3 | V_{IDL3+} | 2.67 | 2.82 | 2.97 | V | At power supply rise |
| Interrupt detection voltage 3 | V_{IDL3-} | 2.60 | 2.75 | 2.90 | V | At power supply fall |
| Interrupt release voltage 4 | V_{IDL4+} | 2.90 | 3.10 | 3.30 | V | At power supply rise |
| Interrupt detection voltage 4 | V_{IDL4-} | 2.80 | 3.00 | 3.20 | V | At power supply fall |
| Power supply start voltage | V_{off} | — | — | 1.8 | V | |
| Power supply end voltage | V_{on} | 3.3 | — | — | V | |
| Power supply voltage change time (at power supply rise) | t_r | 3000 | — | — | μs | Slope of power supply that the reset release signal generates within the rating (V_{PDL+}/V_{IDL+}) |
| Power supply voltage change time (at power supply fall) | t_f | 3000 | — | — | μs | Slope of power supply that the reset detection signal generates within the rating (V_{PDL-}/V_{IDL-}) |

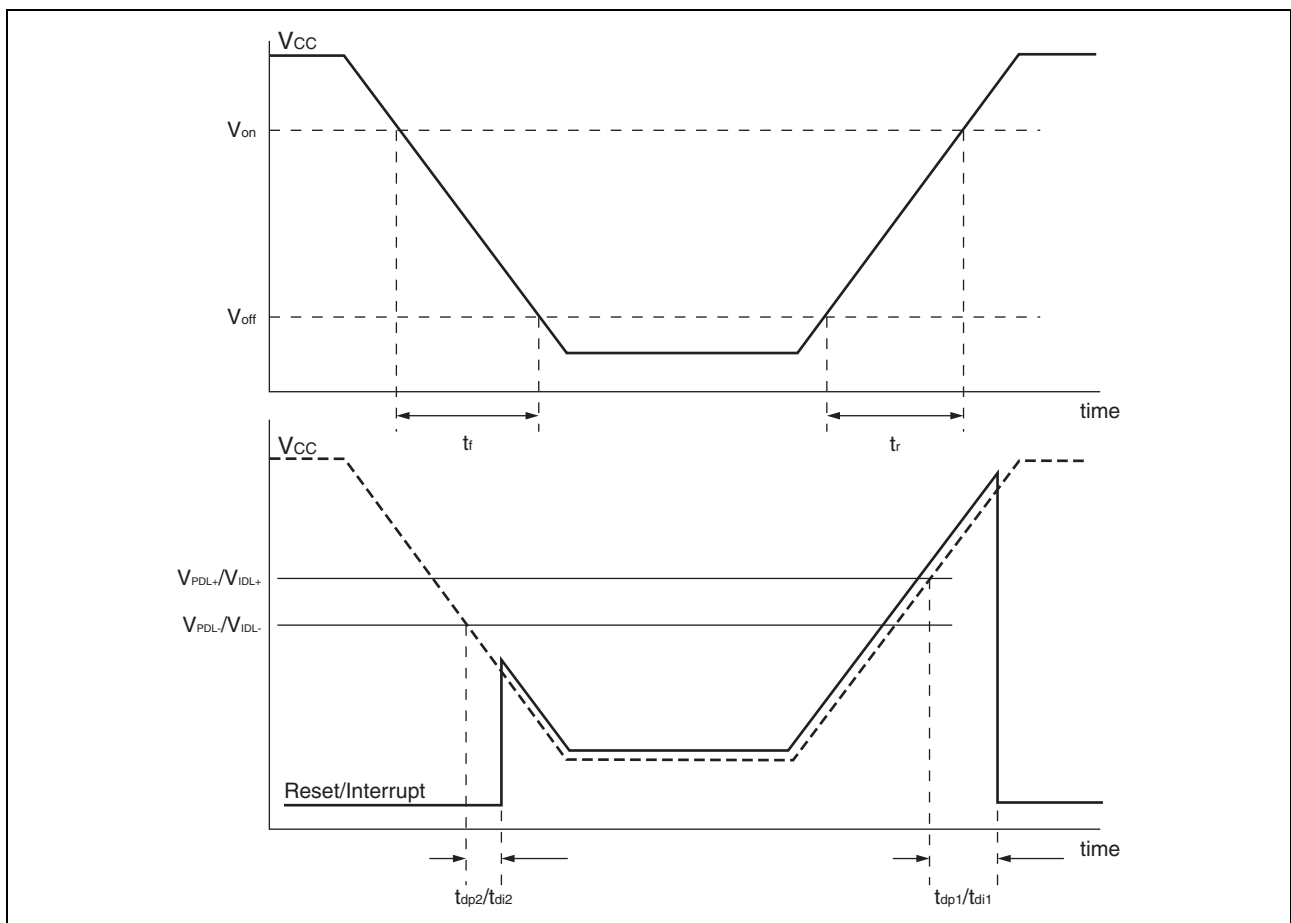
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MB95310L/370L Series

(Continued)

($V_{SS} = 0.0\text{ V}$, $V_{CC} = 1.8\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)

| Parameter | Symbol | Value | | | Unit | Remarks |
|--------------------------------------|-----------|-------|-----|-----|---------------|---------|
| | | Min | Typ | Max | | |
| Power reset release delay time | t_{dp1} | 10 | — | 300 | μs | |
| Power reset detection delay time | t_{dp2} | — | — | 150 | μs | |
| Interrupt reset release delay time | t_{di1} | 10 | — | 200 | μs | |
| Interrupt reset detection delay time | t_{di2} | — | — | 150 | μs | |



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(8) I²C Timing

(V_{CC} = 3.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = -40°C to +85°C)

| Parameter | Symbol | Pin name | Conditions | Value | | | | Unit |
|--|---------------------|---------------|----------------------------|---------------|--------|-----------|-------|------|
| | | | | Standard-mode | | Fast-mode | | |
| | | | | Min | Max | Min | Max | |
| SCL clock frequency | f _{SCL} | SCL0 | R = 1.7 kΩ, C = 50 pF*1 | 0 | 100 | 0 | 400 | kHz |
| (Repeat) Start condition hold time SDA ↓ → SCL ↓ | t _{HD,STA} | SCL0, SDA0 | | 4.0 | — | 0.6 | — | μs |
| SCL clock "L" width | t _{LOW} | SCL0 | | 4.7 | — | 1.3 | — | μs |
| SCL clock "H" width | t _{HIGH} | SCL0 | | 4.0 | — | 0.6 | — | μs |
| (Repeat) Start condition setup time SCL ↑ → SDA ↓ | t _{SU,STA} | SCL0, SDA0 | | 4.7 | — | 0.6 | — | μs |
| Data hold time SCL ↓ → SDA ↓ ↑ | t _{HD,DAT} | SCL0, SDA0 | | 0 | 3.45*2 | 0 | 0.9*3 | μs |
| Data setup time SDA ↓ ↑ → SCL ↑ | t _{SU,DAT} | SCL0, SDA0 | | 0.25 | — | 0.1 | — | μs |
| Stop condition setup time SCL ↑ → SDA ↑ | t _{SU,STO} | SCL0, SDA0 | | 4.0 | — | 0.6 | — | μs |
| Bus free time between stop condition and start condition | t _{BUF} | SCL0, SDA0 | | 4.7 | — | 1.3 | — | μs |

*1: R represents the pull-up resistor of the SCL0 and SDA0 lines, and C the load capacitor of the SCL0 and SDA0 lines.

*2: The maximum t_{HD,DAT} in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at "L" (t_{LOW}) does not extend.

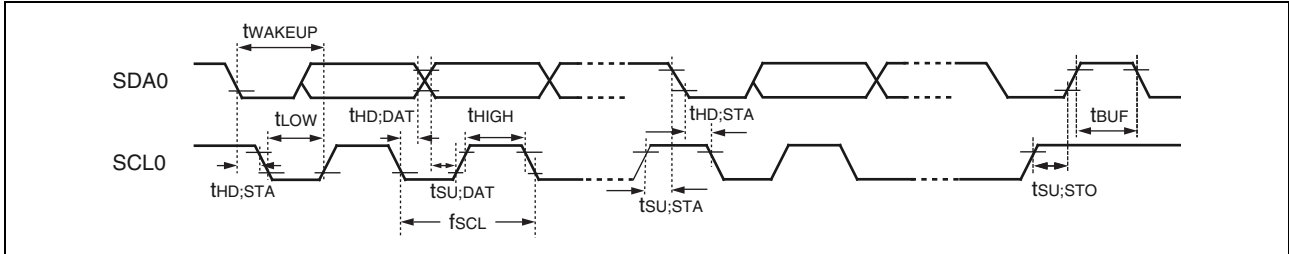
*3: A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, provided that the condition of t_{SU,DAT} ≥ 250 ns is fulfilled.

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Note: The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.

Be sure to adjust the pull-up resistor of SDA0 and SCL0 if the rating of the input data set-up time cannot be satisfied.



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($V_{CC} = 3.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Pin name | Conditions | Value*2 | | Unit | Remarks |
|--|--------------|------------|-------------------------------------|-------------------------------|------------------------------|------|--|
| | | | | Min | Max | | |
| SCL clock "L" width | t_{LOW} | SCL0 | R = 1.7 k Ω , C = 50 pF*1 | $(2 + nm / 2) t_{MCLK} - 20$ | — | ns | Master mode |
| SCL clock "H" width | t_{HIGH} | SCL0 | | $(nm / 2)t_{MCLK} - 20$ | $(nm / 2)t_{MCLK} + 20$ | ns | Master mode |
| Start condition hold time | $t_{HD,STA}$ | SCL0, SDA0 | | $(-1 + nm / 2) t_{MCLK} - 20$ | $(-1 + nm)t_{MCLK} + 20$ | ns | Master mode Maximum value is applied when $m, n = 1, 8$. Otherwise, the minimum value is applied. |
| Stop condition setup time | $t_{SU,STO}$ | SCL0, SDA0 | | $(1 + nm / 2) t_{MCLK} - 20$ | $(1 + nm / 2)t_{MCLK} + 20$ | ns | Master mode |
| Start condition setup time | $t_{SU,STA}$ | SCL0, SDA0 | | $(1 + nm / 2)t_{MCLK} - 20$ | $(1 + nm / 2)t_{MCLK} + 20$ | ns | Master mode |
| Bus free time between stop condition and start condition | t_{BUF} | SCL0, SDA0 | | $(2 nm + 4)t_{MCLK} - 20$ | — | ns | |
| Data hold time | $t_{HD,DAT}$ | SCL0, SDA0 | | $3 t_{MCLK} - 20$ | — | ns | Master mode |
| Data setup time | $t_{SU,DAT}$ | SCL0, SDA0 | | $(-2 + nm / 2)t_{MCLK} - 20$ | $(-1 + nm / 2)t_{MCLK} + 20$ | ns | Master mode When assuming that "L" of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied. |

(Continued)

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($V_{CC} = 3.0 V \pm 10\%$, $AV_{SS} = V_{SS} = 0.0 V$, $T_A = -40^\circ C$ to $+85^\circ C$)

| Parameter | Symbol | Pin name | Conditions | Value*2 | | Unit | Remarks |
|--|--------------|---------------|-------------------------------------|---|-----------------------------|------|---|
| | | | | Min | Max | | |
| Setup time between clearing interrupt and SCL rising | $t_{SU,INT}$ | SCL0 | R = 1.7 k Ω , C = 50 pF*1 | $(nm / 2)t_{MCLK} - 20$ | $(1 + nm / 2)t_{MCLK} + 20$ | ns | Minimum value is applied to interrupt at 9th SCL \downarrow . Maximum value is applied to interrupt at 8th SCL \downarrow . |
| SCL clock "L" width | t_{LOW} | SCL0 | | $4 t_{MCLK} - 20$ | — | ns | At reception |
| SCL clock "H" width | t_{HIGH} | SCL0 | | $4 t_{MCLK} - 20$ | — | ns | At reception |
| Start condition detection | $t_{HD,STA}$ | SCL0, SDA0 | | $2 t_{MCLK} - 20$ | — | ns | Not detected when 1 t_{MCLK} is used at reception |
| Stop condition detection | $t_{SU,STO}$ | SCL0, SDA0 | | $2 t_{MCLK} - 20$ | — | ns | Not detected when 1 t_{MCLK} is used at reception |
| Restart condition detection condition | $t_{SU,STA}$ | SCL0, SDA0 | | $2 t_{MCLK} - 20$ | — | ns | Not detected when 1 t_{MCLK} is used at reception |
| Bus free time | t_{BUF} | SCL0, SDA0 | | $2 t_{MCLK} - 20$ | — | ns | At reception |
| Data hold time | $t_{HD,DAT}$ | SCL0, SDA0 | | $2 t_{MCLK} - 20$ | — | ns | At slave transmission mode |
| Data setup time | $t_{SU,DAT}$ | SCL0, SDA0 | | $t_{LOW} - 3 t_{MCLK} - 20$ | — | ns | At slave transmission mode |
| Data hold time | $t_{HD,DAT}$ | SCL0, SDA0 | | 0 | — | ns | At reception |
| Data setup time | $t_{SU,DAT}$ | SCL0, SDA0 | | $t_{MCLK} - 20$ | — | ns | At reception |
| SDA $\downarrow \rightarrow$ SCL \uparrow (at wakeup function) | t_{WAKEUP} | SCL0, SDA0 | | Oscillation stabilization wait time + $2 t_{MCLK} - 20$ | — | ns | |

(Continued)

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(Continued)

*1: R represents the pull-up resistor of the SCL0 and SDA0 lines, and C the load capacitor of the SCL0 and SDA0 lines.

*2: • See “(2) Source Clock/Machine Clock” for t_{MCLK} .

- m represents the CS4 bit and CS3 bit (bit4 and bit3) in the I²C clock control register (ICCR0).
- n represents the CS2 bit to CS0 bit (bit2 to bit0) in the I²C clock control register (ICCR0).
- The actual timing of I²C is determined by the values of m and n set by the machine clock (t_{MCLK}) and the CS4 to CS0 bits in the ICCR0 register.

• Standard-mode:

m and n can be set to values in the following range: $0.9 \text{ MHz} < t_{MCLK} \text{ (machine clock)} < 16.25 \text{ MHz}$.

The usable frequencies of the machine clock are determined by the settings of m and n as shown below.

| | |
|--|---|
| (m, n) = (1, 8) | : $0.9 \text{ MHz} < t_{MCLK} \leq 1 \text{ MHz}$ |
| (m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4) | : $0.9 \text{ MHz} < t_{MCLK} \leq 2 \text{ MHz}$ |
| (m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8) | : $0.9 \text{ MHz} < t_{MCLK} \leq 4 \text{ MHz}$ |
| (m, n) = (1, 98), (5, 22), (6, 22), (7, 22) | : $0.9 \text{ MHz} < t_{MCLK} \leq 10 \text{ MHz}$ |
| (m, n) = (8, 22) | : $0.9 \text{ MHz} < t_{MCLK} \leq 16.25 \text{ MHz}$ |

• Fast-mode:

m and n can be set to values in the following range: $3.3 \text{ MHz} < t_{MCLK} \text{ (machine clock)} < 16.25 \text{ MHz}$.

The usable frequencies of the machine clock are determined by the settings of m and n as shown below.

| | |
|--|---|
| (m, n) = (1, 8) | : $3.3 \text{ MHz} < t_{MCLK} \leq 4 \text{ MHz}$ |
| (m, n) = (1, 22), (5, 4) | : $3.3 \text{ MHz} < t_{MCLK} \leq 8 \text{ MHz}$ |
| (m, n) = (1, 38), (6, 4), (7, 4), (8, 4) | : $3.3 \text{ MHz} < t_{MCLK} \leq 10 \text{ MHz}$ |
| (m, n) = (5, 8) | : $3.3 \text{ MHz} < t_{MCLK} \leq 16.25 \text{ MHz}$ |

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5. A/D Converter

(1) A/D Converter Electrical Characteristics

($V_{CC} = 1.8\text{ V to }3.6\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)

| Parameter | Symbol | Value | | | Unit | Remarks |
|-------------------------------|-----------|----------------------------|----------------------------|----------------------------|---------------|---|
| | | Min | Typ | Max | | |
| Resolution | — | — | — | 10 | bit | |
| Total error | | -3 | — | +3 | LSB | |
| Linearity error | | -2.5 | — | +2.5 | LSB | |
| Differential linear error | | -1.9 | — | +1.9 | LSB | |
| Zero transition voltage | V_{OT} | $AV_{SS} - 1.5\text{ LSB}$ | $AV_{SS} + 0.5\text{ LSB}$ | $AV_{SS} + 2.5\text{ LSB}$ | V | $2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ |
| | | $AV_{SS} - 0.5\text{ LSB}$ | $AV_{SS} + 1.5\text{ LSB}$ | $AV_{SS} + 3.5\text{ LSB}$ | V | $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$ |
| Full-scale transition voltage | V_{FST} | $AV_{CC} - 3.5\text{ LSB}$ | $AV_{CC} - 1.5\text{ LSB}$ | $AV_{CC} + 0.5\text{ LSB}$ | V | $2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ |
| | | $AV_{CC} - 2.5\text{ LSB}$ | $AV_{CC} - 0.5\text{ LSB}$ | $AV_{CC} + 1.5\text{ LSB}$ | V | $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$ |
| Compare time | — | 0.6 | — | 140 | μs | $2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ |
| | | 20 | — | 140 | μs | $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$ |
| Sampling time | — | 0.4 | — | ∞ | μs | $2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$, with external impedance $< 1.8\text{ k}\Omega$ |
| | | 30 | — | ∞ | μs | $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$, with external impedance $< 14.8\text{ k}\Omega$ |
| Analog input current | I_{AIN} | -0.3 | — | +0.3 | μA | |
| Analog input voltage | V_{AIN} | AV_{SS} | — | AV_{CC} | V | |

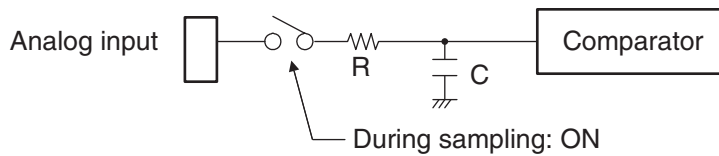
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(2) Notes on Using the A/D Converter

• External impedance of analog input and its sampling time

- The A/D converter has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 μF to the analog input pin.

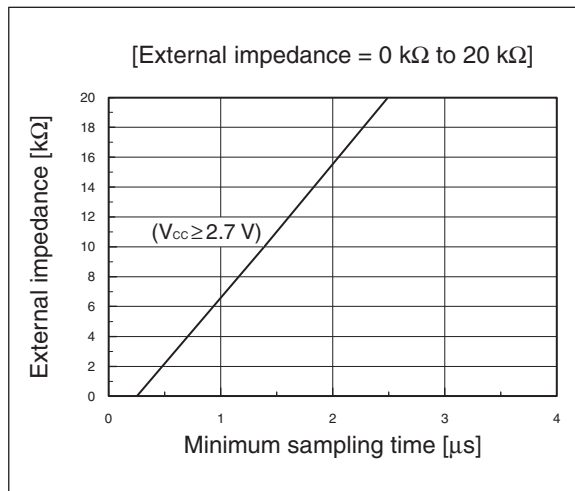
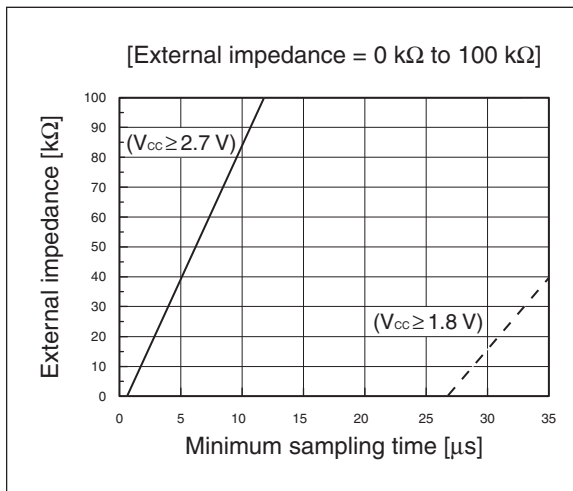
• Analog input equivalent circuit



| V_{CC} | R | C |
|--|----------------------|---------------|
| $2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ | 1.7 k Ω (Max) | 14.5 pF (Max) |
| $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$ | 8.4 k Ω (Max) | 25.2 pF (Max) |

Note: The values are reference values.

• Relationship between external impedance and minimum sampling time

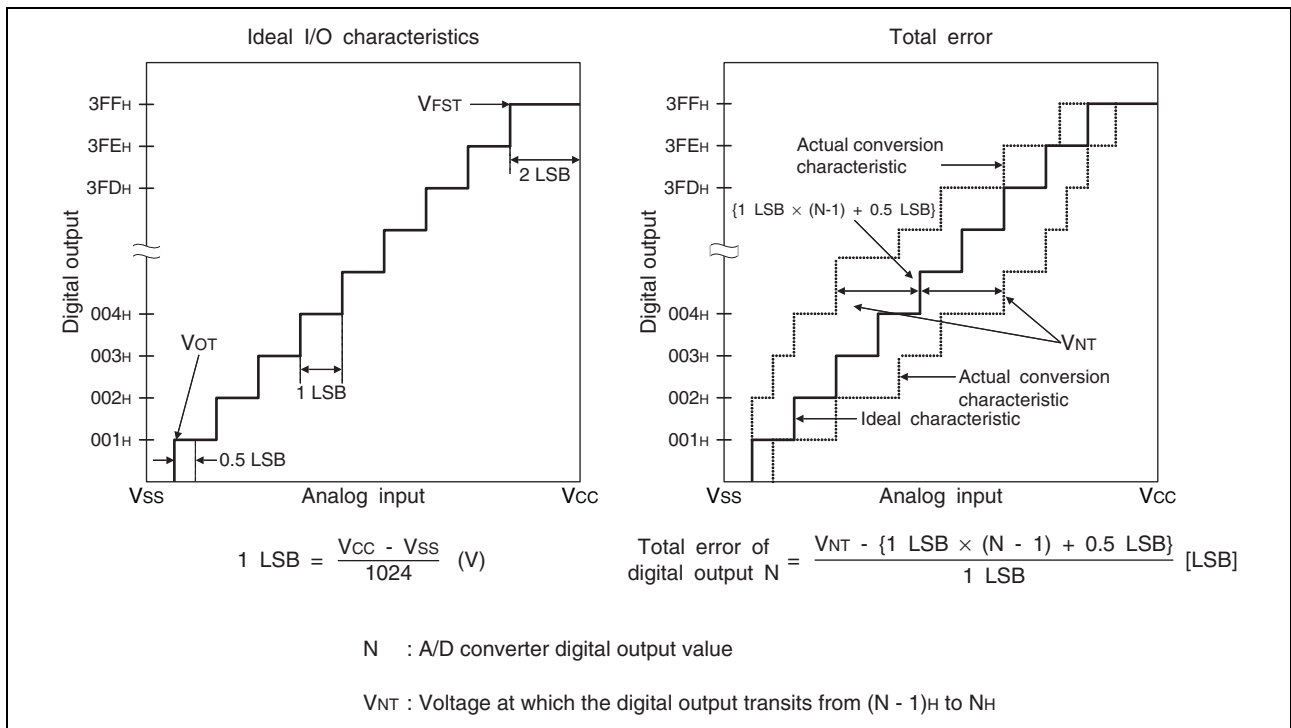


• A/D conversion error

As $V_{CC} - V_{SS}$ decreases, the A/D conversion error increases proportionately.

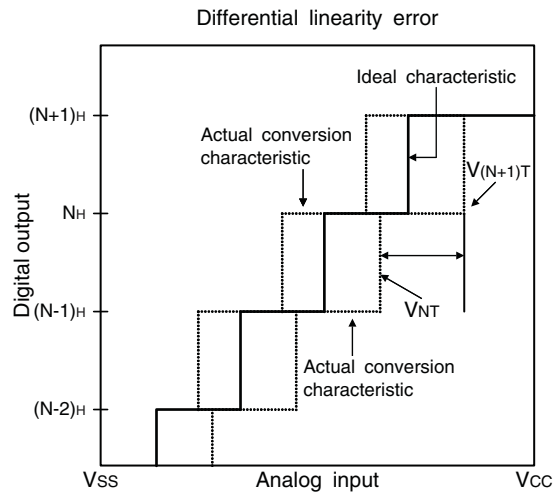
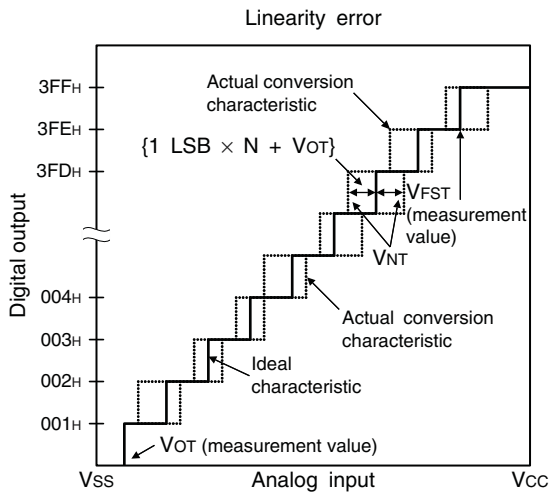
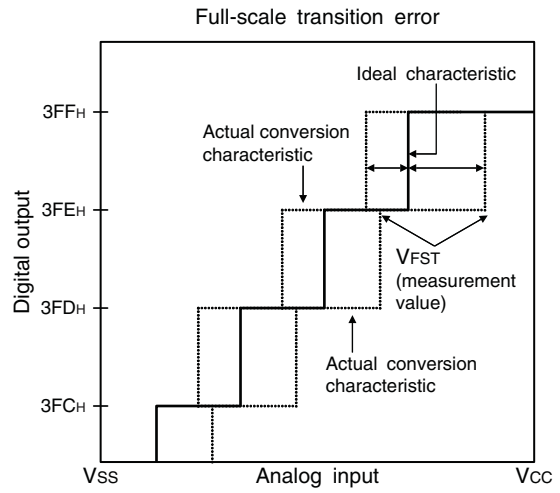
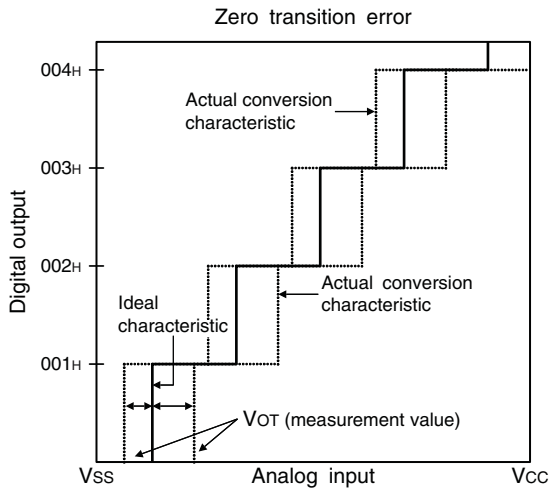
(3) Definitions of A/D Converter Terms

- Resolution
It indicates the level of analog variation that can be distinguished by the A/D converter.
When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.
- Linearity error (unit: LSB)
It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point ("00 0000 0000" $\leftarrow \rightarrow$ "00 0000 0001") of a device to the full-scale transition point ("11 1111 1111" $\leftarrow \rightarrow$ "11 1111 1110") of the same device.
- Differential linear error (unit: LSB)
It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.
- Total error (unit: LSB)
It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.



(Continued)

(Continued)



$$\text{Linearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times N + V_{OT}\}}{1 \text{ LSB}}$$

$$\text{Differential linear error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from (N - 1)_H to N_H

V_{OT} (ideal value) = V_{ss} + 0.5 LSB [V]

V_{FST} (ideal value) = V_{cc} - 2 LSB [V]

6. Flash Memory Program/Erase Characteristics

| Parameter | Value | | | Unit | Remarks |
|--|------------------|-------------------|--------------------|-------|---|
| | Min | Typ | Max | | |
| Sector erase time (2 Kbyte sector) | — | 0.2* ¹ | 0.5* ² | s | The time of programming 00 _H prior to erasure is excluded. |
| Sector erase time (16 Kbyte sector) | — | 0.5* ¹ | 7.5* ² | s | The time of programming 00 _H prior to erasure is excluded. |
| Byte programming time | — | 21 | 6100* ² | μs | System-level overhead is excluded. |
| Program/erase cycle | 100000 | — | — | cycle | |
| Power supply voltage at program/erase | 2.7 | 3.0 | 3.6 | V | |
| Flash memory data retention time | 20* ³ | — | — | year | Average T _A = +85°C |

*1: T_A = +25°C, V_{CC} = 3.0 V, 100000 cycles

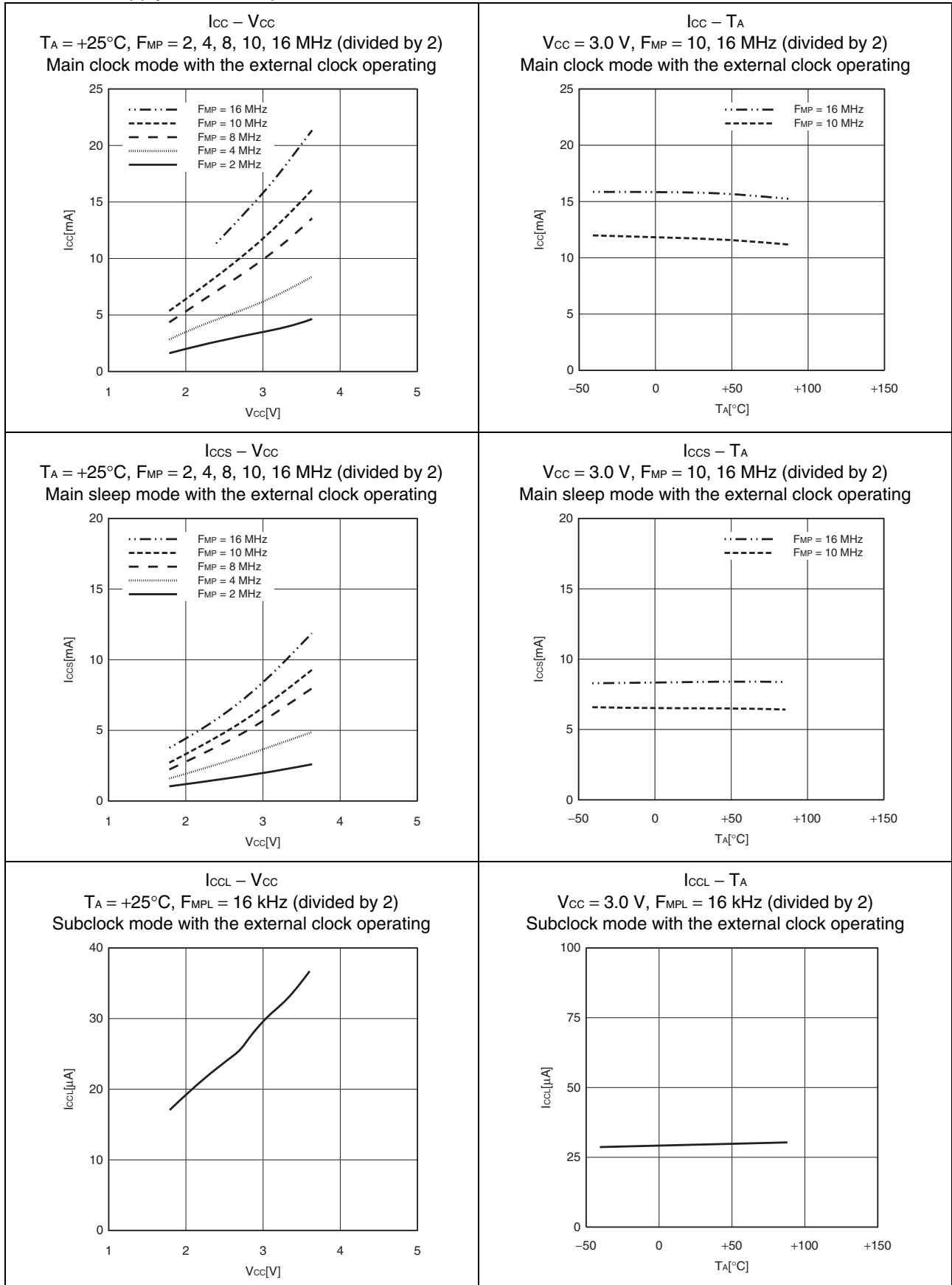
*2: T_A = +85°C, V_{CC} = 2.7 V, 100000 cycles

*3: This value is converted from the result of a technology reliability assessment. (The value is converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being +85°C).

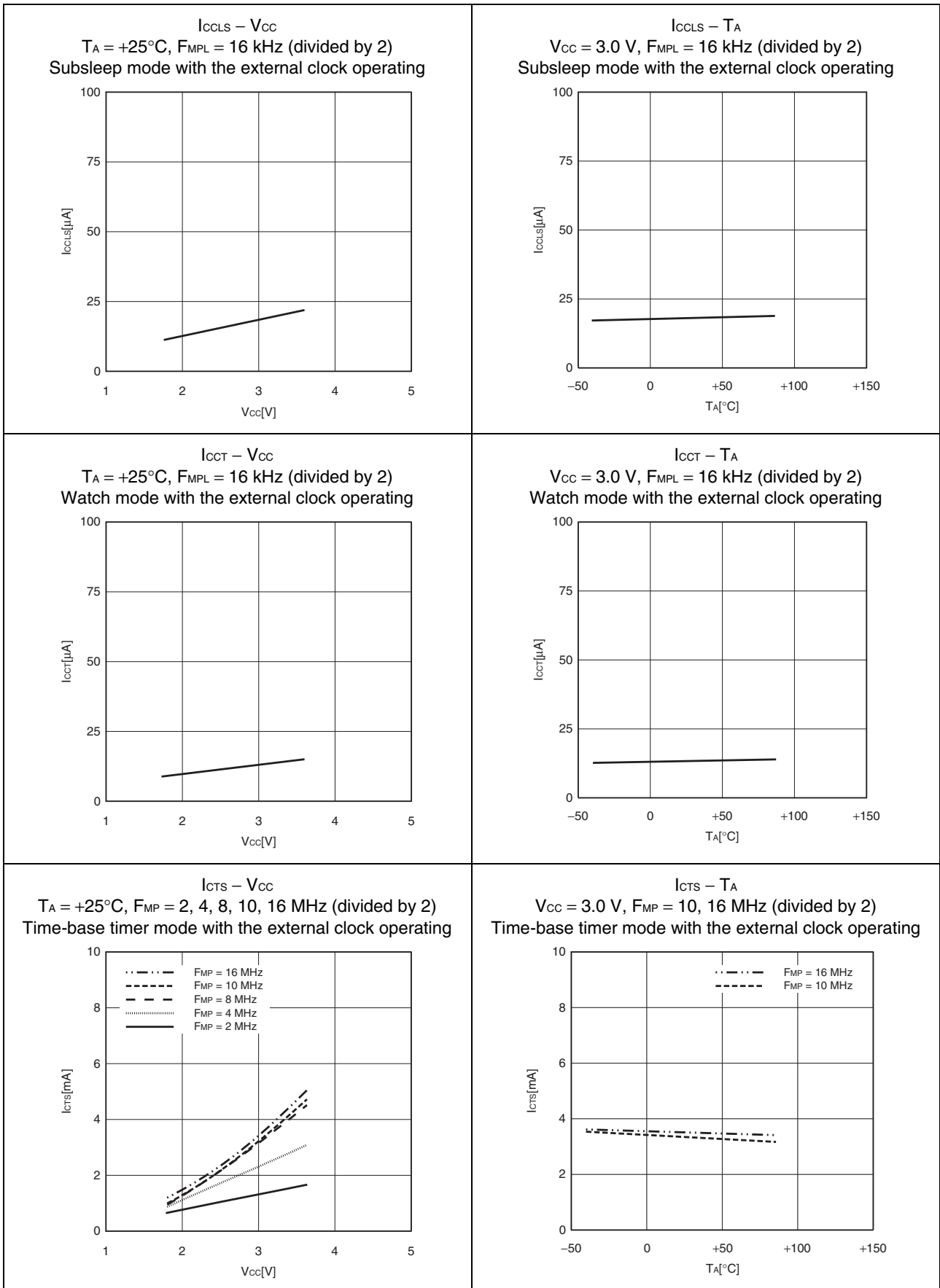
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■ SAMPLE CHARACTERISTICS

- Power supply current temperature characteristics



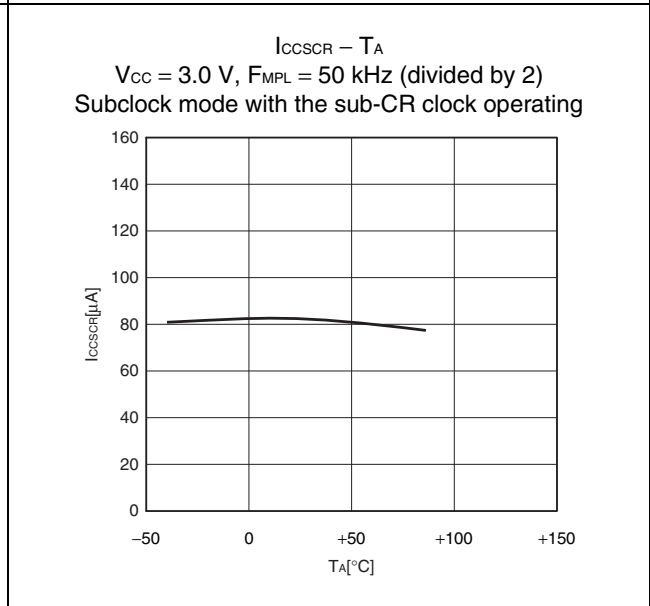
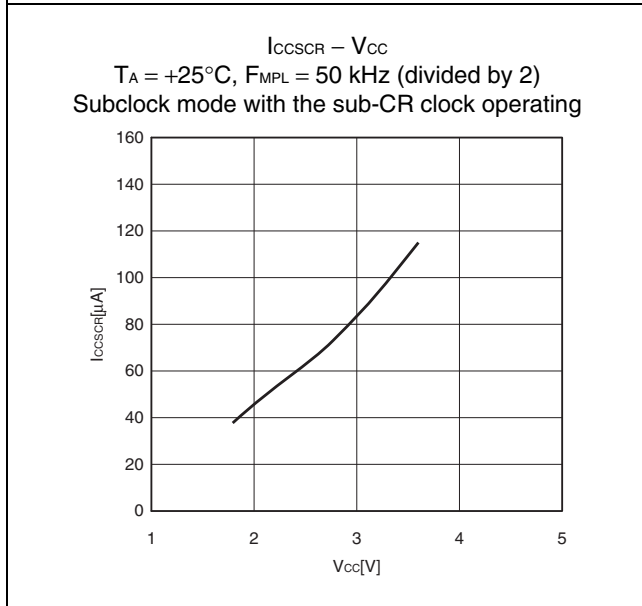
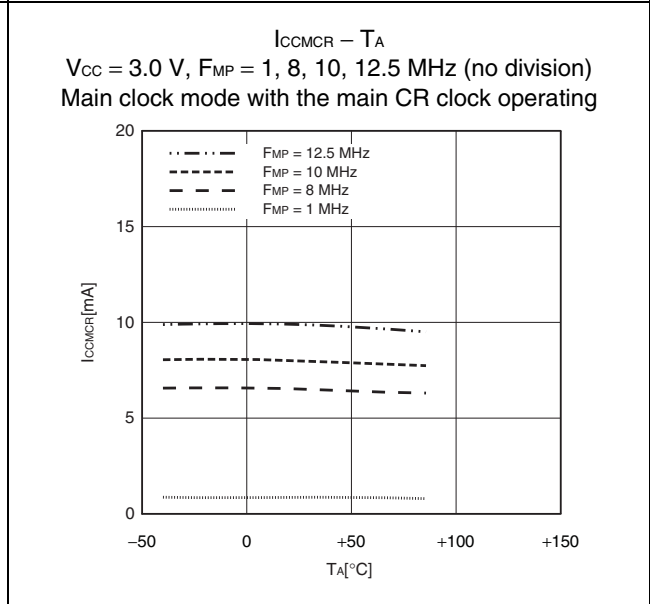
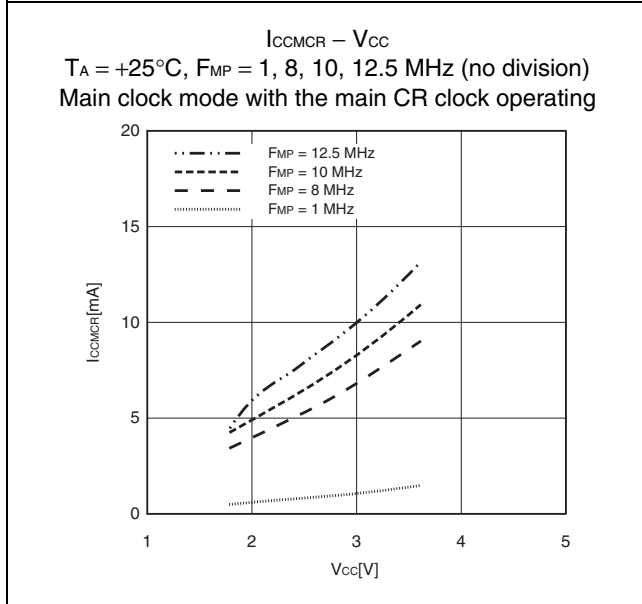
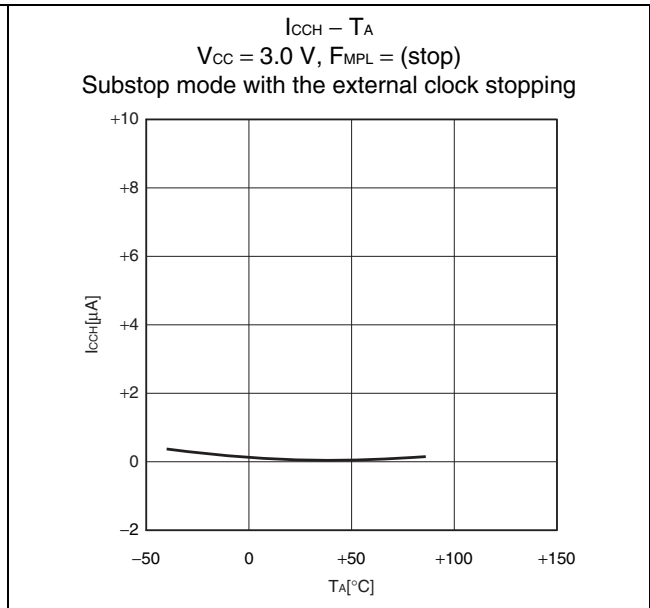
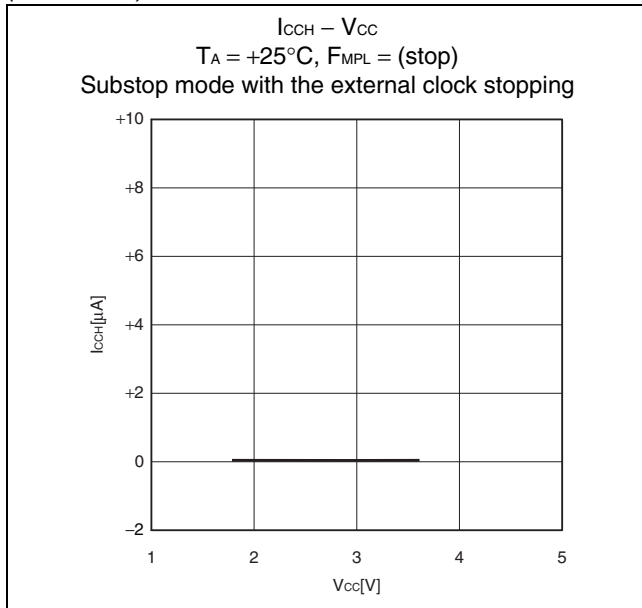
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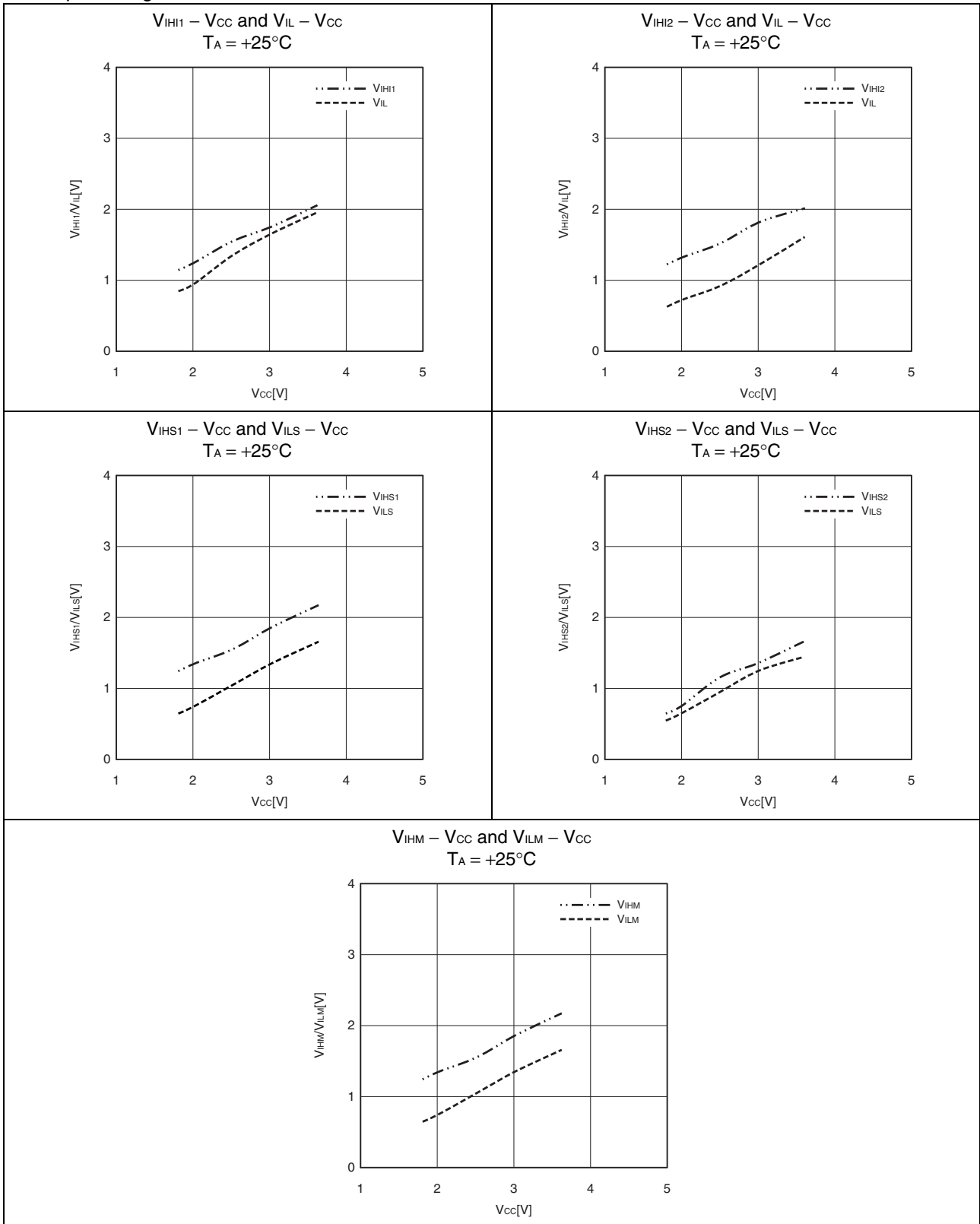
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MB95310L/370L Series

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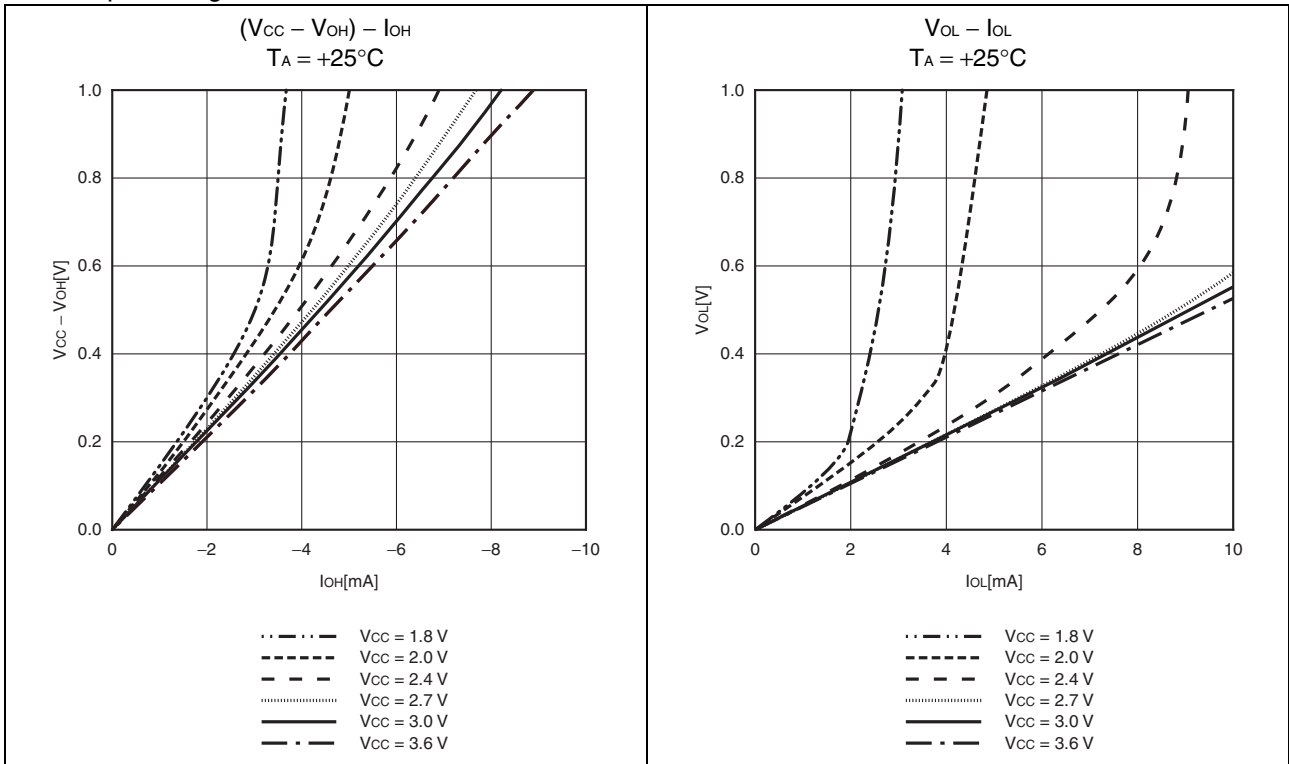


• Input voltage characteristics

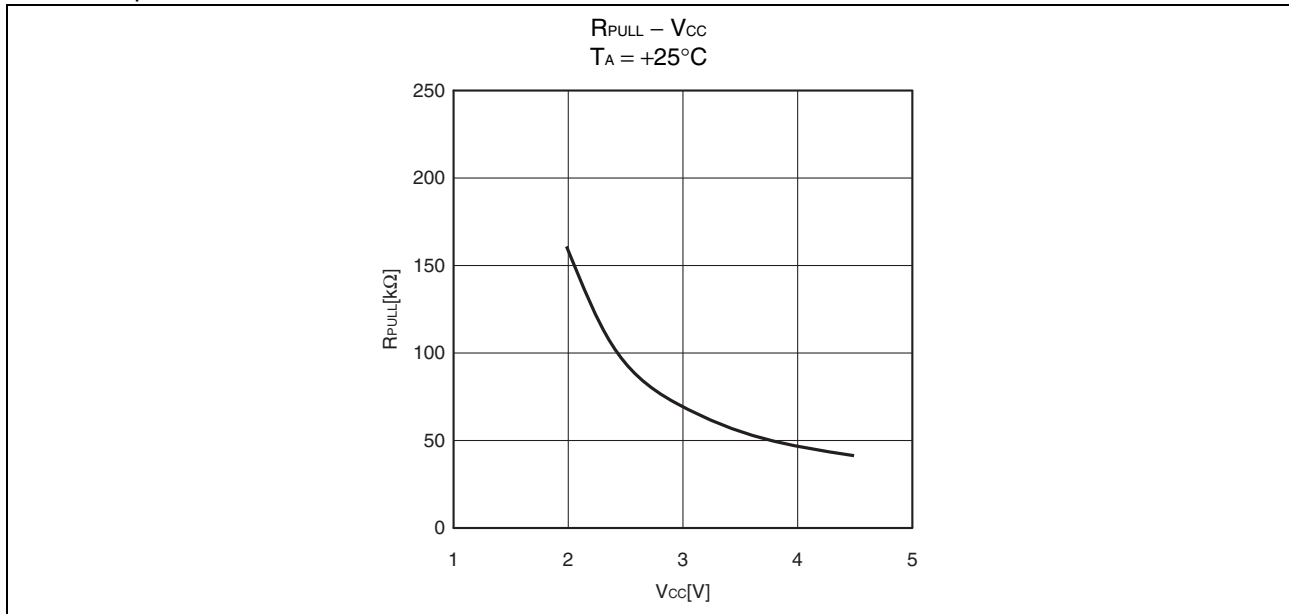


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- Output voltage characteristics



- Pull-up characteristics



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■ MASK OPTIONS

| No. | Part Number | MB95F314E MB95F316E MB95F318E MB95F374E MB95F376E MB95F378E | MB95F314L MB95F316L MB95F318L MB95F374L MB95F376L MB95F378L |
|-----|-----------------------------|--|--|
| | Selectable/Fixed | Fixed | |
| 1 | Low-voltage detection reset | With low-voltage detection reset | Without low-voltage detection reset |

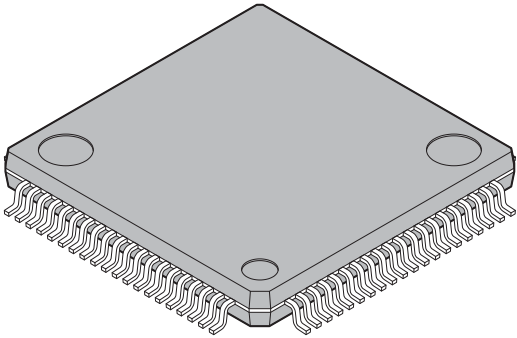
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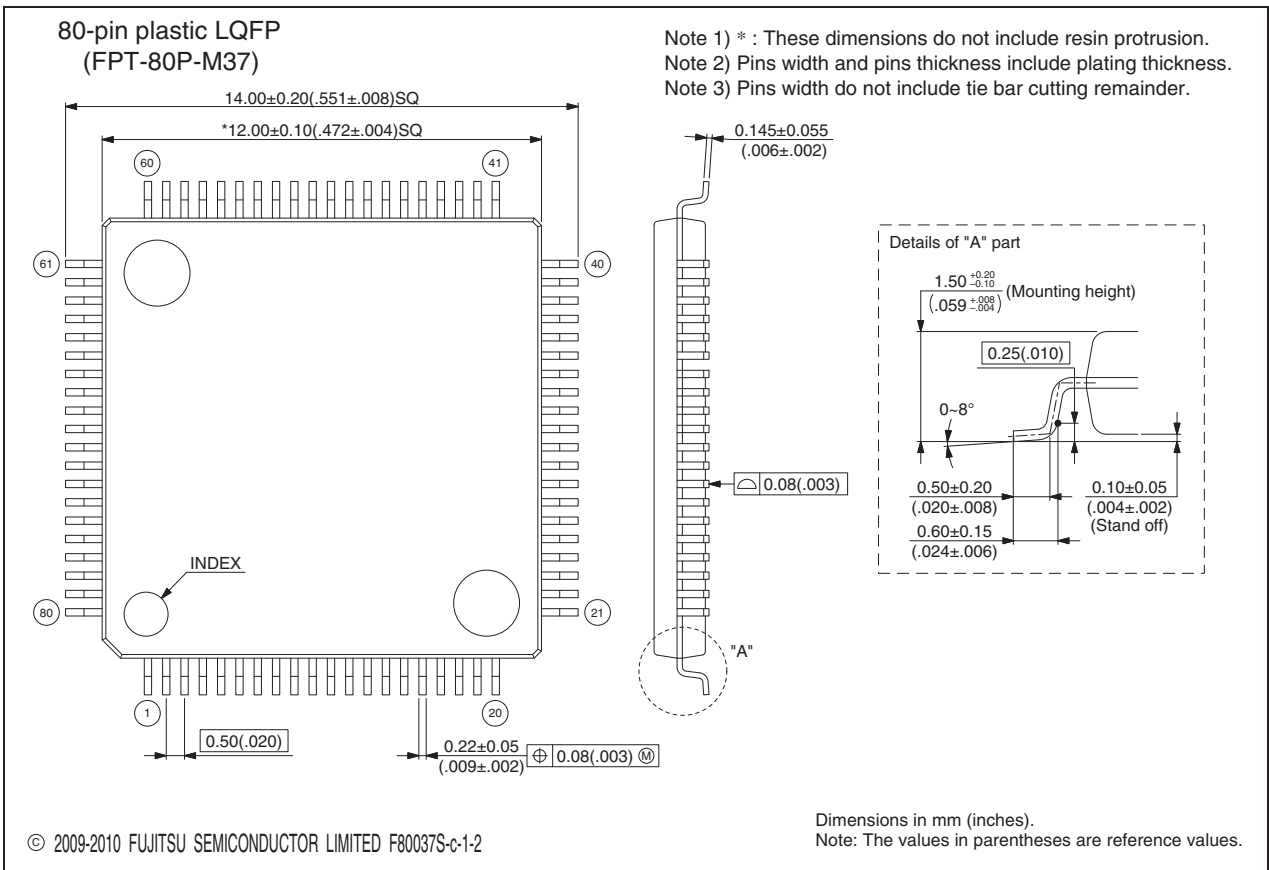
■ ORDERING INFORMATION

| Part Number | Package |
|--|--------------------------------------|
| MB95F314EPMC-G-SNE2 MB95F314LPMC-G-SNE2 MB95F316EPMC-G-SNE2 MB95F316LPMC-G-SNE2 MB95F318EPMC-G-SNE2 MB95F318LPMC-G-SNE2 | 80-pin plastic LQFP (FPT-80P-M37) |
| MB95F374EPMC1-G-SNE2 MB95F374LPMC1-G-SNE2 MB95F376EPMC1-G-SNE2 MB95F376LPMC1-G-SNE2 MB95F378EPMC1-G-SNE2 MB95F378LPMC1-G-SNE2 | 64-pin plastic LQFP (FPT-64P-M38) |
| MB95F374EPMC2-G-SNE2 MB95F374LPMC2-G-SNE2 MB95F376EPMC2-G-SNE2 MB95F376LPMC2-G-SNE2 MB95F378EPMC2-G-SNE2 MB95F378LPMC2-G-SNE2 | 64-pin plastic LQFP (FPT-64P-M39) |

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PACKAGE DIMENSION

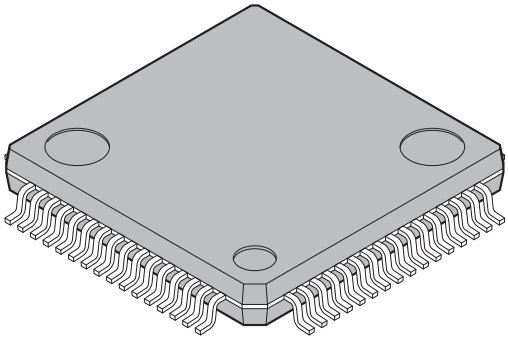
| | | |
|---|--------------------------------|---------------------|
|  <p>80-pin plastic LQFP</p> <p>(FPT-80P-M37)</p> | Lead pitch | 0.50 mm |
| | Package width × package length | 12.00 mm × 12.00 mm |
| | Lead shape | Gullwing |
| | Lead bend direction | Normal bend |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Weight | 0.47 g |

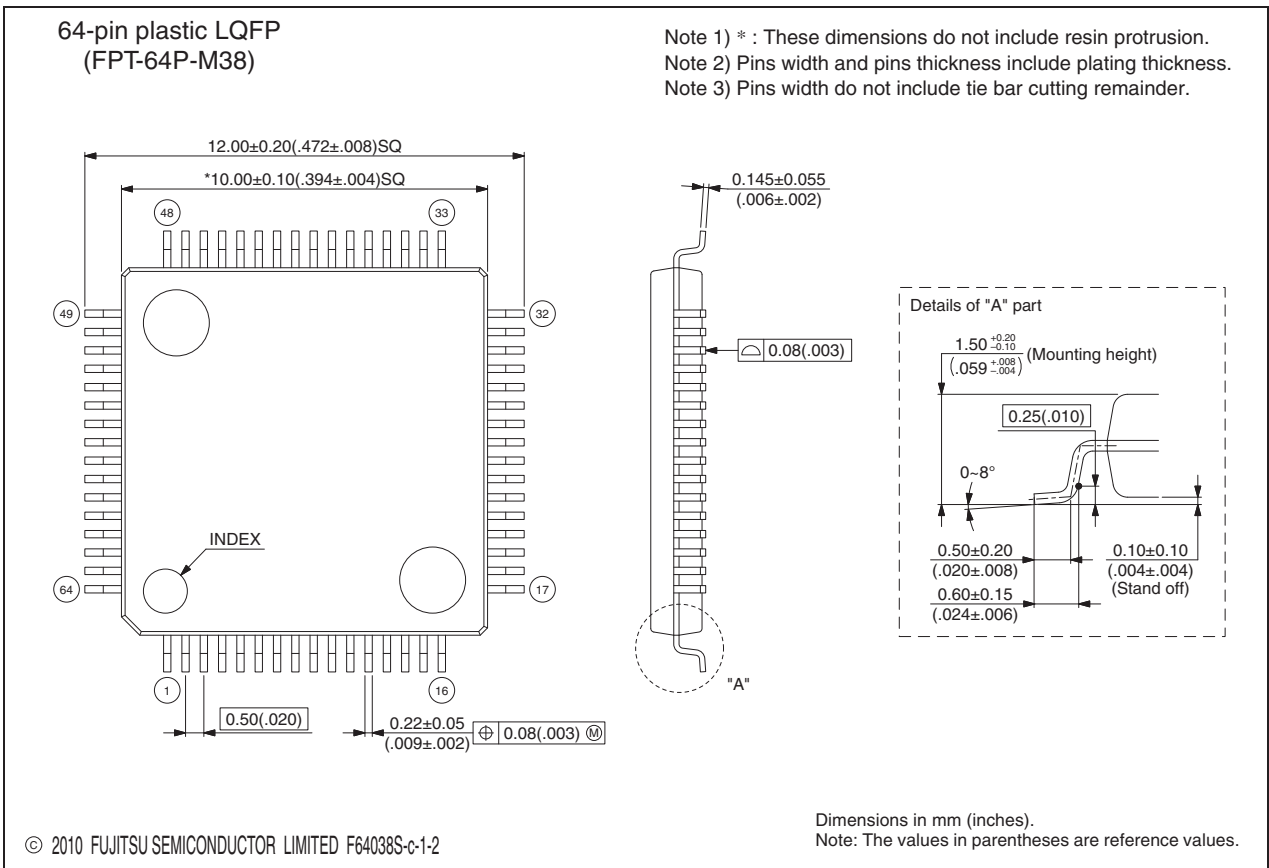


Please check the latest package dimension at the following URL.
<http://edevic.fujitsu.com/package/en-search/>

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| | | |
|---|--------------------------------|---------------------|
| <p>64-pin plastic LQFP</p>  <p>(FPT-64P-M38)</p> | Lead pitch | 0.50 mm |
| | Package width × package length | 10.00 mm × 10.00 mm |
| | Lead shape | Gullwing |
| | Lead bend direction | Normal bend |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Weight | 0.32 g |

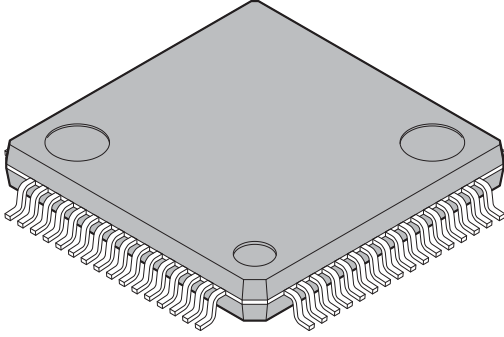


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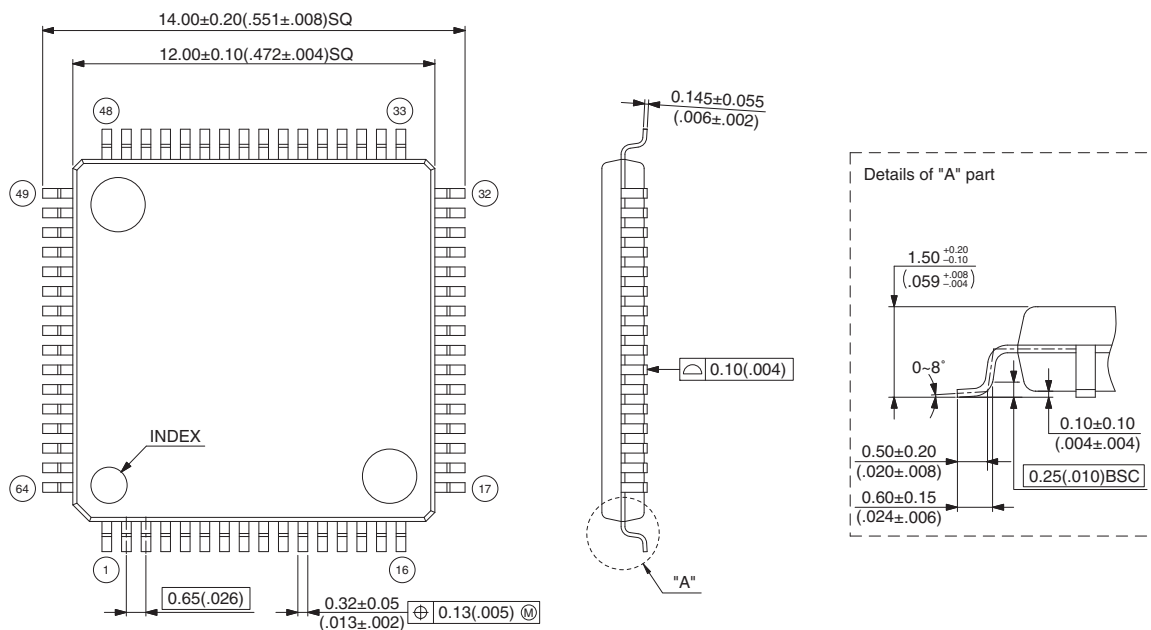
MB95310L/370L Series

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| | | |
|---|--------------------------------|---------------------|
| <p>64-pin plastic LQFP</p>  <p>(FPT-64P-M39)</p> | Lead pitch | 0.65 mm |
| | Package width × package length | 12.00 mm × 12.00 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Weight | 0.47 g |
| | | |

64-pin plastic LQFP (FPT-64P-M39)

Note 1) Pins width and pins thickness include plating thickness.



Top view dimensions:
 Overall width: 14.00 ± 0.20 ($.551 \pm .008$) SQ
 Pin pitch: 0.65 (.026)
 Pin width: 0.32 ± 0.05 ($.013 \pm .002$)
 Pin thickness: 0.13 (.005) M

Side view dimensions:
 Pin height: 0.145 ± 0.055 ($.006 \pm .002$)
 Lead thickness: 0.10 (.004)

Details of "A" part:
 Lead height: $1.50^{+0.20}_{-0.10}$ ($.059^{+.008}_{-.004}$)
 Lead angle: 0-8°
 Lead thickness: 0.10 ± 0.10 ($.004 \pm .004$)
 Lead width: 0.50 ± 0.20 ($.020 \pm .008$)
 Lead thickness: 0.60 ± 0.15 ($.024 \pm .006$)
 Reference: 0.25(.010)BSC

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Dimensions in mm (inches).
 Note: The values in parentheses are reference values.

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■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

| Page | Section | Details |
|----------|--|---|
| 1 | — | Changed the family name. F ² MC-8FX → New 8FX |
| 1 | ■ FEATURES | Changed the main CR clock oscillation frequency. 1/8/10 MHz ±3%, maximum machine clock frequency: 10 MHz → 1/8/10/12.5 MHz ±2%, maximum machine clock frequency: 12.5 MHz |
| 23 | ■ PIN CONNECTION | Added “• Notes on handling the external clock pins while using the CR clock”. |
| 46 | ■ ELECTRICAL CHARACTERISTICS 3. DC Characteristics | Changed the condition for the power supply current (I _{CCMCR}). F _{CRH} = 10 MHz F _{MP} = 10 MHz Main CR clock mode → F _{CRH} = 12.5 MHz F _{MP} = 12.5 MHz Main CR clock mode Changed the condition for the power supply current (I _{CCSCR}). F _{CL} = 32 kHz F _{MPL} = 16 kHz Sub-CR clock mode (divided by 2) T _A = +25°C → Sub-CR clock mode (divided by 2) T _A = +25°C |
| 47 | | Changed the condition for the power supply current (I _{CRH}). Current consumption for the main CR oscillator at 10 MHz → Current consumption for the main CR oscillator |
| 48 | ■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (1) Clock Timing | Changed the values of the clock frequency (F _{CRH}). |
| 58 | ■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (7) Low-voltage Detection | Deleted the following parameters: Power hysteresis width 0, Power hysteresis width 1, Power hysteresis width 2, Interrupt hysteresis width 0, Interrupt hysteresis width 1, Interrupt hysteresis width 2, Interrupt hysteresis width 3, Interrupt hysteresis width 4 |
| 59 | | Deleted V _{PHYS} /V _{IHYS} from the diagram. |
| 64 | ■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (8) I ² C Timing | Changed the settings related to the machine clock shown in *2. |
| 70 to 75 | ■ SAMPLE CHARACTERISTICS | Added “■ SAMPLE CHARACTERISTICS”. |

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MEMO

MB95310L/370L Series

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