GENERAL DESCRIPTION

The XRT83VSH316 is a fully integrated 16-channel short-haul line interface unit (LIU) that operates from a 1.8V Inner Core and 3.3V I/O power supplies. Using internal termination, the LIU provides one bill of materials to operate in T1, E1, or J1 mode independently on a per channel basis with minimum external components. The LIU features are programmed through a standard parallel microprocessor interface or SPI (Serial Mode). EXAR's LIU has patented high impedance circuits that allow the transmitter outputs and receiver inputs to be high impedance when experiencing a power failure or when the LIU is powered off. Key design features within the LIU optimize 1:1 or 1+1 redundancy and non-intrusive monitoring applications to ensure reliability without using relays.

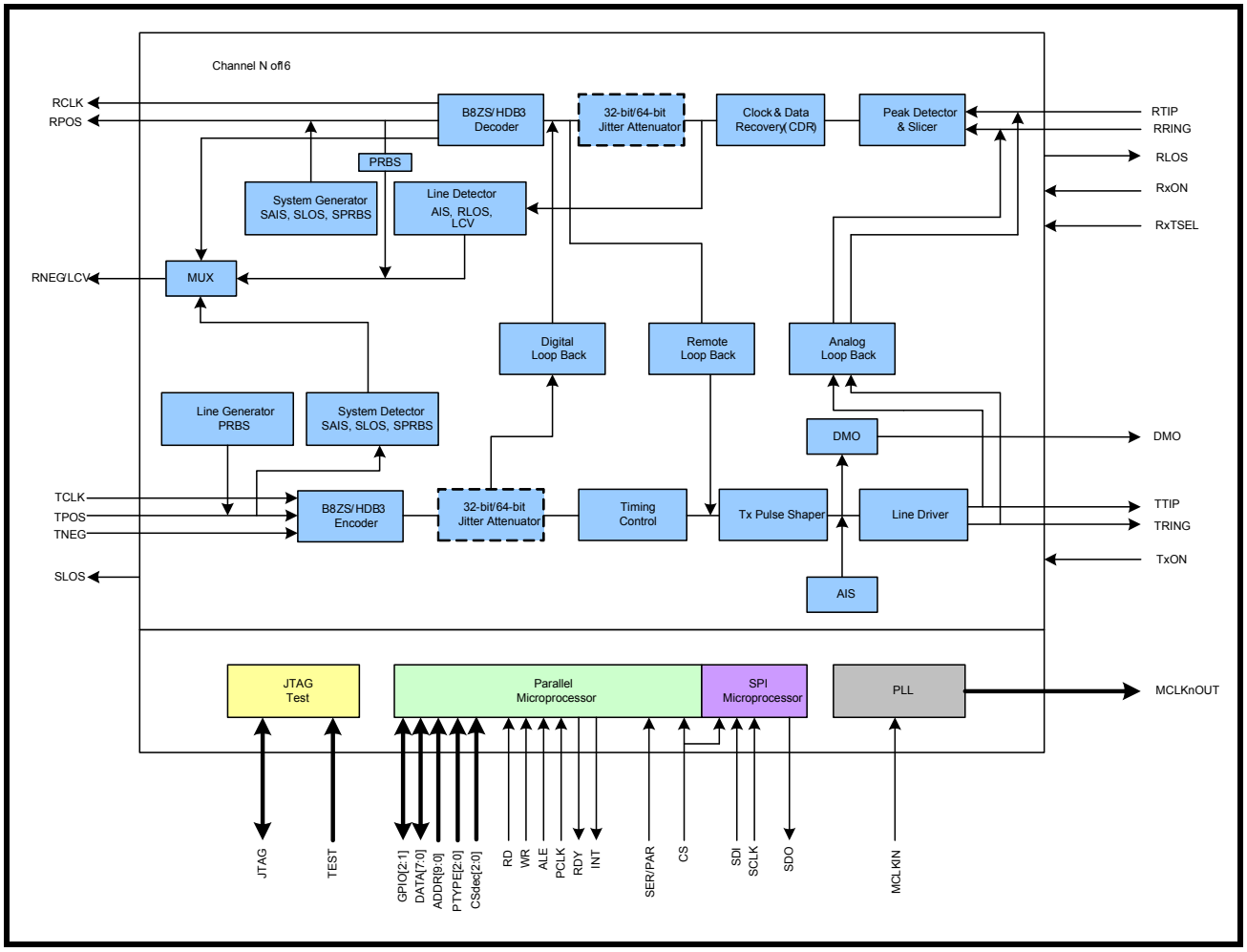
The on-chip clock synthesizer generates T1/E1/J1 clock rates from a selectable external clock frequency and has five output clock references that can be used for external timing (8kHz, 1.544Mhz, 2.048Mhz, nxT1/J1, nxE1).

Additional features include System Side LOS, AIS, QRSS/PRBS and Line Side RLOS, AIS, QRSS/PRBS, DMO with 16-bit LCV counters and diagnostic loopback modes for each channel.

APPLICATIONS

- T1 Digital Cross Connects (DSX-1)
- ISDN Primary Rate Interface
- CSU/DSU E1/T1/J1 Interface
- T1/E1/J1 LAN/WAN Routers
- Public Switching Systems and PBX Interfaces
- T1/E1/J1 Multiplexer and Channel Banks
- Integrated Multi-Service Access Platforms (IMAPs)
- Integrated Access Devices (IADs)
- Inverse Multiplexing for ATM (IMA)
- Wireless Base Stations

FIGURE 1. BLOCK DIAGRAM OF THE XRT83VSH316



FEATURES

- Fully integrated 16-Channel short haul transceivers for T1/J1 (1.544MHz) and E1 (2.048MHz) applications
- Parallel or SPI Microprocessor Interface
- T1/E1/J1 short haul and clock rate are per port selectable through software without changing components
- Internal Impedance matching on both receive and transmit for 75Ω (E1), 100Ω (T1), 110Ω (J1), and 120Ω (E1) applications are per port selectable through software without changing components
- Power down on a per channel basis with independent receive and transmit selection
- Five pre-programmed transmit pulse settings for T1 short haul applications per channel
- User programable Arbitrary Pulse mode for T1 and E1
- On-Chip transmit short-circuit protection and limiting protects line drivers from damage on a per channel basis
- Crystal-Less digital jitter attenuators (JA) with 32-Bit or 64-Bit FIFO for the receive or transmit path per channel
- Driver failure monitor output (DMO) alerts of possible system or external component problems
- Transmit outputs and receive inputs may be "High" impedance for protection or redundancy applications on a per channel basis
- Support for automatic protection switching
- 1:1 and 1+1 protection without relays
- Receive monitor mode handles 0 to 6dB resistive attenuation (flat loss) along with 0 to 6dB cable loss for both T1 and E1
- Loss of signal (LOS) according to ITU-T G.775/ETS300233 (E1) and ANSI T1.403 (T1/J1) for system (SLOS) and line (RLOS) side diagnostics
- Programmable data stream muting upon RLOS detection
- On-Chip HDB3/B8ZS encoder/decoder with an internal 16-bit LCV counter for each channel
- On-Chip digital clock recovery circuit for high input jitter tolerance
- QRSS/PRBS pattern generator and detection for testing and monitoring for system (SPRBS) and line (PRBS) side diagnostics
- Error and bipolar violation insertion and detection
- Transmit all ones (TAOS) Generators and Detectors for system (SAIS) and line (AIS) side diagnostics
- Supports local analog, remote, digital, and dual loopback modes
- Supports gapped clocks for mapper/multiplexer applications
- 1.8V Digital Core
- 3.3V I/O and Analog Core
- 316-Pin STBGA package
- -40°C to +85°C Temperature Range

PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT83VSH316IB-F	316 Shrink Thin Ball Grid Array (21.0 mm x 21.0 mm, STBGA)	-40^{O}C to +85^{O}C

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1.0 PIN DESCRIPTIONS

MICROPROCESSOR

NAME	PIN	TYPE	DESCRIPTION
$\overline{CS}$	A19	I	**Chip Select Input** Active low signal. This signal enables the microprocessor interface by pulling chip select "Low". The microprocessor interface is disabled when the chip select signal returns "High". This pin is used for both the Parallel or the Serial Interface modes. ***NOTE:*** *Internally pulled "High" with a 50k Ω resistor.*
ALE_TS	D15	I	**Address Latch Enable Input (Transfer Start)** See the Microprocessor section of this datasheet for a description. ***NOTE:*** *Internally pulled "Low" with a 50k Ω resistor.*
$\overline{WR}$_R/$\overline{W}$	E15	I	**Write Strobe Input (Read/Write)** See the Microprocessor section of this datasheet for a description. ***NOTE:*** *Internally pulled "Low" with a 50k Ω resistor.*
$\overline{RD}$_$\overline{WE}$	C18	I	**Read Strobe Input (Write Enable)** See the Microprocessor section of this datasheet for a description. ***NOTE:*** *Internally pulled "Low" with a 50k Ω resistor.*
$\overline{RDY}$_$\overline{TA}$	R5	O	**Ready Output (Transfer Acknowledge)** See the Microprocessor section of this datasheet for a description.
$\overline{INT}$	B19	O	**Interrupt Output** Active low signal. This signal is asserted "Low" when a change in alarm status occurs. Once the status registers have been read, the interrupt pin will return "High". GIE (Global Interrupt Enable) must be set "High" in the appropriate global register to enable interrupt generation. ***NOTE:*** *This pin is an open-drain output that requires an external 10KΩ pull-up resistor.*
PCLK	U6	I	**Micro Processor Clock Input** In a synchronous microprocessor interface, PCLK is used as the internal timing reference for programming the LIU. ***NOTE:*** *Internally pulled "Low" with a 50k Ω resistor.*
ADDR9 ADDR8 ADDR7 ADDR6 ADDR5 ADDR4 ADDR3 ADDR2 ADDR1 ADDR0	E17 D17 Y18 W18 W17 V17 V16 U16 U15 T15	I	**Address Bus Input** ADDR[9:0] are a direct address bus for permitting access to the internal registers. ***NOTE:*** *Internally pulled "Low" with a 50k Ω resistor.*

MICROPROCESSOR

NAME	PIN	TYPE	DESCRIPTION
CSdec2 CSdec1 CSdec0	U17 F16 E16	I	**Chip Select Decoder Input Pins [2:0]** CSdec[2:0] are used as a chip select decoder. The LIU has 5 chip select output pins for enabling up to 5 additional devices for accessing internal registers. The LIU has the option to select itself (master device), up to 5 additional devices, or all 6 devices simultaneously by setting the CSdec[2:0] pins specified below. 000 = Master Device 001 = Chip Select Output 1 010 = Chip Select Output 2 011 = Chip Select Output 3 100 = Chip Select Output 4 101 = Chip Select Output 5 110 = Reserved 111 = All Chip Selects Active Including the Master Device *Internally pulled "Low" with a 50k Ω resistor.*
DATA7 DATA6 DATA5 DATA4 DATA3 DATA2 DATA1 DATA0	U5 V5 V4 W4 W3 Y3 Y2 Y5	I/O	**Bi-directional Data Bus** DATA[7:0] is a bi-directional data bus used for read and write operations. ***NOTE:*** *Internally pulled "Low" with a 50k Ω resistor.*
PTYPE2 PTYPE1 PTYPE0	W19 W2 U4	I	**Microprocessor Type Select Input** PTYPE[2:0] are used to select the microprocessor type interface. 000 = Intel 8051 Asynchronous 001 = Motorola Asynchronous 101 = Power PC Synchronous 111 = MPC8xx Motorola Synchronous ***NOTE:*** *Internally pulled "Low" with a 50k Ω resistor.*
$\overline{\text{Reset}}$	D16	I	**Hardware Reset Input** Active low signal. When this pin is pulled "Low" for more than 10µS, the internal registers are set to their default state. See the register description for the default values. ***NOTE:*** *Internally pulled "High" with a 50KΩ resistor.*
$\overline{\text{CS5}}$ $\overline{\text{CS4}}$ $\overline{\text{CS3}}$ $\overline{\text{CS2}}$ $\overline{\text{CS1}}$	C16 C17 B17 B18 A18	O	**Chip Select Output** The XRT83VSH316 can be used to provide the necessary chip selects for up to 5 additional devices by using the CSdec[2:0] input pins. The LIU allows up to 84-channel applications with only using one chip select. See the CSdec[2:0] definition in the pin description.
GPIO1 GPIO0	T16 R16	I/O	**General Purpose Input/Output** These two GPIO pins are controlled through the internal registers in the microprocessor block. One register controls the direction, while the other register is used to store or retrieve the status of these pins.

RECEIVER SECTION

NAME	PIN	TYPE	DESCRIPTION
RxON	Y16	I	**Receive On/Off Input** Upon power up, the receivers are powered off. Turning the receivers On or Off can be selected through the microprocessor interface by programming the appropriate channel register if the hardware pin is pulled "High". If the hardware pin is pulled "Low", all channels are automatically turned off. ***NOTE:*** *Internally pulled "Low" with a 50KΩ resistor.*
RxTSEL	A16	I	**Receive Termination Control** Upon power up, the receivers are in "High" impedance. Switching to internal termination can be selected through the microprocessor interface by programming the appropriate channel register. However, to switch control to the hardware pin, RxTCNTL must be programmed to "1" in the appropriate global register. Once control has been granted to the hardware pin, it must be pulled "High" to switch to internal termination. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.* **RxTSEL (pin)** / **Rx Termination** 0 / External 1 / Internal *Note: RxTCNTL (bit) must be set to "1"*
RLOS	T4	O	**Receive Loss of Signal (Global Pin for All 16-Channels)** When a line side receive loss of signal occurs for any one of the 16-channels according to ITU-T G.775, the RLOS pin will go "High" for a minimum of one RCLK cycle. RLOS will remain "High" until the loss of signal condition clears. See the Receive Loss of Signal section of this datasheet for more details. ***NOTE:*** *This pin is for redundancy applications to initiate an automatic switch to the backup card. For individual channel RLOS, see the register map.*
SRLOS	T5	O	**System Receive Loss of Signal (Global Pin for All 16-Channels)** When a system side receive loss of signal occurs for any one of the 16-channels according to ITU-T G.775, the SRLOS pin will go "High" for a minimum of one TCLK cycle. SRLOS will remain "High" until the loss of signal condition clears. See the Receive Loss of Signal section of this datasheet for more details.

RECEIVER SECTION

NAME	PIN	TYPE	DESCRIPTION
RCLK15 RCLK14 RCLK13 RCLK12 RCLK11 RCLK10 RCLK9 RCLK8 RCLK7 RCLK6 RCLK5 RCLK4 RCLK3 RCLK2 RCLK1 RCLK0	V12 R17 N18 V15 C15 H18 F17 C12 C9 F4 H3 C6 V6 N3 R4 V9	O	**Receive Clock Output** RCLK is the recovered clock from the incoming data stream. If the incoming signal is absent or RxON is pulled "Low", RCLK maintains its timing by using an internal master clock as its reference. Software control (RCLKE) allows RPOS/RNEG data to be updated on either edge of RCLK. ***NOTE:*** *RCLKE is a global setting that applies to all 16 channels.*

RECEIVER SECTION

<table>
<tr><th>NAME</th><th>PIN</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>RCLK_IO</td><td>C5</td><td>I/O</td><td>Recovered Clock Input/Output:
This bi-directional clock can be used in two different modes:
1. As an input, the LIU will use this clock as its internal clock timing synchronization of the 19.44Mhz clock reference.
2. As an output, it is one of 16 recoverd line clocks selected by the Recovered Clock Select [4:0] bits and output through this pin.
See table below.

<table>
<tr><th>Recovered Clock Select [4:0]</th><th>Selected RCLK</th></tr>
<tr><td>0XXXX</td><td>Input</td></tr>
<tr><td>10000</td><td>RCLK0</td></tr>
<tr><td>10001</td><td>RCLK1</td></tr>
<tr><td>10010</td><td>RCLK2</td></tr>
<tr><td>10011</td><td>RCLK3</td></tr>
<tr><td>10100</td><td>RCLK4</td></tr>
<tr><td>10101</td><td>RCLK5</td></tr>
<tr><td>10110</td><td>RCLK6</td></tr>
<tr><td>10111</td><td>RCLK7</td></tr>
<tr><td>11000</td><td>RCLK8</td></tr>
<tr><td>11001</td><td>RCLK9</td></tr>
<tr><td>11010</td><td>RCLK10</td></tr>
<tr><td>11011</td><td>RCLK11</td></tr>
<tr><td>11100</td><td>RCLK12</td></tr>
<tr><td>11101</td><td>RCLK13</td></tr>
<tr><td>11110</td><td>RCLK14</td></tr>
<tr><td>11111</td><td>RCLK15</td></tr>
</table>
</td></tr>
<tr><td>RCLK_T1_E1B</td><td>V18</td><td>I/O</td><td>Recovered Clock Frequency Select
This bi-directional clock can be used in two different modes along with the RCLK_IO pin.
1. As an input (RCLK_IO must be an input), it selects the frequency of the RCLK_IO input. "Low" = E1, "High" = T1.
2. As an output (RCLK_IO must be an output), it indicates the frequency of RCLK_IO, "Low" = E1, "High" = T1.
NOTE: The RCLKSEL[4:0] bits determine whether this pin is an input or output.</td></tr>
</table>

RECEIVER SECTION

NAME	PIN	TYPE	DESCRIPTION
RPOS15 RPOS14 RPOS13 RPOS12 RPOS11 RPOS10 RPOS9 RPOS8 RPOS7 RPOS6 RPOS5 RPOS4 RPOS3 RPOS2 RPOS1 RPOS0	U12 U19 P19 W15 B15 G19 D19 D12 D9 D2 G2 B6 W6 P2 U2 U9	O	**RPOS/RDATA Output** Receive digital output pin. In dual rail mode, this pin is the receive positive data output. In single rail mode, this pin is the receive non-return to zero (NRZ) data output.
RNEG15 RNEG14 RNEG13 RNEG12 RNEG11 RNEG10 RNEG9 RNEG8 RNEG7 RNEG6 RNEG5 RNEG4 RNEG3 RNEG2 RNEG1 RNEG0	W11 T18 P18 N19 H19 G18 E18 B11 B10 E3 G3 H2 N2 P3 T3 W10	O	**RNEG/LCV_OF Output** In dual rail mode, this pin is the receive negative data output. In single rail mode, this pin can either be a Line Code Violation or Overflow indicator. If LCV is selected by software and if a line code violation, a bi-polar violation, or excessive zeros occur, the LCV pin will pull "High" for a minimum of one RCLK cycle. LCV will remain "High" until there are no more violations. However, if OF is selected the LCV pin will pull "High" if the internal LCV counter is saturated. The LCV pin will remain "High" until the LCV counter is reset.

RECEIVER SECTION

NAME	PIN	TYPE	DESCRIPTION
RTIP15 RTIP14 RTIP13 RTIP12 RTIP11 RTIP10 RTIP9 RTIP8 RTIP7 RTIP6 RTIP5 RTIP4 RTIP3 RTIP2 RTIP1 RTIP0	Y12 V20 T20 P20 G20 E20 C20 A12 A9 C1 E1 G1 P1 T1 V1 Y9	I	**Receive Differential Tip Input** RTIP is the positive differential input from the line interface. Along with the RRING signal, these pins should be coupled to a 1:1 transformer for proper operation.
RRING15 RRING14 RRING13 RRING12 RRING11 RRING10 RRING9 RRING8 RRING7 RRING6 RRING5 RRING4 RRING3 RRING2 RRING1 RRING0	Y11 U20 R20 N20 H20 F20 D20 A11 A10 D1 F1 H1 N1 R1 U1 Y10	I	**Receive Differential Ring Input** RRING is the negative differential input from the line interface. Along with the RTIP signal, these pins should be coupled to a 1:1 transformer for proper operation.

TRANSMITTER SECTION

NAME	PIN	TYPE	DESCRIPTION
TxON	Y19	I	**Transmit On/Off Input** Upon power up, the transmitters are powered off. Turning the transmitters On or Off is selected through the microprocessor interface by programming the appropriate channel register if this pin is pulled "High". If the TxON pin is pulled "Low", all 16 transmitters are powered off. ***NOTES:*** *1. TxON is ideal for redundancy applications. See the Redundancy Applications Section of this datasheet for more details.* *2. Internally pulled "Low" with a 50KΩ resistor.*
DMO	T6	O	**Digital Monitor Output (Global Pin for All 16-Channels)** When no transmit output pulse is detected for more than 128 TCLK cycles on one of the 16-channels, the DMO pin will go "High" for a minimum of one TCLK cycle. DMO will remain "High" until the transmitter sends a valid pulse. ***NOTE:*** *This pin is for redundancy applications to initiate an automatic switch to the backup card. For individual channel DMO, see the register map.*
TCLK15 TCLK14 TCLK13 TCLK12 TCLK11 TCLK10 TCLK9 TCLK8 TCLK7 TCLK6 TCLK5 TCLK4 TCLK3 TCLK2 TCLK1 TCLK0	W13 Y15 U13 U14 D14 D13 A15 B13 B8 A6 D8 D7 U7 U8 Y6 W8	I	**Transmit Clock Input** TCLK is the input facility clock used to sample the incoming TPOS/TNEG data. If TCLK is absent, pulled "Low", or pulled "High", the transmitter outputs at TTIP/TRING can be selected to send an all ones or an all zero signal by programming TCLKCNL. In addition, software control (TCLKE) allows TPOS/TNEG data to be sampled on either edge of TCLK. ***NOTES:*** *1. TCLKE is a global setting that applies to all 16 channels.* *2. Internally pulled "Low" with a 50k Ω resistor.*

TRANSMITTER SECTION

NAME	PIN	TYPE	DESCRIPTION
TPOS15 TPOS14 TPOS13 TPOS12 TPOS11 TPOS10 TPOS9 TPOS8 TPOS7 TPOS6 TPOS5 TPOS4 TPOS3 TPOS2 TPOS1 TPOS0	W12 Y14 V13 T14 E14 C13 A14 B12 B9 A7 C8 E7 T7 V8 Y7 W9	I	**TPOS/TDATA Input** Transmit digital input pin. In dual rail mode, this pin is the transmit positive data input. In single rail mode, this pin is the transmit non-return to zero (NRZ) data input. ***NOTE:*** *Internally pulled "Low" with a 50KΩ resistor.*
TNEG15 TNEG14 TNEG13 TNEG12 TNEG11 TNEG10 TNEG9 TNEG8 TNEG7 TNEG6 TNEG5 TNEG4 TNEG3 TNEG2 TNEG1 TNEG0	Y13 W14 T13 V14 C14 E13 B14 A13 A8 B7 E8 C7 V7 T8 W7 Y8	I	**Transmit Negative Data Input** In dual rail mode, this pin is the transmit negative data input. In single rail mode, this pin can be left unconnected. ***NOTE:*** *Internally pulled "Low" with a 50KΩ resistor.*

TRANSMITTER SECTION

NAME	PIN	TYPE	DESCRIPTION
TTIP15 TTIP14 TTIP13 TTIP12 TTIP11 TTIP10 TTIP9 TTIP8 TTIP7 TTIP6 TTIP5 TTIP4 TTIP3 TTIP2 TTIP1 TTIP0	T11 P16 L16 L17 K17 K16 G16 E11 E10 G5 K5 K4 L4 L5 P5 T10	O	**Transmit Differential Tip Output** TTIP is the positive differential output to the line interface. Along with the TRING signal, these pins should be coupled to a 1:2 step up transformer for proper operation.
TRING15 TRING14 TRING13 TRING12 TRING11 TRING10 TRING9 TRING8 TRING7 TRING6 TRING5 TRING4 TRING3 TRING2 TRING1 TRING0	V11 N16 M16 M19 J19 J16 H16 C11 C10 H5 J5 J2 M2 M5 N5 V10	O	**Transmit Differential Ring Output** TRING is the negative differential output to the line interface. Along with the TTIP signal, these pins should be coupled to a 1:2 step up transformer for proper operation.

CONTROL FUNCTION

NAME	PIN	TYPE	DESCRIPTION
TEST	V3	I	**Factory Test Mode** For normal operation, the TEST pin should be tied to ground. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
$\overline{\text{ICT}}$	C3	I	**In Circuit Testing** When this pin is tied "Low", all output pins are forced to "High" impedance for in circuit testing. ***NOTE:*** *Internally pulled "High" with a 50KΩ resistor.*

CLOCK SECTION

NAME	PIN	TYPE	DESCRIPTION
MCLKin	A5	I	**Master Clock Input** The master clock input can accept a wide range of inputs that can be used to generate T1 or E1 clock rates on a per channel basis. See the register map for details. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
8kHzOUT	B3	O	**8kHz Output Clock**
MCLKE1out	A2	O	**2.048MHz Output Clock**
MCLKE1Nout	A3	O	**2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz Output Clock** See the register map for programming details.
MCLKT1out	B4	O	**1.544MHz Output Clock**
MCLKT1Nout	C4	O	**1.544MHz, 3.088MHz, 6.176MHz, or 12.352MHz Output Clock** See the register map for programming details.
CLK19MHz	M1	O	**19.44MHz Output Clock Reference for Recovered Clock Synchronization** The purpose of this clock is to provide a 19.44MHz clock that is synchronous to either an externally provided clock or to one of the 16 selectable recovered line clocks from the LIU. See Figure 3 for details.
XTAL1	J1	I	**Crystal Input Pin** This pin should be tied to the input pin of a 19.44MHz crystal with an accuracy of +/-20ppm.
XTAL2	K1	O	**Crystal Output Pin** This pin should be tied to the output pin of a 19.44MHz crystal with an accuracy of +/-20ppm.
CMPOUT	L1	O	**Charge Pump Filter Output** See Figure 3 for filtering component selection.

SPI (SERIAL PERIPHERAL INTERFACE)

NOTE: *These pins are only used if the SPI interface is used in place of the parallel microprocessor interface. The SPI Microprocessor interface uses shared pins except for SER/PAR.*

NAME	PIN	TYPE	DESCRIPTION
SER/PAR	T17	I	**Serial/Parallel Select Input** This pin is used to select between the parallel microprocessor or serial interface. By default, the parallel microprocessor mode is selected. To configure the device for a serial interface, this pin must be pulled "HIgh". **NOTE:** *Internally pulled "Low" with a 50kΩ resistor.*
SCLK/PCLK	U6	I	**Serial Clock Input** If Pin SER_PAR is pulled "High", this input pin is used as the timing reference for the serial microprocessor interface. See the Microprocessor Section of this datasheet for details.
SDI/ADDR0	T15	I	**Serial Data Input** If Pin SER_PAR is pulled "High", this input pin from the serial interface is used to input the serial data for Read and Write operations. See the Microprocessor Section of this datasheet for details.
SDO/D0	Y5	O	**Serial Data Output** If Pin SER_PAR is pulled "High", this output pin from the serial interface is used to read back the regsiter contents. See the Microprocessor Section of this datasheet for details.

JTAG SECTION

NAME	PIN	TYPE	DESCRIPTION
ATP_TIP ATP_RING	M20 L20	I/O	**Analog Test Pin_TIP** **Analog Test Pin_RING** These pins are used to check continuity of the Transmit and Receive TIP and RING connections on the assembled board. **NOTE:** *See "Section 5.7, Analog Board Continuity Check" on page 48 for more detailed description.*
TMS	E6	I	**Test Mode Select** This pin is used as the input mode select for the boundary scan chain. **NOTE:** *Internally pulled "High" with a 50KΩ resistor.*
TCK	D5	I	**Test Clock Input** This pin is used as the input clock source for the boundary scan chain. **NOTE:** *Internally pulled "High" with a 50KΩ resistor.*
TDI	D6	I	**Test Data In** This pin is used as the input data pin for the boundary scan chain. **NOTE:** *Internally pulled "High" with a 50KΩ resistor.*
TDO	D4	O	**Test Data Out** This pin is used as the output data pin for the boundary scan chain.

JTAG SECTION

NAME	PIN	TYPE	DESCRIPTION
Analog	C2	O	**Factory Test Mode Pin** *NOTE: For Internal Use Only*
Sense	B2	O	**Factory Test Mode Pin** *NOTE: For Internal Use Only*

POWER AND GROUND

NAME	PIN	TYPE	DESCRIPTION
TVDD15 TVDD14 TVDD13 TVDD12 TVDD11 TVDD10 TVDD9 TVDD8 TVDD7 TVDD6 TVDD5 TVDD4 TVDD3 TVDD2 TVDD1 TVDD0	U11 P17 M17 M18 J18 J17 G17 D11 D10 G4 J4 J3 M3 M4 P4 U10	PWR	**Transmit Analog Power Supply (3.3V ±5%)** TVDD can be shared with DVDD. However, it is recommended that TVDD be isolated from the analog power supply RVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1μF capacitor.
RVDD1 RVDD0	F19 F2	PWR	**Receive Analog Power Supply (3.3V ±5%)** RVDD should not be shared with other power supplies. It is recommended that RVDD be isolated from the digital power supply DVDD and the analog power supply TVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1μF capacitor.
DVDD_DRV DVDD_DRV DVDD_DRV DVDD_DRV	Y1 Y20 A20 A1	PWR	**Digital Power Supply (3.3V ±5%)** DVDD should be isolated from the analog power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1μF capacitor.
DVDD_PRE DVDD_PRE DVDD_PRE DVDD_PRE DVDD DVDD DVDD DVDD DVDD_μP	V2 V19 C19 D3 E2 T2 T19 E19 Y17	PWR	**Digital Power Supply (1.8V ±5%)** DVDD should be isolated from the analog power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1μF capacitor.

POWER AND GROUND

NAME	PIN	TYPE	DESCRIPTION
AVDD_BIAS AVDD_PLL22 AVDD_PLL21 AVDD_PLL1	J20 A4 A17 Y4	PWR	**Analog Power Supply (1.8V ±5%)** AVDD should be isolated from the digital power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through at least one 0.1μF capacitor.
TGND15 TGND14 TGND13 TGND12 TGND11 TGND10 TGND9 TGND8 TGND7 TGND6 TGND5 TGND4 TGND3 TGND2 TGND1 TGND0	T12 R18 N17 L18 K18 H17 F18 E12 E9 F3 H4 K3 L3 N4 R3 T9	GND	**Transmit Analog Ground** It's recommended that all ground pins of this device be tied together.
RGND1 RGND0	R19 R2	GND	**Receive Analog Ground** It's recommended that all ground pins of this device be tied together.
DGND DGND DGND DGND	K2 L2 L19 K19	GND	**Digital Ground** It's recommended that all ground pins of this device be tied together.
DGND_DRV DGND_DRV DGND_DRV DGND_DRV DGND_PRE DGND_PRE DGND_PRE DGND_PRE DGND_μP	B1 W1 W20 B20 U3 U18 D18 E4 W16	GND	**Digital Ground** It's recommended that all ground pins of this device be tied together.
AGND_BIAS AGND_PLL22 AGND_PLL21 AGND_PLL1	K20 B5 B16 W5	GND	**Analog Ground** It's recommended that all ground pins of this device be tied together.

THERMAL GROUND

NAME	PIN	TYPE	DESCRIPTION
THGND15 THGND14 THGND13 THGND12 THGND11 THGND10 THGND9 THGND8 THGND7 THGND6 THGND5 THGND4 THGND3 THGND2 THGND1 THGND0	J9 J10 J11 J12 K9 K10 K11 K12 L9 L10 L11 L12 M9 M10 M11 M12	GND	**Thermal Ground** It's recommended that all ground pins of this device be tied together.

NO CONNECTS

NAME	PIN	TYPE	DESCRIPTION
NC	E5 F5	NC	**No Connect** These pins can be left floating or tied to ground.

2.0 CLOCK SYNTHESIZER

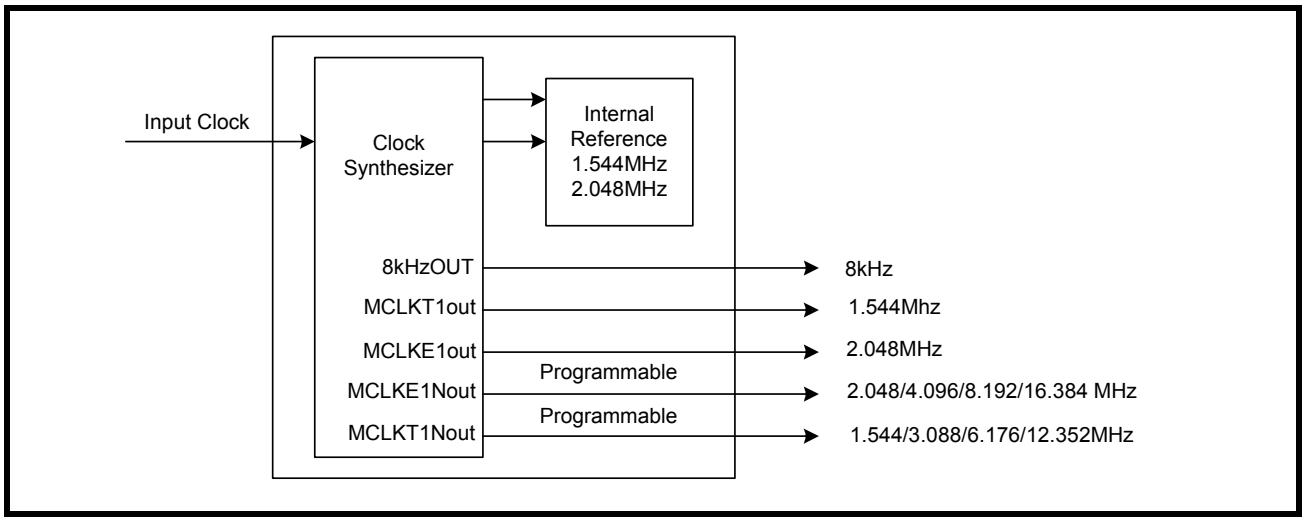
In system design, fewer clocks on the network card could reduce noise and interference. Network cards that support both T1 and E1 modes must be able to produce 1.544MHz and 2.048MHz transmission data. The XRT83VSH316 has a built in clock synthesizer that requires only one input clock reference by programming CLKSEL[3:0] in the appropriate global register. A list of the input clock options is shown in Table 1.

TABLE 1: INPUT CLOCK SOURCE SELECT

CLKSEL[3:0]	INPUT CLOCK REFERENCE
0h (0000)	2.048 MHz
1h (0001)	1.544MHz
8h (1000)	4.096 MHz
9h (1001)	3.088 MHz
Ah (1010)	8.192 MHz
Bh (1011)	6.176 MHz
Ch (1100)	16.384 MHz
Dh (1101)	12.352 MHz
Eh (1110)	2.048 MHz
Fh (1111)	1.544 MHz

The single input clock reference is used to generate multiple timing references. The first objective of the clock synthesizer is to generate 1.544MHz and 2.048MHz for each of the 16 channels. This allows each channel to operate in either T1 or E1 mode independent from the other channels. The state of the equalizer control bits in the appropriate channel registers determine whether the LIU operates in T1 or E1 mode. The second objective is to generate additional output clock references for system use. The available output clock references are shown in Figure 2.

FIGURE 2. SIMPLIFIED BLOCK DIAGRAM OF THE CLOCK SYNTHESIZER

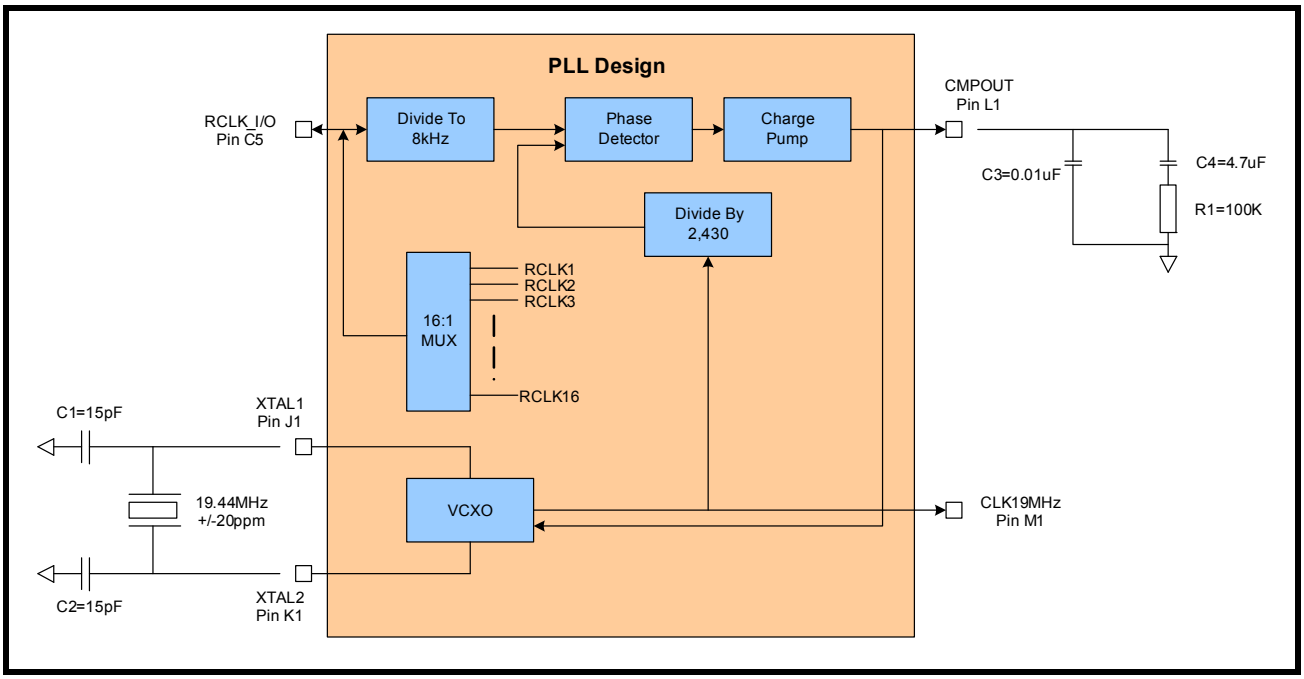


2.1 19.44MHz Output Clock Reference for Recovered Clock Synchronization

For Loop Timing Applications, the EXAR 16-channel LIIU can provide a SONET 19.44MHz clock reference that is synchronized to one of the recovered line clocks from the T1 or E1 line interface or to an externally supplied reference clock. Figure 3 below shows a simplified block diagram with recommend components for this feature. The external crystall connected to XTAL1 and XTAL2 should have a minimum accuracy of +/-20ppm if it is to be used as a SONET/SDH clock reference. The two filtering caps, C1 and C2 are recommendations only. The value of these caps will depend on the system characteristics of the PCB, but should range from 10pf to 20pf.

If RCLK_I/O is configured as an output, it will be connected to one of the 16 channel recovered line clocks. In addition, the recovered line clock that is selected will be used as the reference for the 19.44MHz SONET/SDH output clock. If RCLK_I/O is configured as an input, an external reference clock will be used to derive the 19.44MHz output clock.

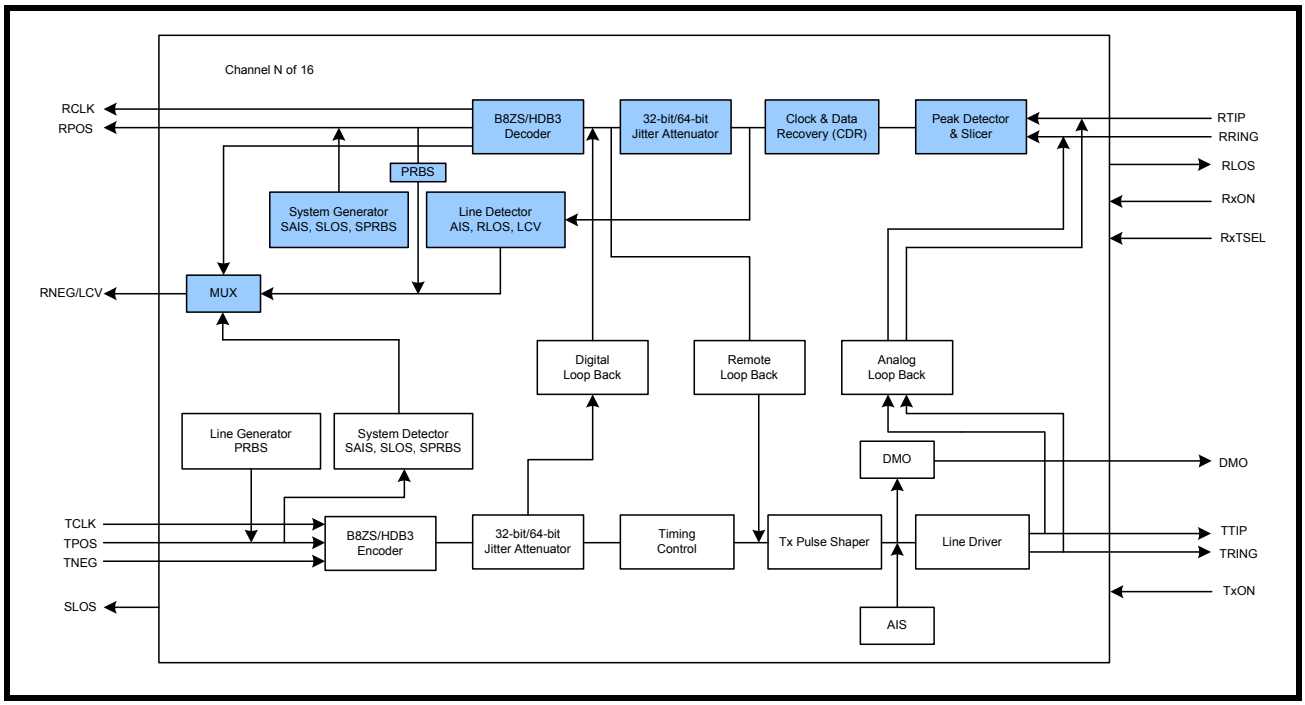
FIGURE 3. 19.44MHZ OUTPUT CLOCK REFERENCE



3.0 RECEIVE PATH LINE INTERFACE

The receive path of the XRT83VSH316 LIU consists of 16 independent T1/E1/J1 receivers. The following section describes the complete receive path from RTIP/RRING inputs to RCLK/RPOS/RNEG outputs. If any of the diagnostic detection features are used, the LIU must be set in Single Rail mode. Since, the receive path has system diagnostic generators, the part will automatically be placed in Singe Rail Mode whenever one of the diagnostic patterns is used. A simplified block diagram of the receive and transmit path is shown in Figure 4.

FIGURE 4. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE PATH



3.1 Line Termination (RTIP/RRING)

3.1.1 Internal Termination

The input stage of the receive path accepts standard T1/E1/J1 twisted pair or E1 coaxial cable inputs through RTIP and RRING. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for all modes of operation reducing the number of external components necessary in system design. The receive termination impedance (along with the transmit impedance) is selected by programming TERSEL[1:0] to match the line impedance. Selecting the internal impedance is shown in Table 2.

TABLE 2: SELECTING THE INTERNAL IMPEDANCE

TERSEL[1:0]	TRANSMISSION TERMINATION
0h (00)	100Ω
1h (01)	110Ω
2h (10)	75Ω
3h (11)	120Ω

The XRT83VSH316 has the ability to switch the internal termination to "High" impedance by programming RxTSEL in the appropriate channel register. For internal termination, set RxTSEL to "1". By default, RxTSEL is set to "0" ("High" impedance). For redundancy applications, a dedicated hardware pin (RxTSEL) is also available to control the receive termination for all channels simultaneously. This hardware pin takes priority over the register setting if RxTCNTL is set to "1" in the appropriate global register. If RxTCNTL is set to "0", the state of this pin is ignored. See Figure 5 for a typical connection diagram using the internal termination.

FIGURE 5. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION

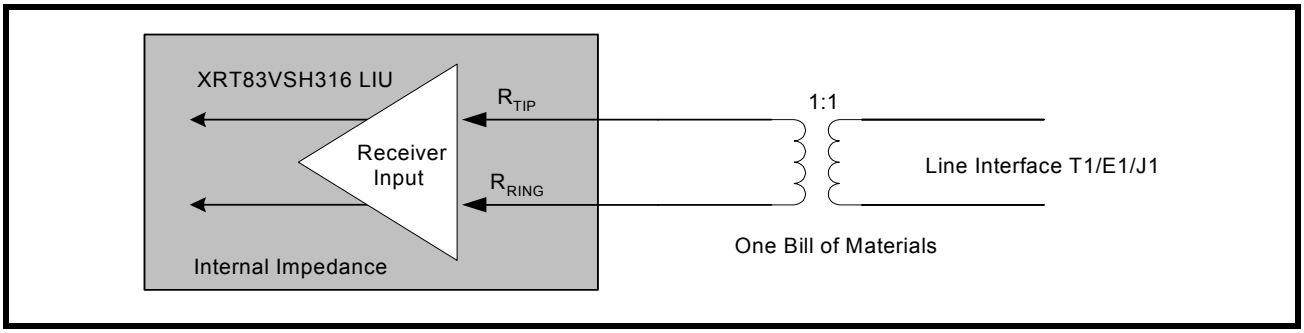


TABLE 3: RECEIVE TERMINATIONS

RXTSEL	TERSEL1	TERSEL0	RXRES1	RXRES0	R_{ext}	R_{int}	MODE
0	x	x	x	x	R_{ext}	∞	T1/E1/J1
1	0	0	0	0	∞	100Ω	T1
1	0	1	0	0	∞	110Ω	J1
1	1	0	0	0	∞	75Ω	E1
1	1	1	0	0	∞	120Ω	E1
1	0	0	0	1	240Ω	172Ω	T1
1	0	1	0	1	240Ω	204Ω	J1
1	1	0	0	1	240Ω	108Ω	E1
1	1	1	0	1	240Ω	240Ω	E1
1	0	0	1	0	210Ω	192Ω	T1
1	0	1	1	0	210Ω	232Ω	J1
1	1	0	1	0	210Ω	116Ω	E1
1	1	1	1	0	210Ω	280Ω	E1
1	0	0	1	1	150Ω	300Ω	T1
1	0	1	1	1	150Ω	412Ω	J1
1	1	0	1	1	150Ω	150Ω	E1
1	1	1	1	1	150Ω	600Ω	E1

3.2 Clock and Data Recovery

The receive clock (RCLK) is recovered by the clock and data recovery circuitry. An internal PLL locks on the incoming data stream and outputs a clock that's in phase with the incoming signal. This allows for multi-channel T1/E1/J1 signals to arrive from different timing sources and remain independent. In the absence of an incoming signal, RCLK maintains its timing by using the internal master clock as its reference. The recovered data can be updated on either edge of RCLK. By default, data is updated on the rising edge of RCLK. To update data on the falling edge of RCLK, set RCLKE to "1" in the appropriate global register. Figure 6 is a timing diagram of the receive data updated on the rising edge of RCLK. Figure 7 is a timing diagram of the receive data updated on the falling edge of RCLK. The timing specifications are shown in Table 4.

FIGURE 6. RECEIVE DATA UPDATED ON THE RISING EDGE OF RCLK

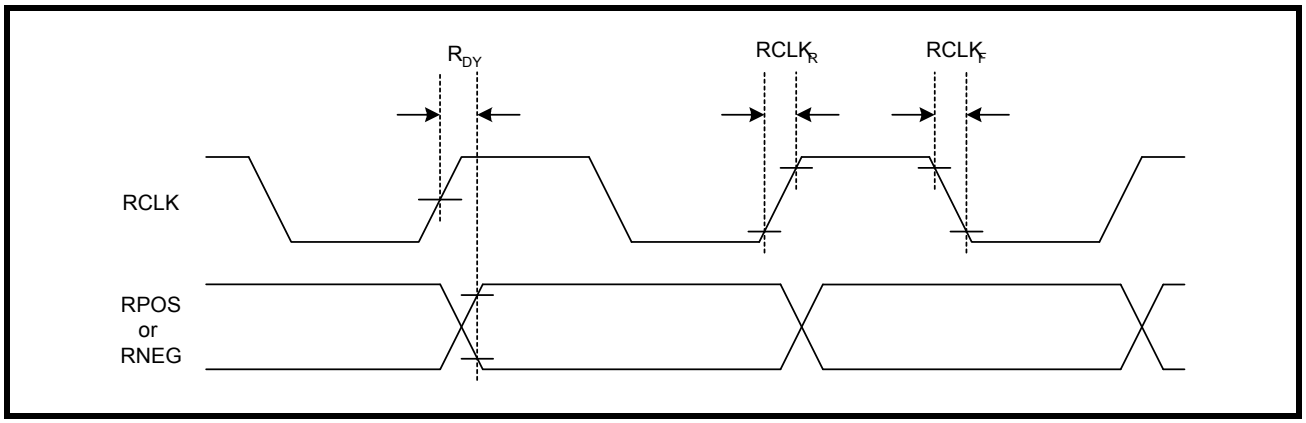


FIGURE 7. RECEIVE DATA UPDATED ON THE FALLING EDGE OF RCLK

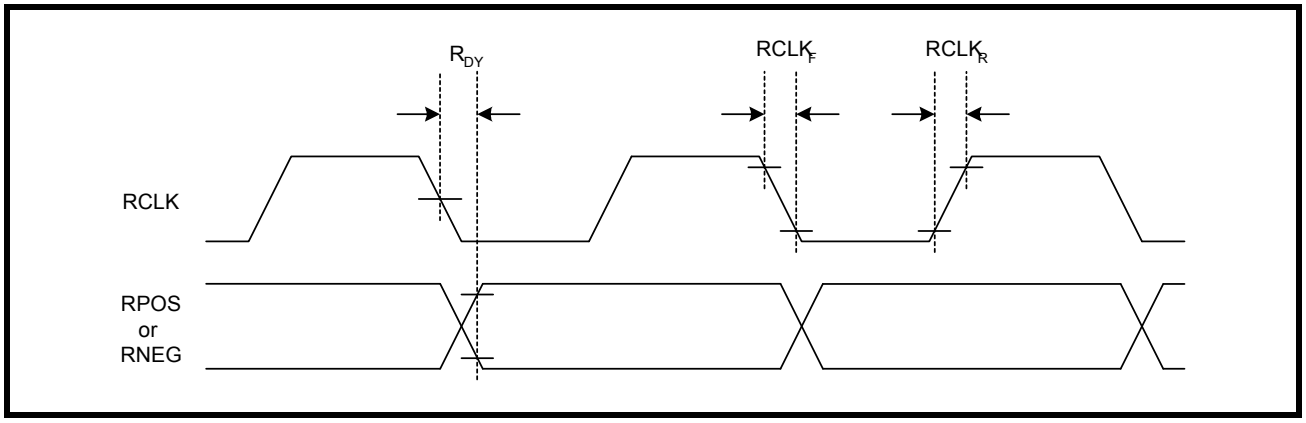


TABLE 4: TIMING SPECIFICATIONS FOR RCLK/RPOS/RNEG

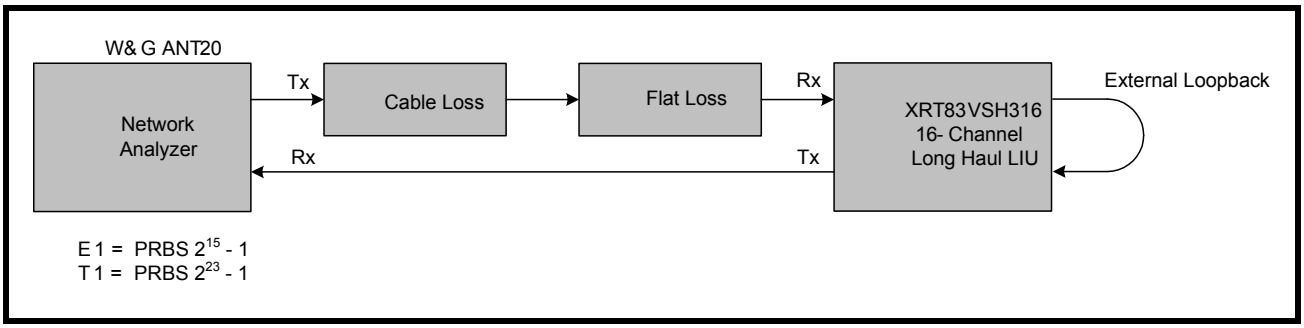
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
RCLK Duty Cycle	R_{CDU}	45	50	55	%
RCLK to Data Delay	R_{DY}	-	-	40	ns
RCLK Rise Time (10% to 90%) with 25pF Loading	$RCLK_R$	-	-	40	ns
RCLK Fall Time (90% to 10%) with 25pF Loading	$RCLK_F$	-	-	40	ns

NOTE: *VDD=3.3V ±5%, VDDc=1.8V ±5%, T_A=25°C, Unless Otherwise Specified*

3.3 Receive Sensitivity

To meet short haul requirements, the XRT83VSH316 can accept T1/E1/J1 signals that have been attenuated by 12dB of flat loss in E1 or 655ft of cable loss plus 6db of flat loss in T1/J1 mode. Although data integrity is maintained, the RLOS function (if enabled) will report an RLOS condition according to the receiver loss of signal section in this datasheet. The test configuration for measuring the receive sensitivity is shown in Figure 8.

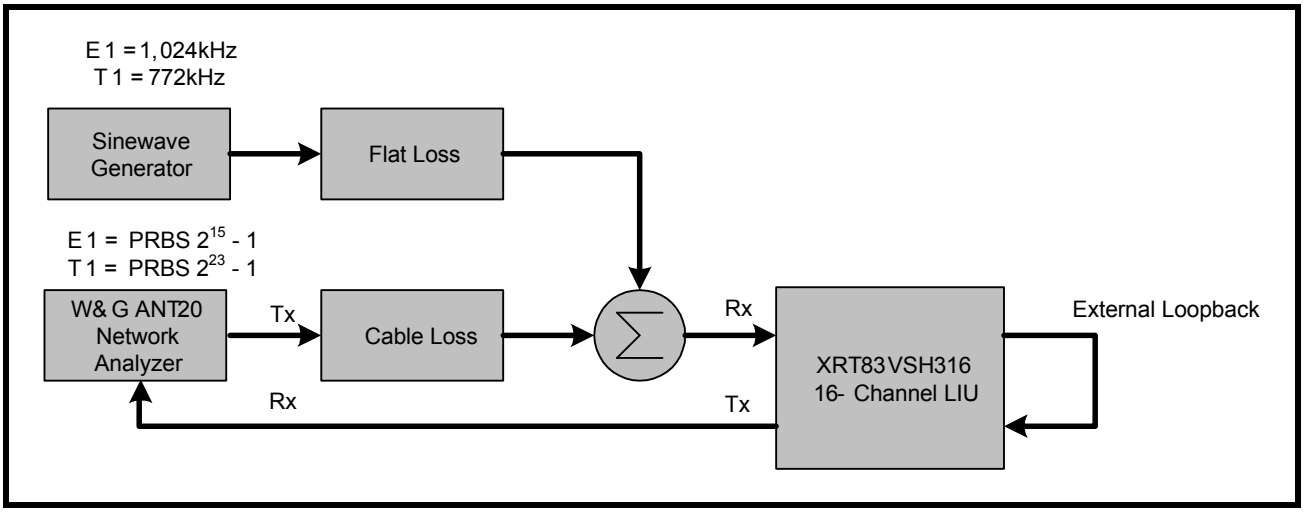
FIGURE 8. TEST CONFIGURATION FOR MEASURING RECEIVE SENSITIVITY



3.4 Interference Margin

The test configuration for measuring the interference margin is shown in Figure 9.

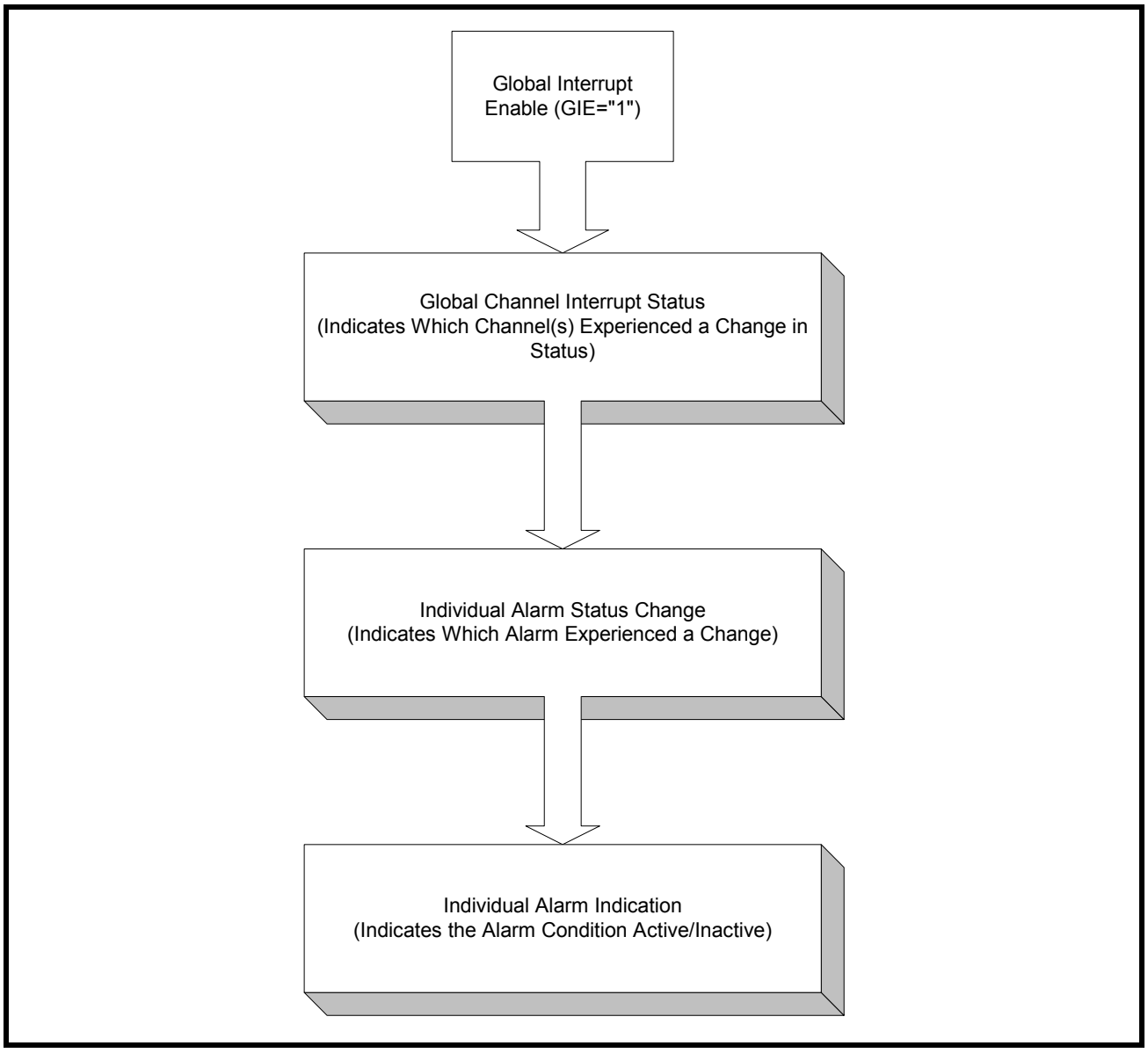
FIGURE 9. TEST CONFIGURATION FOR MEASURING INTERFERENCE MARGIN



3.5 General Alarm Detection and Interrupt Generation

The receive path and transmit path detect RLOS/SLOS, AIS/SAIS, PRBS/SPRBS, and Line Side LCV and DMO. These alarms can be individually masked to prevent the alarm from triggering an interrupt. To enable interrupt generation, the Global Interrupt Enable (GIE) bit must be set "High" in the appropriate global register. Any time a change in status occurs (it the alarms are enabled), the interrupt pin will pull "Low" to indicate an alarm has occurred. Once the status registers have been read, the INT pin will return "High". The status registers are Reset Upon Read (RUR). The interrupts are categorized in a hierarchical process block. Figure 10 is a simplified block diagram of the interrupt generation process.

FIGURE 10. INTERRUPT GENERATION PROCESS BLOCK



NOTE: *The interrupt pin is an open-drain output that requires a 10kΩ external pull-up resistor.*

3.6 Receive Diagnostic Pattern Detection

The receive path has the ability to detect diagnostic patterns on the line side interface from the RTip/RRing input pins (Single Rail Mode Only). The LIU can detect an All Ones (SAIS), Loss of Signal (RLOS), PRBS/QRSS (SPRBS), or Line Code Violations (LCV).

3.6.1 RLOS (Receiver Loss of Signal, Line Side)

The XRT83VSH316 supports both G.775 or ETSI-300-233 RLOS detection scheme.

In G.775 mode, LOS is declared when the received signal is less than 375mV for 32 consecutive pulse periods (typical). The device clears LOS when the receive signal achieves 12.5% ones density with no more than 15 consecutive zeros in a 32 bit sliding window and the signal level exceeds 425mV (typical).

In ETSI-300-233 mode the device declares LOS when the input level drops below 375mV (typical) for more than 2048 pulse periods (1msec).

The device exits LOS when the input signal exceeds 425mV (typical) and has transitions for more than 32 pulse periods with 12.5% ones density with no more than 15 consecutive zero's in a 32 bit sliding window.

In T1 mode RLOS is declared when the received signal is less than 320mV for 175 consecutive pulse period (typical). The device clears RLOS when the receive signal achieves 12.5% ones density with no more than 100 consecutive zeros in a 128 bit sliding window and the signal level exceeds 425mV (typical).

3.6.2 EXLOS (Extended Loss of Signal)

By enabling the extended loss of signal by programming the appropriate channel register, the digital LOS is extended to count 4,096 consecutive zeros before declaring LOS in T1 and E1 mode. By default, EXLOS is disabled and LOS operates in normal mode.

3.6.3 AIS (Alarm Indication Signal, Line Side)

The XRT83VSH316 adheres to the ITU-T G.775 specification for an all ones pattern. The alarm indication signal is set to "1" if an all ones pattern (at least 99.9% ones density) is present for T, where T is 3ms to 75ms in T1 mode. AIS will clear when the ones density is not met within the same time period T. In E1 mode, the AIS is set to "1" if the incoming signal has 2 or less zeros in a 512-bit window. AIS will clear when the incoming signal has 3 or more zeros in the 512-bit window.

3.6.4 FLSD (FIFO Limit Status Detection)

The purpose of the FIFO limit status is to indicate when the Read and Write FIFO pointers are within a pre-determined range (over-flow or under-flow indication). The FLSD is set to "1" if the FIFO Read and Write Pointers are within ±3-Bits.

3.6.5 LCV (Line Code Violation Detection, Line Side Only)

The LIU contains 16 independent, 16-bit LCV counters. When the counters reach full-scale, they remain saturated at 0xFFFFh until they are reset globally or on a per channel basis. For performance monitoring, the counters can be updated globally or on a per channel basis to place the contents of the counters into holding registers. The LIU uses an indirect address bus to access a counter for a given channel. Once the contents of the counters have been placed in holding registers, they can be individually read.

The LCV_OF bit supports monitoring of Line Code violations or Over Flow status of the LCV counters. By default, the LCV_OF bit monitors the Line Code Violations and will be set to a "1" if the receiver is currently detecting line code violations or excessive zeros for HDB3 (E1 mode) or B8ZS (T1 mode). In AMI mode, the LCV_OF will be set to a "1" if the receiver is currently detecting bipolar violations or excessive zeros. However, if the LIU is configured to monitor the 16-bit LCV counter, the LCV_OF will be set to a "1" if the counter saturates.

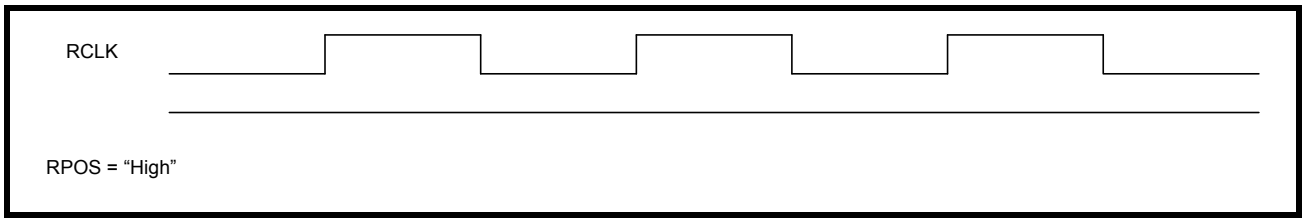
3.7 Receive Diagnostic Pattern Generation

The receive path has the ability to generate diagnostic patterns to the system side interface on the RPOS output pin (Single Rail Mode Only). The LIU can generate an All Ones (SAIS), All Zeros (SLOS), or PRBS/ QRSS (SPRBS) signal.

3.7.1 System Side AIS (SAIS)

The system side SAIS signal is an all ones pattern sent to the RPOS output pin. This diagnostic pattern is created by pulling RPOS "High" for the duration it's enabled.

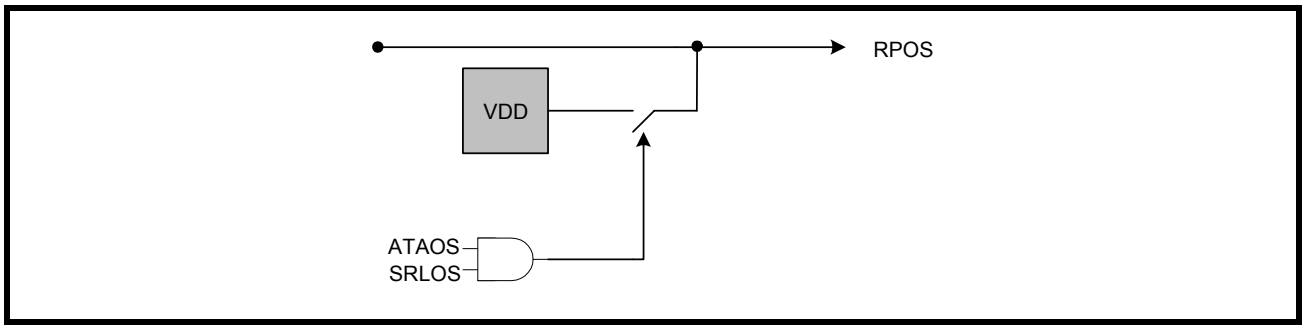
FIGURE 11. SYSTEM SIDE SAIS RECEIVE OUTPUT



3.7.2 ATAOS (System Automatic Transmit All Ones)

If ATAOS is selected by programming the appropriate global register, an all ones signal will be output to RPOS for each channel that experiences a SRLOS condition. If SLOS does not occur, the ATAOS will remain inactive until a SRLOS on a given channel occurs. A simplified block diagram of the ATAOS function is shown in Figure 12.

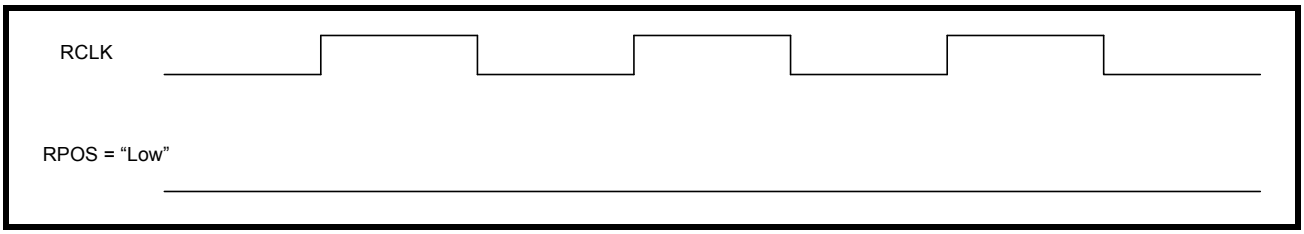
FIGURE 12. SIMPLIFIED BLOCK DIAGRAM OF THE ATAOS FUNCTION



3.7.3 System Side LOS (SLOS)

The system side SLOS signal is an all zeros pattern sent to the RPOS output pin. This diagnostic pattern is created by pulling RPOS "Low" for the duration it's enabled.

FIGURE 13. SYSTEM SIDE SLOS RECEIVE OUTPUT



3.8 System Side SPRBS Receive Output

The system side SPRBS/SQRSS signal is a Pseudo Random Bit Sequence or Quasi Random Bit Sequence with the following polynomials.

TABLE 5: RANDOM BIT SEQUENCE POLYNOMIALS

RANDOM PATTERN	T1	E1
SQRSS	$2^{20} - 1$	$2^{20} - 1$
SPRBS	$2^{15} - 1$	$2^{15} - 1$

3.9 Jitter Attenuator (If enabled in the Receive Path)

The receive jitter attenuator reduces phase and frequency jitter in the recovered clock if it is enabled. The jitter attenuator uses a data FIFO (First In First Out) with a programmable depth of 32-bit or 64-bit. If the LIU is used for line synchronization (loop timing systems), the JA should be enabled in the receive path. When the Read and Write pointers of the FIFO are within 2-Bits of over-flowing or under-flowing, the bandwidth of the jitter attenuator is widened to track the short term input jitter, thereby avoiding data corruption. When this condition occurs, the jitter attenuator will not attenuate input jitter until the Read/Write pointer's position is outside the 2-Bit window. In T1 mode, the bandwidth of the JA is always set to 3Hz. In E1 mode, the bandwidth is programmable to either 10Hz or 1.5Hz (1.5Hz automatically selects the 64-Bit FIFO depth). The JA has a clock delay equal to ½ of the FIFO bit depth.

NOTE: If the LIU is used in a multiplexer/mapper application where stuffing bits are typically removed, the jitter attenuator can be placed in the transmit path to smooth out the gapped clock. See the Transmit Section of this datasheet.

3.10 HDB3/B8ZS Decoder

In single rail mode, RPOS can decode AMI or HDB3/B8ZS signals. For E1 mode, HDB3 is defined as any block of 4 successive zeros replaced with 000V or B00V, so that two successive V pulses are of opposite polarity to prevent a DC component. In T1 mode, 8 successive zeros are replaced with 000VB0VB. If the HDB3/B8ZS decoder is selected, the receive path removes the V and B pulses so that the original data is output to RPOS.

3.10.0.1 RPOS/RNEG/RCLK

The digital output data can be programmed to either single rail or dual rail formats. Figure 14 is a timing diagram of a repeating "0011" pattern in single-rail mode. Figure 15 is a timing diagram of the same fixed pattern in dual rail mode.

FIGURE 14. SINGLE RAIL MODE WITH A FIXED REPEATING "0011" PATTERN

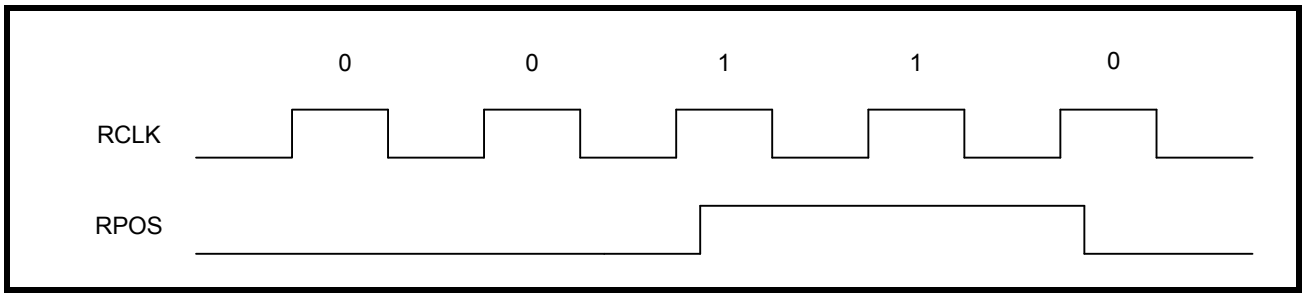
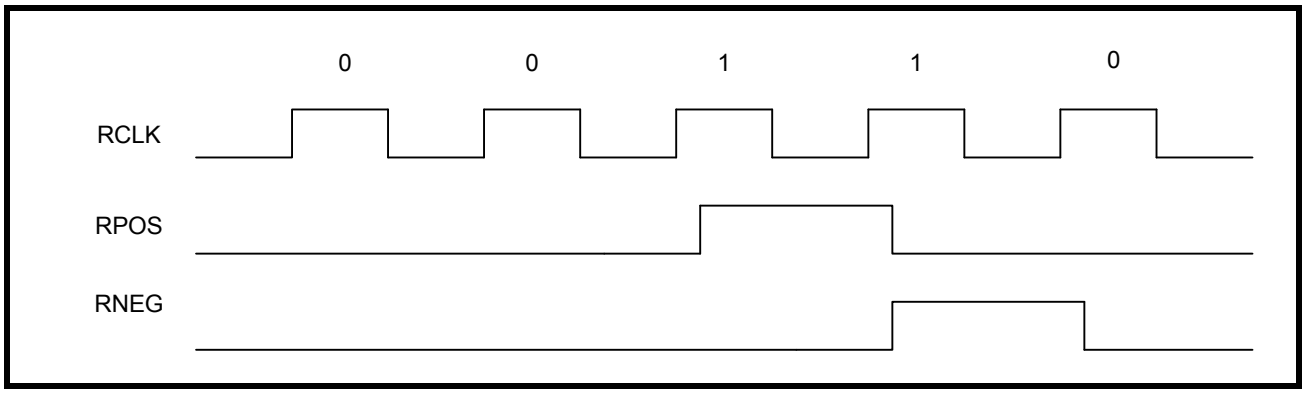


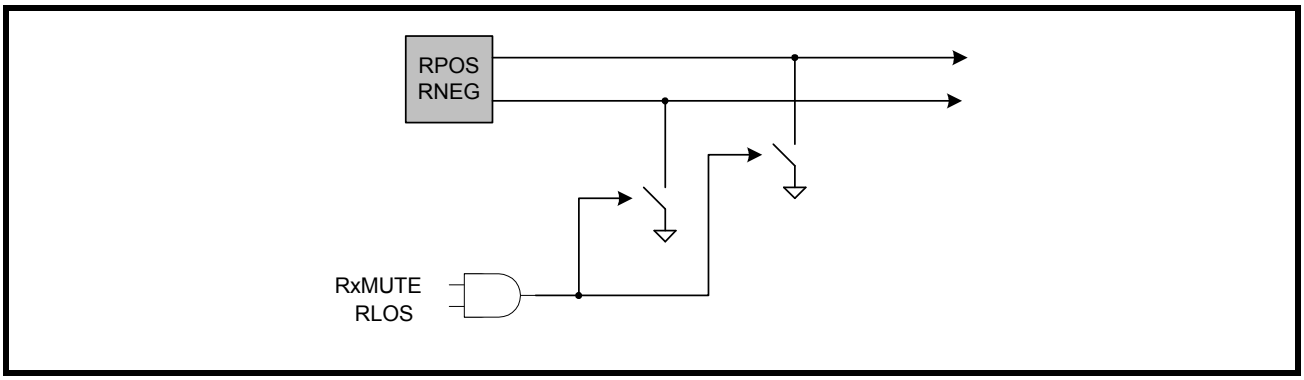
FIGURE 15. DUAL RAIL MODE WITH A FIXED REPEATING "0011" PATTERN



3.11 RxMUTE (Receiver LOS with Data Muting, Line Side Only)

The receive muting function can be selected by setting RxMUTE to "1" in the appropriate global register. If selected, any channel that experiences an RLOS condition on the line side will automatically pull RPOS and RNEG "Low" to prevent data chattering. If RLOS does not occur, the RxMUTE will remain inactive until an RLOS on a given channel occurs. The default setting for RxMUTE is "0" which is disabled. A simplified block diagram of the RxMUTE function is shown in Figure 16.

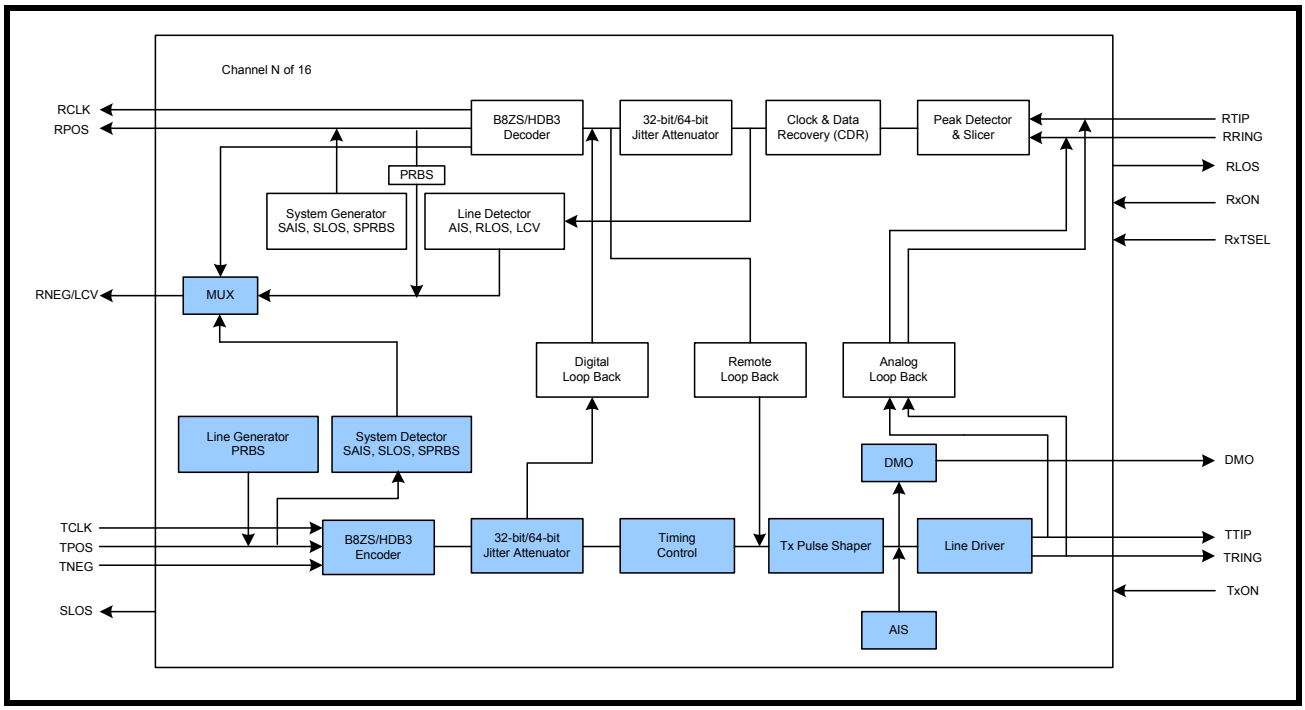
FIGURE 16. SIMPLIFIED BLOCK DIAGRAM OF THE RXMUTE FUNCTION



4.0 TRANSMIT PATH LINE INTERFACE

The transmit path of the XRT83VSH316 LIU consists of 16 independent T1/E1/J1 transmitters. The following section describes the complete transmit path from TCLK/TPOS/TNEG inputs to TTIP/TRING outputs. If any of the diagnostic detection features are used, the LIU must be set in Single Rail mode. Since, the transmit path has line side diagnostic generators, the part will automatically be placed in Singe Rail Mode whenever one of the diagnostic patterns is used. A simplified block diagram of the transmit and receive path is shown in Figure 17.

FIGURE 17. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT PATH



4.1 TCLK/TPOS/TNEG Digital Inputs

In dual rail mode, TPOS and TNEG are the digital inputs for the transmit path. In single rail mode, TNEG has no function and can be left unconnected. The XRT83VSH316 can be programmed to sample the inputs on either edge of TCLK. By default, data is sampled on the falling edge of TCLK. To sample data on the rising edge of TCLK, set TCLKE to "1" in the appropriate global register. Figure 18 is a timing diagram of the transmit input data sampled on the falling edge of TCLK. Figure 19 is a timing diagram of the transmit input data sampled on the rising edge of TCLK. The timing specifications are shown in Table 6.

FIGURE 18. TRANSMIT DATA SAMPLED ON FALLING EDGE OF TCLK

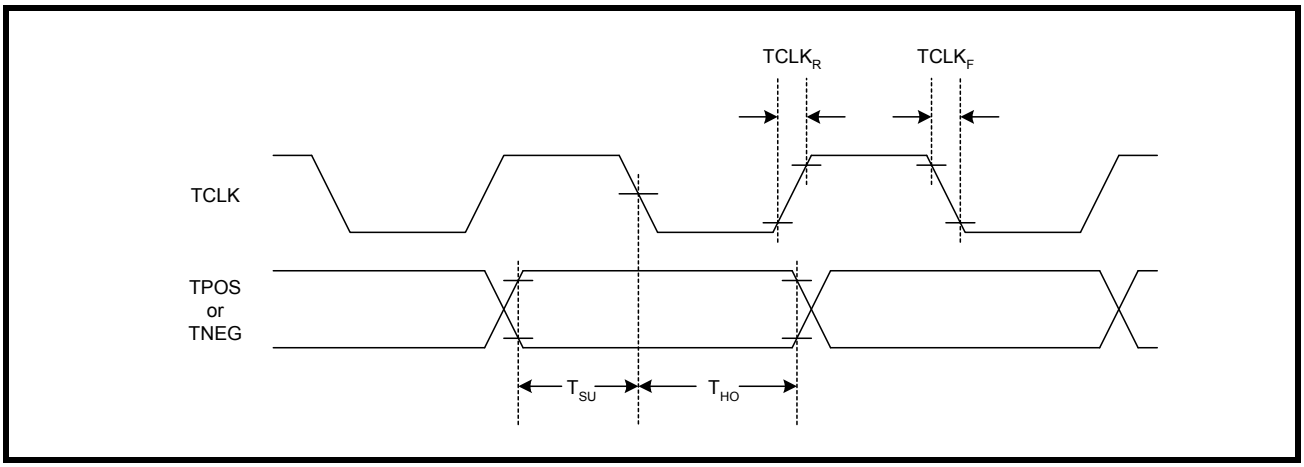


FIGURE 19. TRANSMIT DATA SAMPLED ON RISING EDGE OF TCLK

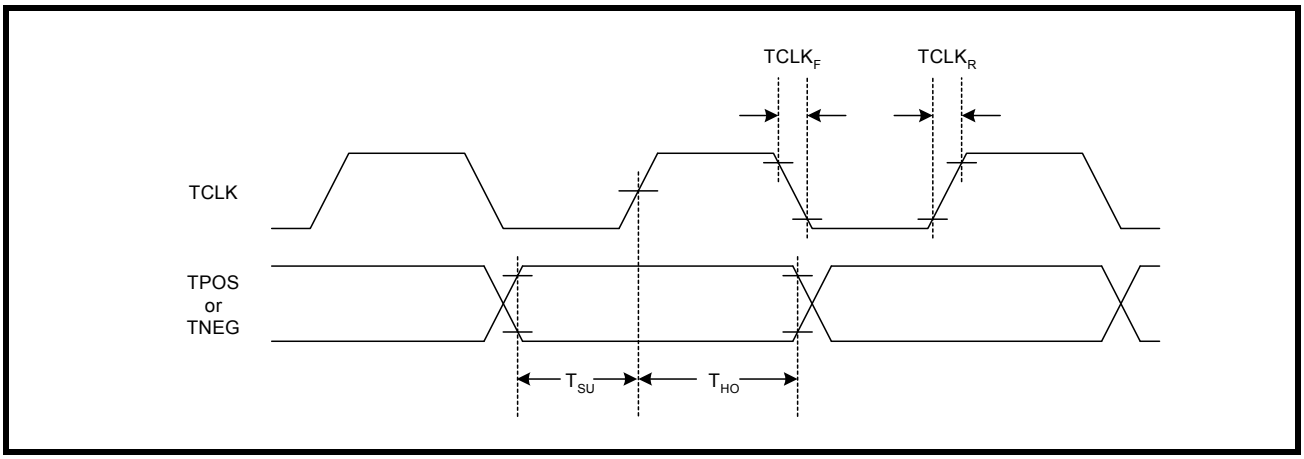


TABLE 6: TIMING SPECIFICATIONS FOR TCLK/TPOS/TNEG

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
TCLK Duty Cycle	T_{CDU}	30	50	70	%
Transmit Data Setup Time	T_{SU}	50	-	-	ns
Transmit Data Hold Time	T_{HO}	30	-	-	ns
TCLK Rise Time (10% to 90%)	$TCLK_R$	-	-	40	ns
TCLK Fall Time (90% to 10%)	$TCLK_F$	-	-	40	ns

NOTE: *VDD=3.3V ±5%, VDDc=1.8V ±5%, T_A=25°C, Unless Otherwise Specified*

4.2 HDB3/B8ZS Encoder

In single rail mode, the LIU can encode the TPOS input signal to AMI or HDB3/B8ZS data. In E1 mode and HDB3 encoding selected, any sequence with four or more consecutive zeros in the input will be replaced with 000V or B00V, where "B" indicates a pulse conforming to the bipolar rule and "V" representing a pulse violating the rule. An example of HDB3 encoding is shown in Table 7. In T1 mode and B8ZS encoding selected, an input data sequence with eight or more consecutive zeros will be replaced using the B8ZS encoding rule. An example with Bipolar with 8 Zero Substitution is shown in Table 8.

TABLE 7: EXAMPLES OF HDB3 ENCODING

	NUMBER OF PULSES BEFORE NEXT 4 ZEROS	
Input		0000
HDB3 (Case 1)	Odd	000V
HDB3 (Case 2)	Even	B00V

TABLE 8: EXAMPLES OF B8ZS ENCODING

CASE	PRECEDING PULSE	NEXT 8 BITS
Case 1		
Input	+	00000000
B8ZS		000VB0VB
AMI Output	+	000+-0-+
Case 2		
Input	-	00000000
B8ZS		000VB0VB
AMI Output	-	000-+0+-

4.3 Jitter Attenuator (If enabled in the Transmit Path)

The XRT83VSH316 LIU is ideal for multiplexer or mapper applications where the network data crosses multiple timing domains. As the higher data rates are de-multiplexed down into T1 or E1 data, stuffing bits are typically removed which can leave gaps in the incoming data stream. The transmit jitter attenuator can be enabled with a 32-Bit or 64-Bit FIFO that is used to smooth the gapped clock into a steady T1 or E1 output. The maximum gap width of the 16-Channel LIU is shown in Table 9.

TABLE 9: MAXIMUM GAP WIDTH FOR MULTIPLEXER/MAPPER APPLICATIONS

FIFO DEPTH	MAXIMUM GAP WIDTH
32-Bit	20 UI
64-Bit	50 UI

NOTE: *If the LIU is used in a loop timing system, the jitter attenuator can be placed in the receive path. See the Receive Section of this datasheet.*

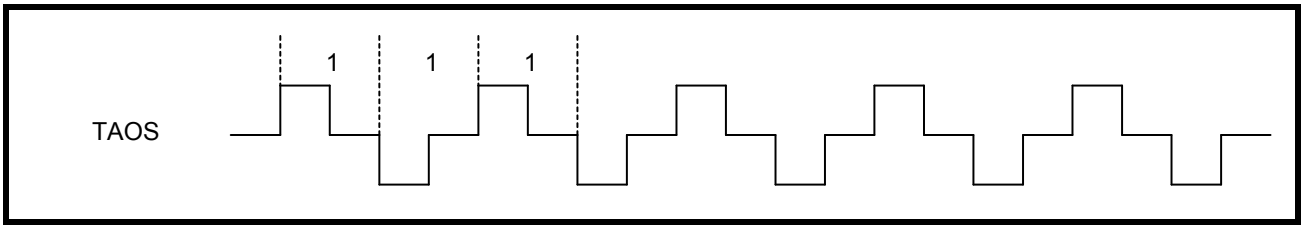
4.4 Transmit Diagnostic Pattern Generation

The transmit path has the ability to generate diagnostic patterns to the line side interface on the TTip/TRing output pins (Single Rail Mode Only). The LIU can generate an All Ones (AIS) or PRBS/QRSS (PRBS) signal.

4.4.1 Line Side AIS (Transmit All Ones)

The XRT83VSH316 has the ability to transmit all ones on a per channel basis by programming the appropriate channel register. The AIS signal is generated on TTip and TRing.

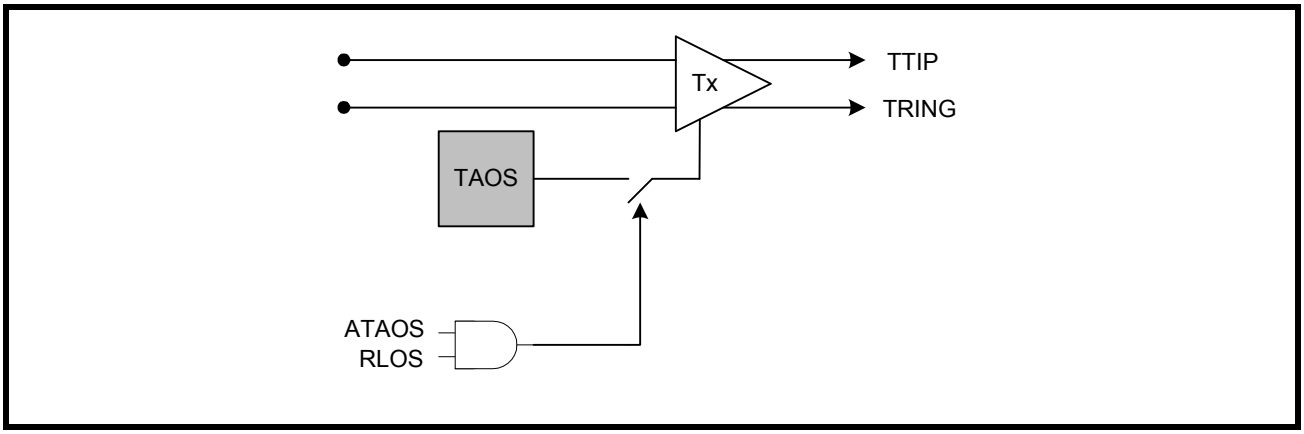
FIGURE 20. TAOS (TRANSMIT ALL ONES)



4.4.2 ATAOS (Automatic Transmit All Ones)

If ATAOS is selected by programming the appropriate global register, an AMI all ones signal will be transmitted for each channel that experiences an RLOS condition. If RLOS does not occur, the ATAOS will remain inactive until an RLOS on a given channel occurs. A simplified block diagram of the ATAOS function is shown in Figure 21.

FIGURE 21. SIMPLIFIED BLOCK DIAGRAM OF THE ATAOS FUNCTION



4.4.3 Line Side PRBS/QRSS (Pseudo/Quasi Random Bit Sequence)

The XRT83VSH316 can transmit a PRBS/QRSS random sequence to a remote location from the TTip/TRing output pins. To select PRBS or QRSS, see the register map for programming details. The polynomial is shown in Table 10.

TABLE 10: RANDOM BIT SEQUENCE POLYNOMIALS

RANDOM PATTERN	T1	E1
QRSS	$2^{20} - 1$	$2^{20} - 1$
PRBS	$2^{15} - 1$	$2^{15} - 1$

4.5 Transmit Diagnostic Pattern Detection

The transmit path has the ability to detect diagnostic patterns on the system side interface from the TPOS input pin (Single Rail Mode Only). The LIU can detect an All Ones (SAIS), Loss of Signal (RLOS), or PRBS/QRSS (SPRBS).

4.5.1 SLOS (System Loss of Signal)

The XRT83VSH316 supports both G.775 or ETSI-300-233 RLOS detection scheme.

In G.775 mode, LOS is declared when the received signal is less than 375mV for 32 consecutive pulse periods (typical). The device clears LOS when the receive signal achieves 12.5% ones density with no more than 15 consecutive zeros in a 32 bit sliding window and the signal level exceeds 425mV (typical).

In ETSI-300-233 mode the device declares LOS when the input level drops below 375mV (typical) for more than 2048 pulse periods (1msec).

The device exits LOS when the input signal exceeds 425mV (typical) and has transitions for more than 32 pulse periods with 12.5% ones density with no more than 15 consecutive zero's in a 32 bit sliding window.

In T1 mode RLOS is declared when the received signal is less than 320mV for 175 consecutive pulse period (typical). The device clears RLOS when the receive signal achieves 12.5% ones density with no more than 100 consecutive zeros in a 128 bit sliding window and the signal level exceeds 425mV (typical).

4.5.2 SYS_EXLOS (System Extended Loss of Signal)

By enabling the system extended loss of signal by programming the appropriate channel register, the digital SLOS is extended to count 4,096 consecutive zeros before declaring SLOS in T1 and E1 mode. By default, EXLOS is disabled and SLOS operates in normal mode.

4.5.3 SAIS (System Alarm Indication Signal)

The XRT83VSH316 adheres to the ITU-T G.775 specification for an all ones pattern. The alarm indication signal is set to "1" if an all ones pattern (at least 99.9% ones density) is present for T, where T is 3ms to 75ms in T1 mode. AIS will clear when the ones density is not met within the same time period T. In E1 mode, the AIS is set to "1" if the incoming signal has 2 or less zeros in a 512-bit window. AIS will clear when the incoming signal has 3 or more zeros in the 512-bit window.

4.6 Transmit Pulse Shaper and Filter

If TCLK is not present, pulled "Low", or pulled "High" the transmitter outputs at TTIP/TRING will automatically send an all ones or an all zero signal to the line by programming the appropriate global register. By default, the transmitters will send all zeros. To send all ones, the TCLKCNL bit must be set "High" in the appropriate global register.

4.6.1 T1 Short Haul Line Build Out (LBO)

The short haul transmitter output pulses are generated using a 7-Bit internal DAC (6-Bit plus the MSB sign bit). The line build out can be set to interface to five different ranges of cable attenuation by programming the appropriate channel register. The pulse shape is divided into eight discrete time segments which are set to fixed values to comply with the pulse template. The short haul LBO settings are shown in Table 11.

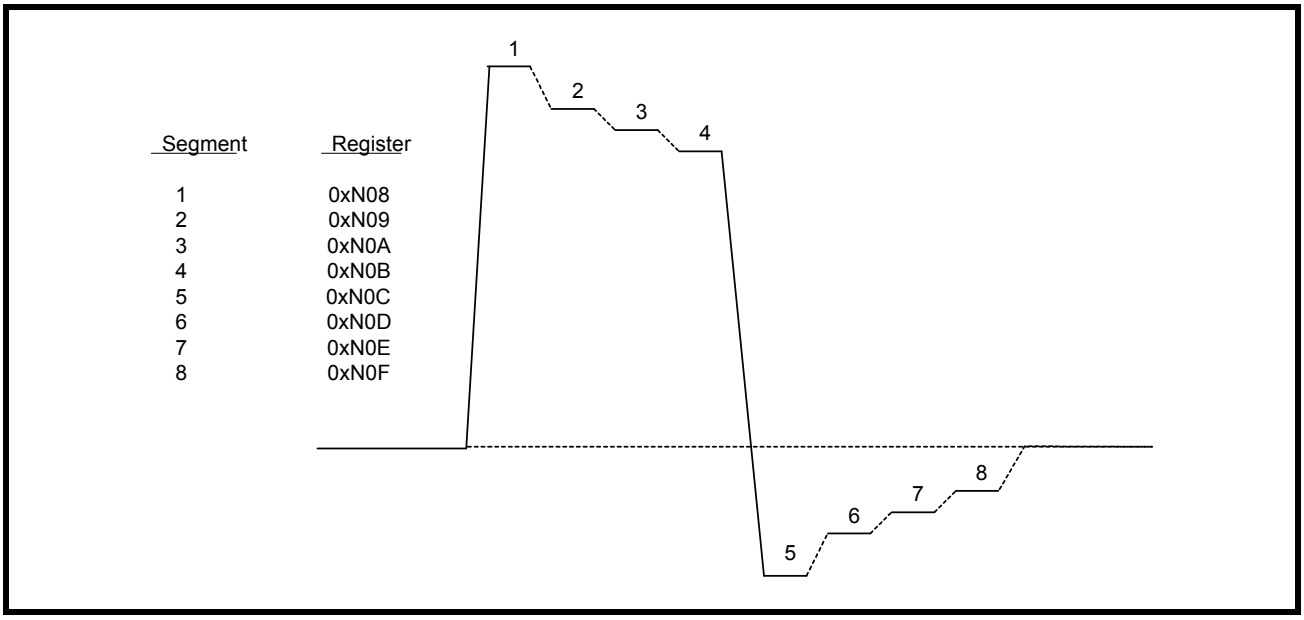
TABLE 11: SHORT HAUL LINE BUILD OUT

LBO SETTING EQC[4:0]	RANGE OF CABLE ATTENUATION
08h (01000)	0 - 133 Feet
09h (01001)	133 - 266 Feet
0Ah (01010)	266 - 399 Feet
0Bh (01011)	399 - 533 Feet
0Ch (01100)	533 - 655 Feet

4.6.2 Arbitrary Pulse Generator For T1 and E1

The arbitrary pulse generator divides the pulse into eight individual segments. Each segment is set by a 7-Bit binary word by programming the appropriate channel register. This allows the system designer to set the overshoot, amplitude, and undershoot for a unique line build out. The MSB (bit 7) is a sign-bit. If the sign-bit is set to "0", the segment will move in a positive direction relative to a flat line (zero) condition. If this sign-bit is set to "1", the segment will move in a negative direction relative to a flat line condition. The resolution of the DAC is typically 45mV per LSB. Thus, writing 7-bit = 1111111 will clamp the output at either voltage rail corresponding to a maximum amplitude. A pulse with numbered segments is shown in Figure 22.

FIGURE 22. ARBITRARY PULSE SEGMENT ASSIGNMENT



NOTE: By default, the arbitrary segments are programmed to 0x00h. The transmitter outputs will result in an all zero pattern to the line interface.

4.6.3 Setting Registers to select an Aribtrary Pulse

For T1: Address:0xN00 hex, bits D[4:0]

For E1: Address: 0xN03 hex, bit D3

To program the transmit output pulse, once the arbitrary pulse has been selected, write the appropriate values into the segment registers in Table 12.

The transmit output pulse is divided into eight individual segments. Segment 1 corresponds to the beginning of the pulse and segment 8 to the end of the pulse. The value for each segment can be programed individually through a corresponding 8-bit register. In normal operation, i.e., non-arbitrary mode, codes are stored in an internal ROM and are used to generate the pulse shape, as shown in Table 12. Typical ROM values are given below in Hex.

TABLE 12: TYPICAL ROM VALUES

LINE DISTANCE	SEGMENT #							
FEET	1	2	3	4	5	6	7	8
0 - 133	22	1F	1E	1D	4F	48	44	41
133 - 266	25	21	20	1E	52	4C	47	43
266 - 399	2C	23	21	20	57	4C	47	43
399 - 525	32	25	23	22	66	52	47	44
525 - 655	3D	27	24	22	70	57	49	44
E1	24	1E	1E	1E	00	00	00	00

NOTE: *The same register bank (eight registers in total) holds the values for any given line length. In other words , the user can not load all the desired values for all the line lengths into the device at one time. If the line length is changed, new codes must be loaded into the register banks.*

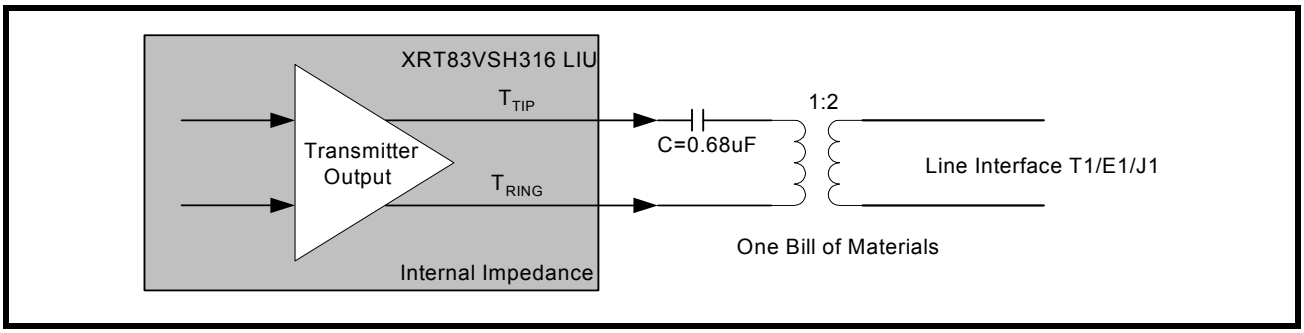
4.7 DMO (Digital Monitor Output, Line Side Only)

The driver monitor circuit is used to detect transmit driver failures by monitoring the activities at TTip/TRing outputs. Driver failure may be caused by a short circuit in the primary transformer or system problems at the transmit inputs. If the transmitter of a channel has no output for more than 128 clock cycles, DMO is set "High" until a valid transmit pulse is detected. If the DMO interrupt is enabled, the change in status of DMO will cause the interrupt pin to go "Low". Once the status register is read, the interrupt pin will return "High" and the status register will be reset (RUR).

4.8 Line Termination (TTip/TRing)

The output stage of the transmit path generates standard return-to-zero (RZ) signals to the line interface for T1/E1/J1 twisted pair or E1 coaxial cable. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for all modes of operation reducing the number of external components necessary in system design. The transmitter outputs only require one DC blocking capacitor of 0.68μF. For redundancy applications (or simply to tri-state the transmitters), set TxTSEL to a "1" in the appropriate channel register. A typical transmit interface is shown in Figure 23.

FIGURE 23. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION



5.0 T1/E1 APPLICATIONS

This application section describes common T1/E1 system considerations along with the various loop back modes available in the LIU.

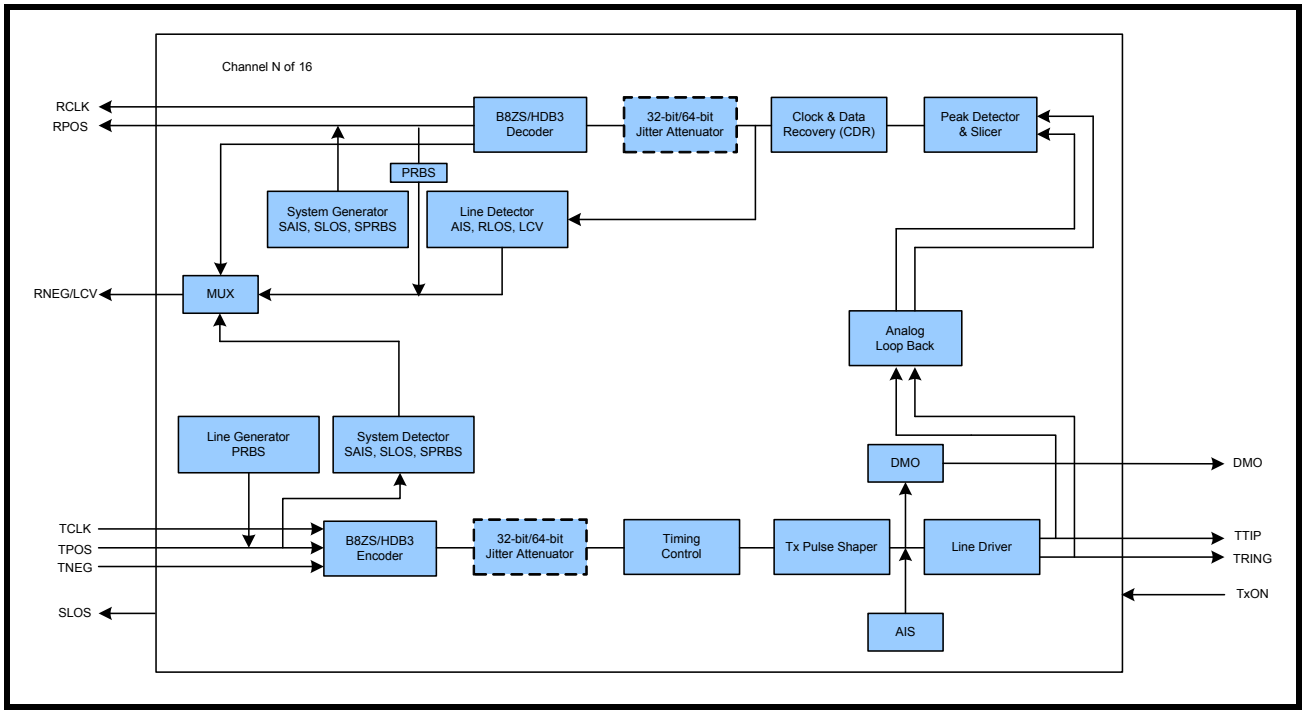
5.1 Loopback Diagnostics

The XRT83VSH316 supports several loopback modes for diagnostic testing. The following section describes the local analog loopback, remote loopback, digital loopback, and dual loopback modes.

5.1.1 Local Analog Loopback

With local analog loopback activated, the transmit output data at TTip/TRing is internally looped back to the analog inputs at RTip/RRing. External inputs at RTip/RRing are ignored while valid transmit output data continues to be sent to the line. A simplified block diagram of local analog loopback is shown in Figure 24.

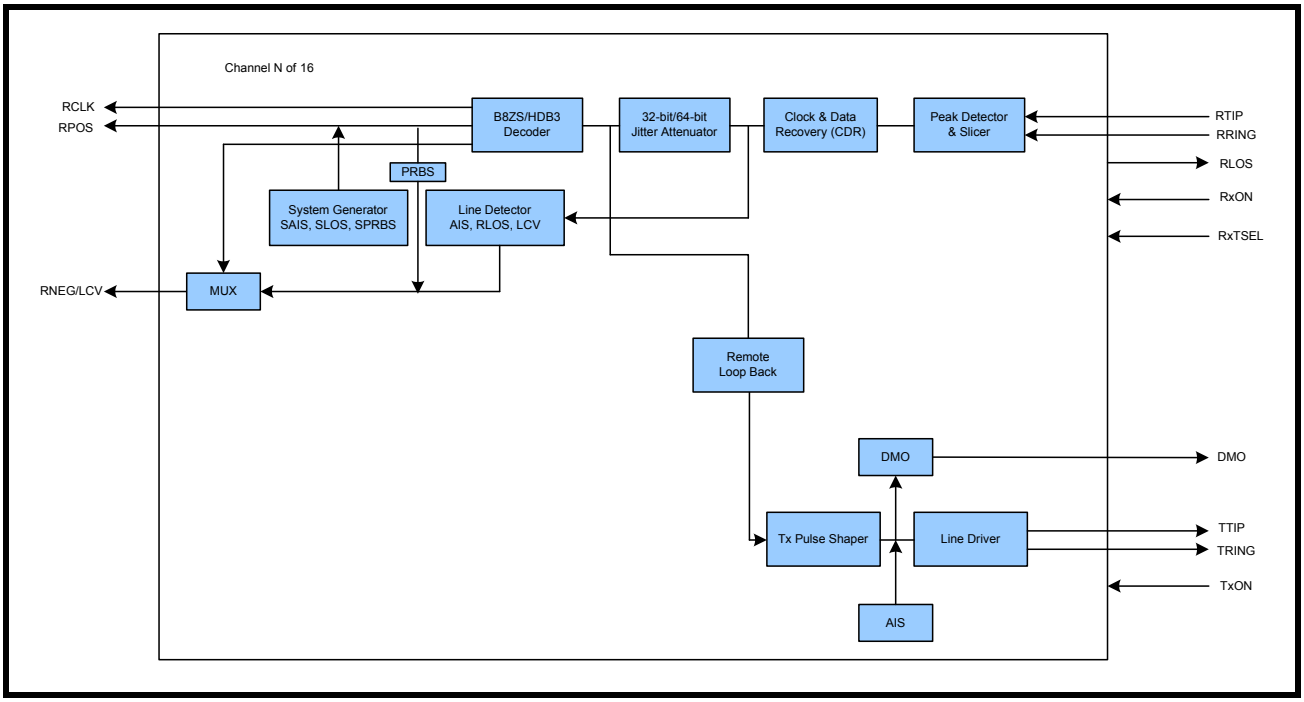
FIGURE 24. SIMPLIFIED BLOCK DIAGRAM OF LOCAL ANALOG LOOPBACK



5.1.2 Remote Loopback

With remote loopback activated, the receive input data at RTip/RRing is internally looped back to the transmit output data at TTip/TRing. The transmit input data at TCLK/TPOS/TNEG are ignored while valid receive output data continues to be sent to the system. A simplified block diagram of remote loopback is shown in Figure 25.

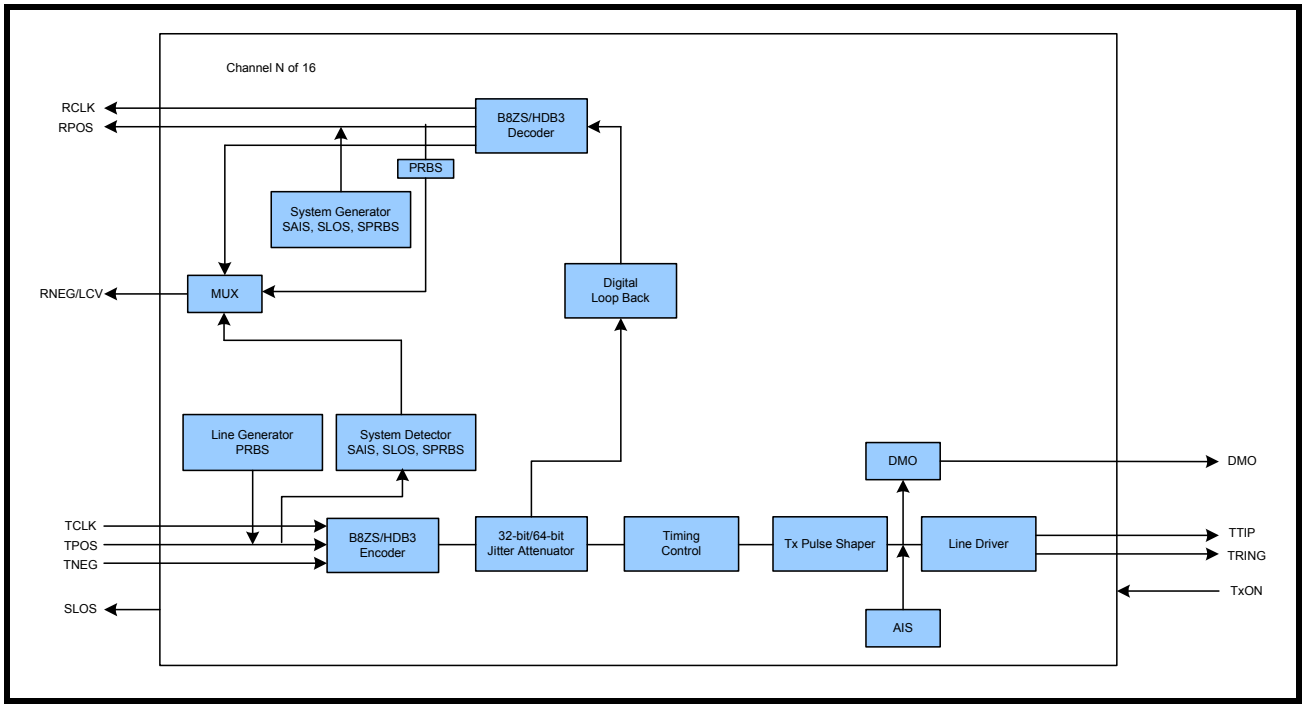
FIGURE 25. SIMPLIFIED BLOCK DIAGRAM OF REMOTE LOOPBACK



5.1.3 Digital Loopback

With digital loopback activated, the transmit input data at TCLK/TPOS/TNEG is looped back to the receive output data at RCLK/RPOS/RNEG after the Transmit Jitter Attenuator (if enabled). The receive input data at RTIP/RRING is ignored while valid transmit output data continues to be sent to the line. A simplified block diagram of digital loopback is shown in Figure 26.

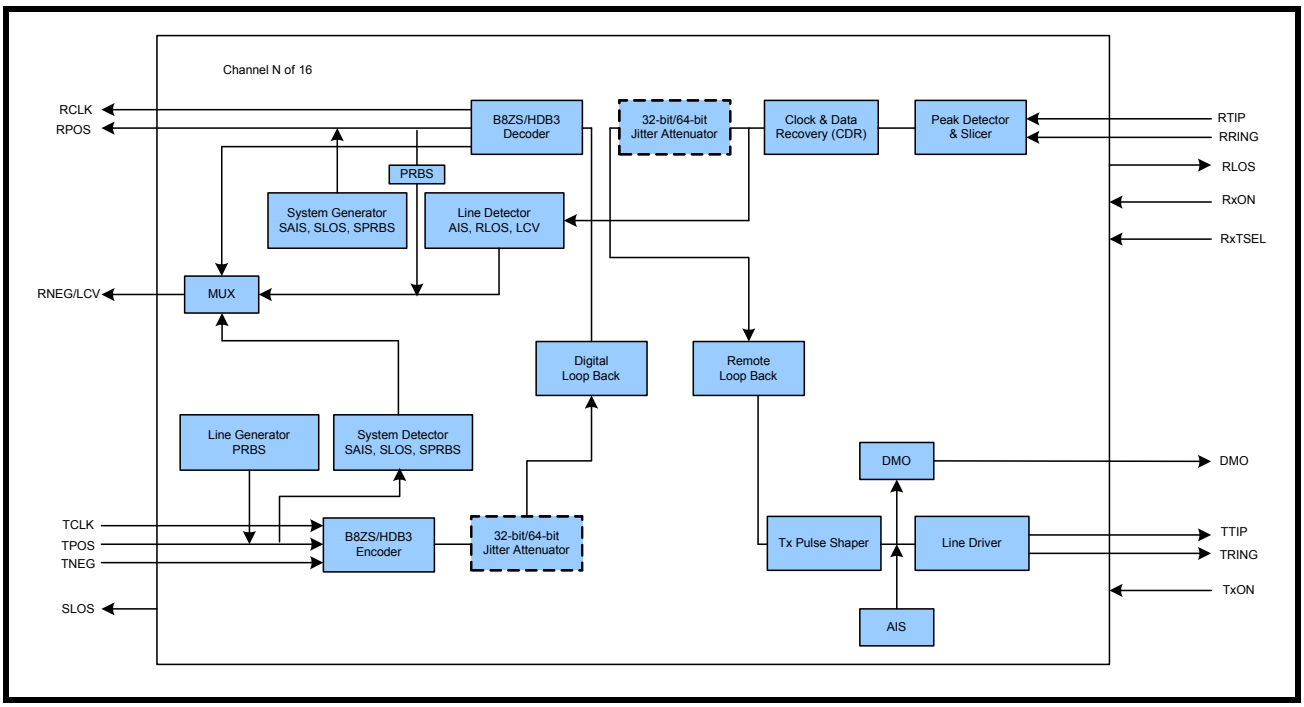
FIGURE 26. SIMPLIFIED BLOCK DIAGRAM OF DIGITAL LOOPBACK



5.1.4 Dual Loopback

With dual loopback activated, the remote loopback is combined with the digital loopback. A simplified block diagram of dual loopback is shown in Figure 27.

FIGURE 27. SIMPLIFIED BLOCK DIAGRAM OF DUAL LOOPBACK



5.2 84-Channel T1/E1 Multiplexer/Mapper Applications

The XRT83VSH316 has the capability of providing the necessary chip selects for multiple 16-channel LIU devices. The LIU is responsible for selecting itself, up to 5 additional LIU devices, or all 6 devices simultaneously for permitting access to internal registers. The state of the chip select output pins is determined by a chip select decoder controlled by the CSdec[2:0]. Figure 28 is a simplified block diagram of connecting six 16-channel LIU devices for 84-channel applications. Selection of the chip select outputs using CSdec[2:0] is shown in Table 13.

FIGURE 28. SIMPLIFIED BLOCK DIAGRAM OF AN 84-CHANNEL APPLICATION

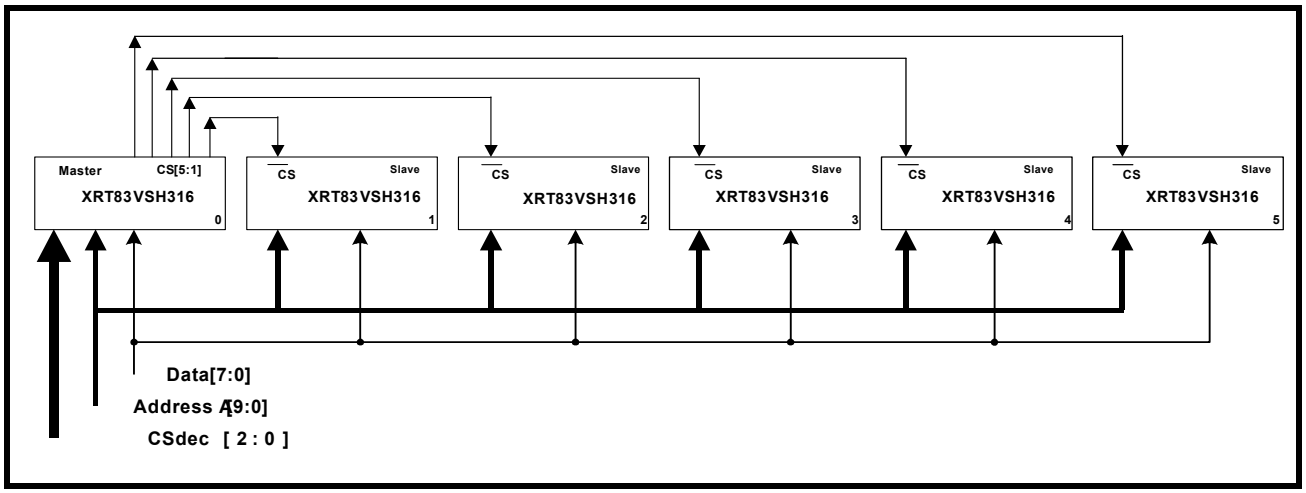


TABLE 13: CHIP SELECT ASSIGNMENTS

CSDEC[2:0]	ACTIVE CHIP SELECT
0h (000)	Current Device (Master)
1h (001)	Chip 1
2h (010)	Chip 2
3h (011)	Chip 3
4h (100)	Chip 4
5h (101)	Chip 5
6h (110)	Reserved
7h (111)	All Devices Active

5.3 Line Card Redundancy

Telecommunication system design requires signal integrity and reliability. When a T1/E1 primary line card has a failure, it must be swapped with a backup line card while maintaining connectivity to a backplane without losing data. System designers can achieve this by implementing common redundancy schemes with the XRT83VSH316 LIU. EXAR offers features that are tailored to redundancy applications while reducing the number of components and providing system designers with solid reference designs.

RLOS/SLOS and DMO

If an RLOS/SLOS or DMO condition occurs, the XRT83VSH316 reports the alarm to the individual status registers on a per channel basis. However, for redundancy applications, an RLOS/SLOS or DMO alarm can be used to initiate an automatic switch to the back up card. For this application, three global pins RLOS, SLOS, and DMO are used to indicate that one of the 16-channels has a LOS or DMO condition.

Typical Redundancy Schemes

- 1:1 One backup card for every primary card (Facility Protection)
- 1+1 One backup card for every primary card (Line Protection)
- ·N+1 One backup card for N primary cards

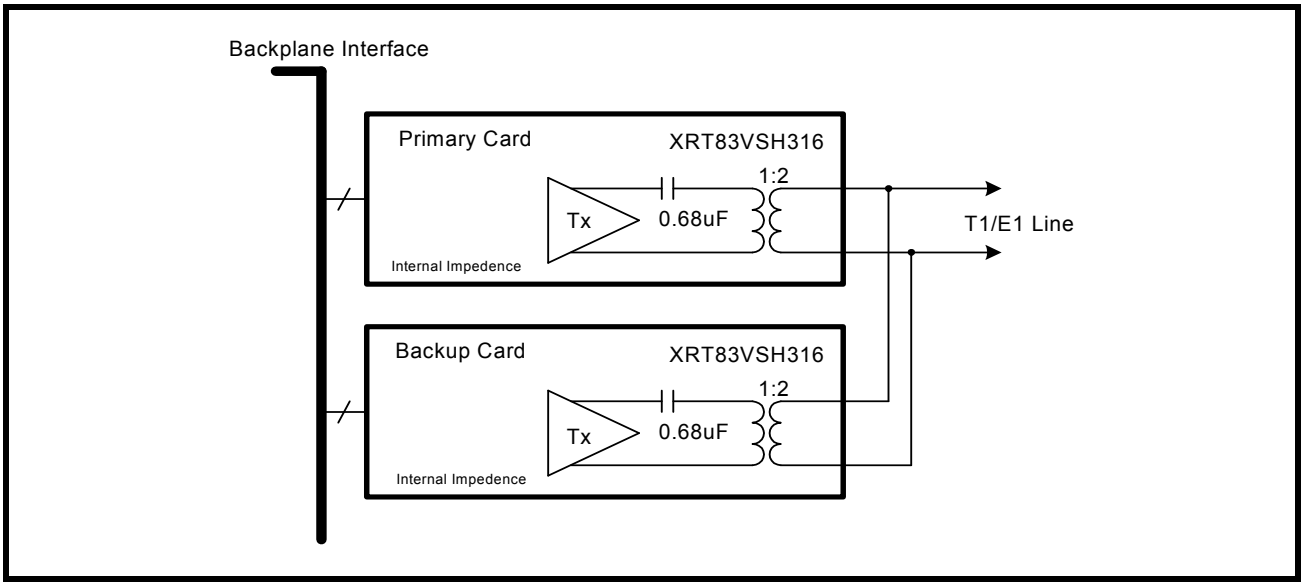
5.3.1 1:1 and 1+1 Redundancy Without Relays

The 1:1 facility protection and 1+1 line protection have one backup card for every primary card. When using 1:1 or 1+1 redundancy, the backup card has its transmitters tri-stated and its receivers in high impedance. This eliminates the need for external relays and provides one bill of materials for all interface modes of operation. For 1+1 line protection, the receiver inputs on the backup card have the ability to monitor the line for bit errors while in high impedance. The transmit and receive sections of the LIU device are described separately.

5.3.2 Transmit Interface with 1:1 and 1+1 Redundancy

The transmitters on the backup card should be tri-stated. Select the appropriate impedance for the desired mode of operation, T1/E1/J1. A 0.68uF capacitor is used in series with TTIP for blocking DC bias. See Figure 29. for a simplified block diagram of the transmit section for a 1:1 and 1+1 redundancy.

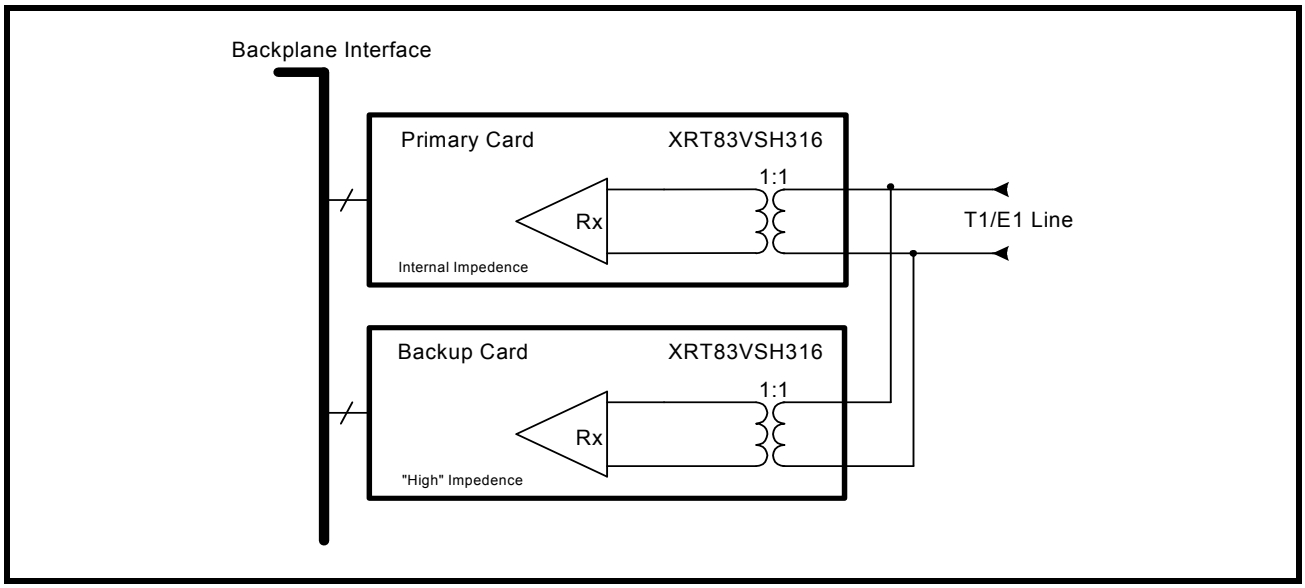
FIGURE 29. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT INTERFACE FOR 1:1 AND 1+1 REDUNDANCY



5.3.3 Receive Interface with 1:1 and 1+1 Redundancy

The receivers on the backup card should be programmed for "High" impedance. Since there is no external resistor in the circuit, the receivers on the backup card will not load down the line interface. This key design feature eliminates the need for relays and provides one bill of materials for all interface modes of operation. Select the impedance for the desired mode of operation, T1/E1/J1. To swap the primary card, set the backup card to internal impedance, then the primary card to "High" impedance. See Figure 30. for a simplified block diagram of the receive section for a 1:1 redundancy scheme.

FIGURE 30. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE INTERFACE FOR 1:1 AND 1+1 REDUNDANCY



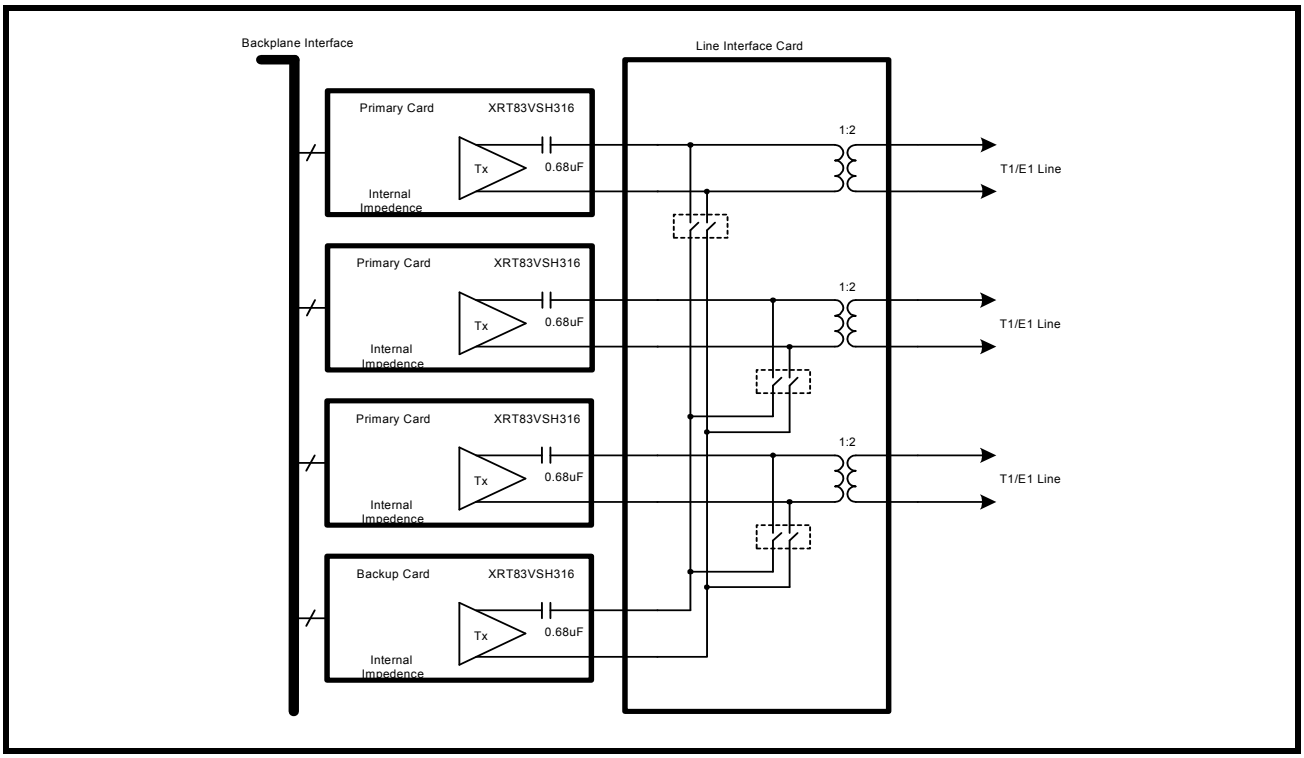
5.3.4 N+1 Redundancy Using External Relays

N+1 redundancy has one backup card for N primary cards. Due to impedance mismatch and signal contention, external relays are necessary when using this redundancy scheme. The relays create complete isolation between the primary cards and the backup card. This allows all transmitters and receivers on the primary cards to be configured in internal impedance, providing one bill of materials for all interface modes of operation. The transmit and receive sections of the LIU device are described separately.

5.3.5 Transmit Interface with N+1 Redundancy

For N+1 redundancy, the transmitters on all cards should be programmed for internal impedance. The transmitters on the backup card do not have to be tri-stated. To swap the primary card, close the desired relays, and tri-state the transmitters on the failed primary card. A 0.68uF capacitor is used in series with TTIP for blocking DC bias. See Figure 31 for a simplified block diagram of the transmit section for an N+1 redundancy scheme.

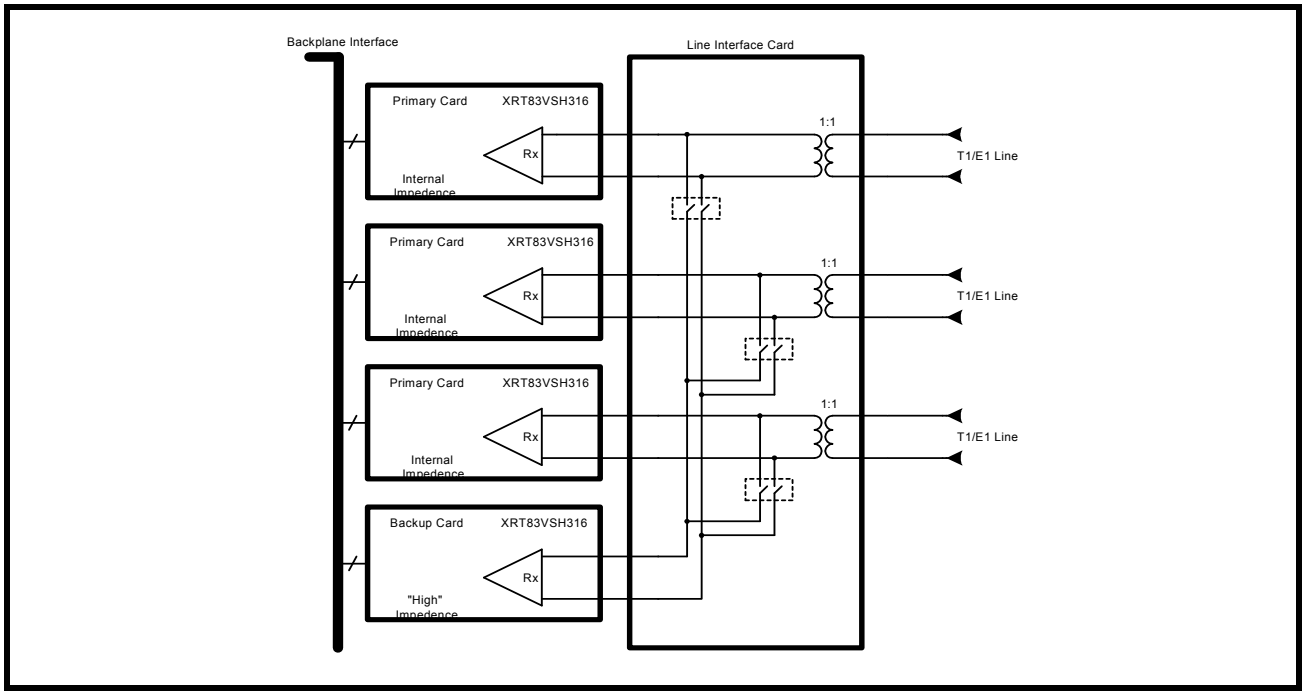
FIGURE 31. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT INTERFACE FOR N+1 REDUNDANCY



5.3.6 Receive Interface with N+1 Redundancy

For N+1 redundancy, the receivers on the primary cards should be programmed for internal impedance. The receivers on the backup card should be programmed for "High" impedance mode. To swap the primary card, set the backup card to internal impedance, then the primary card to "High" impedance. See Figure 32 for a simplified block diagram of the receive section for a N+1 redundancy scheme.

FIGURE 32. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE INTERFACE FOR N+1 REDUNDANCY



5.4 Power Failure Protection

For 1:1 or 1+1 line card redundancy in T1/E1 applications, power failure could cause a line card to change the characteristics of the line impedance, causing a degradation in system performance. The XRT83VSH316 was designed to ensure reliability during power failures. The LIU has patented high impedance circuits that allow the receiver inputs and the transmitter outputs to be in "High" impedance when the LIU experiences a power failure or when the LIU is powered off.

NOTE: *For power failure protection, a transformer must be used to couple to the line interface. See the TAN-56 application note for more details.*

5.5 Overvoltage and Overcurrent Protection

Physical layer devices such as LIUs that interface to telecommunications lines are exposed to overvoltage transients posed by environmental threats. An Overvoltage transient is a pulse of energy concentrated over a small period of time, usually under a few milliseconds. These pulses are random and exceed the operating conditions of CMOS transceiver ICs. Electronic equipment connecting to data lines are susceptible to many forms of overvoltage transients such as lightning, AC power faults and electrostatic discharge (ESD). There are three important standards when designing a telecommunications system to withstand overvoltage transients.

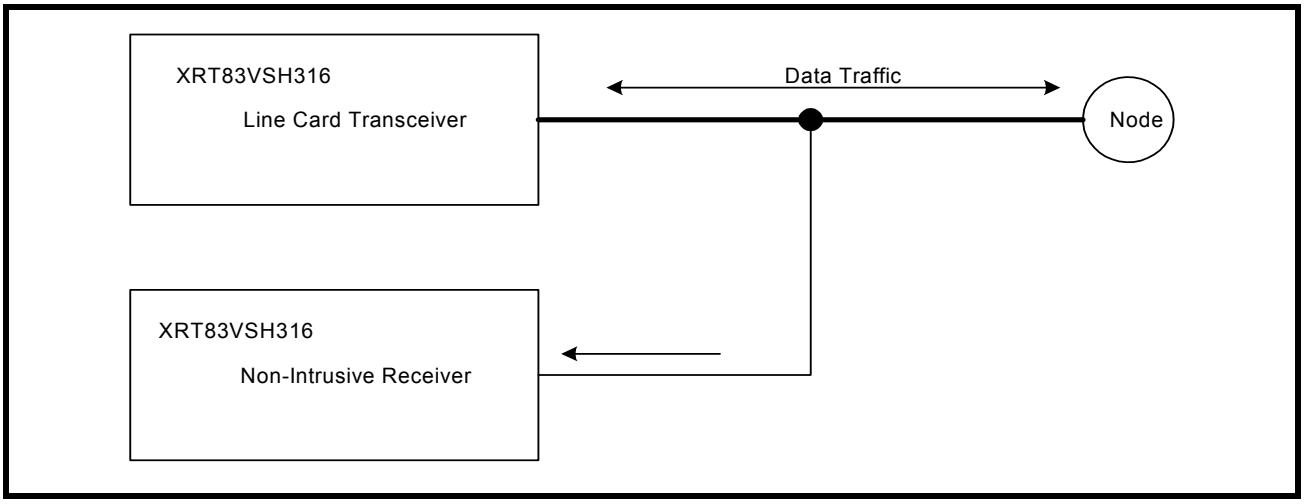
- UL1950 and FCC Part 68
- Telcordia (Bellcore) GR-1089
- ITU-T K.20, K.21 and K.41

NOTE: For a reference design and performance, *see the TAN-58 application note for more details.*

5.6 Non-Intrusive Monitoring

In non-intrusive monitoring applications, the transmitters are shut off by setting TxON "Low". The receivers must be actively receiving data without interfering with the line impedance. The XRT83VSH316's internal termination ensures that the line termination meets T1/E1 specifications for 75Ω, 100Ω or 120Ω while monitoring the data stream. System integrity is maintained by placing the non-intrusive receiver in "High" impedance, equivalent to that of a 1+1 redundancy application. A simplified block diagram of non-intrusive monitoring is shown in Figure 33.

FIGURE 33. SIMPLIFIED BLOCK DIAGRAM OF A NON-INTRUSIVE MONITORING APPLICATION



5.7 Analog Board Continuity Check

This test verifies the per-channel continuity from the Line Side of TIP and RING for both the transmitters and receivers, through the transformers on the assembly and LIU. Inside the LIU, a MUX and Control logic using TMS and TCK as reset and clock, successively connect each TIP and RING on the XRT83VSH316 side to two Analog Test Pins, (ATP_TIP and ATP_RING). Simplified block and timing diagrams are shown in Figure 34 and Figure 35.

FIGURE 34. ATP TESTING BLOCK DIAGRAM

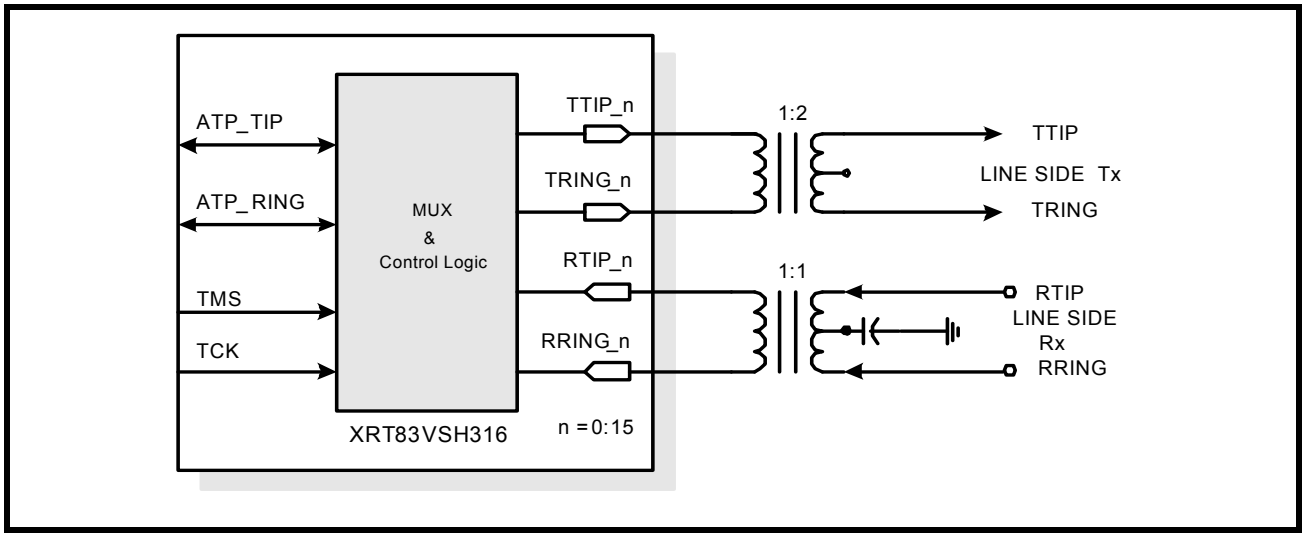
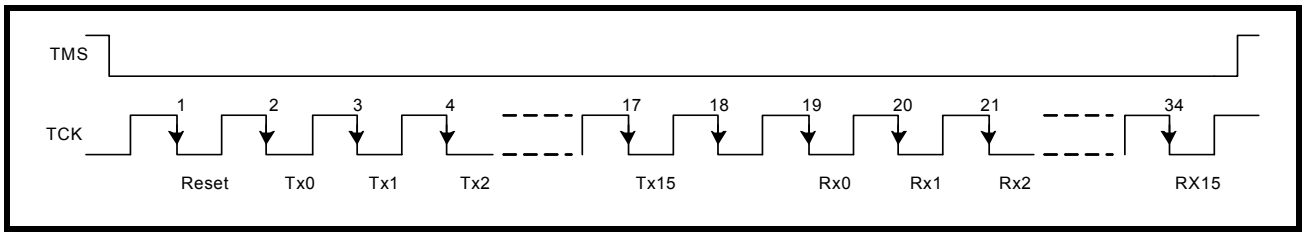


FIGURE 35. TIMING DIAGRAM FOR ATP TESTING



5.7.1 Transmitter TTIP and TRING Testing

Testing of each channel must be done in sequence. With a clock signal applied to TCK, Setting TMS to “0” will begin the test sequence. On the falling edge of the 1st clock pulse after TMS is set to “0”, the sequence will reset as shown in Figure 35 above. On the 2nd falling clock edge the signal on ATP_TIP and ATP_RING will be TTIP_0 and TRING_0, respectively. On the falling edge of the 19th clock pulse the signal on ATP_TIP and ATP_RING will be connected to RTIP_0 and RRING_0, respectively. After the 34th clock pulse TMS can be returned to a “1” and all channels will return to their normal state.

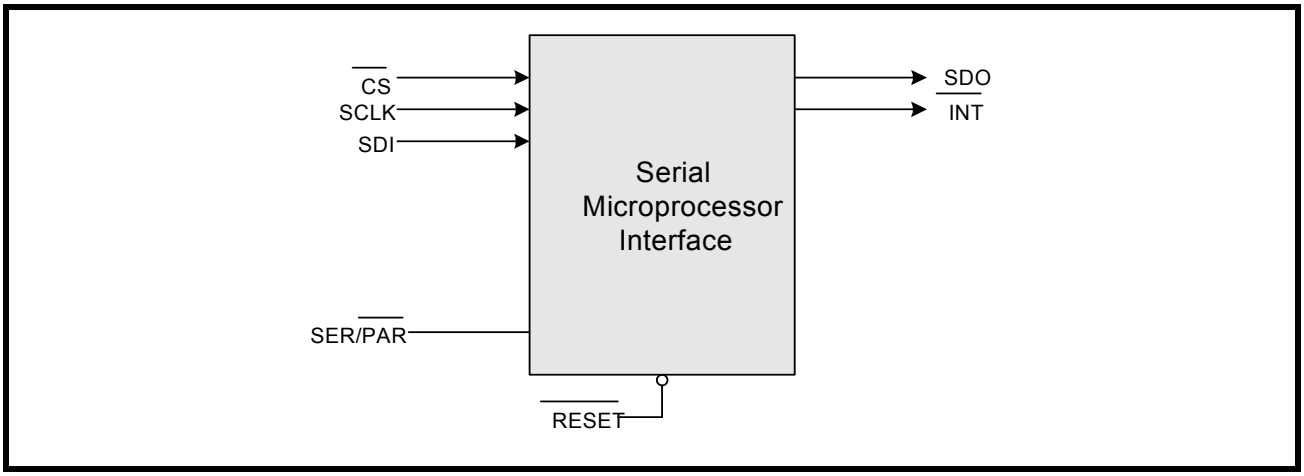
6.0 MICROPROCESSOR INTERFACE

The microprocessor interface can be accessed through a Standard Peripheral Interface (Serial SPI) or Standard Parallel Microprocessor Interface. By default, the parallel interface is selected. To use the SPI interface, the SER/$\overline{PAR}$ pin must be pulled "High".

6.1 *SPI Serial Peripheral Interface Block*

The serial microprocessor uses a standard 3-pin serial port with $\overline{CS}$, SCLK, and SDI for programming the LIU. Optional pins such as SDO, $\overline{INT}$, and $\overline{RESET}$ allow the ability to read back contents of the registers, monitor the LIU via an interrupt pin, and reset the LIU to its default configuration by pulling reset "Low" for more than 10μS. A simplified block diagram of the Serial Microprocessor is shown in Figure 36.

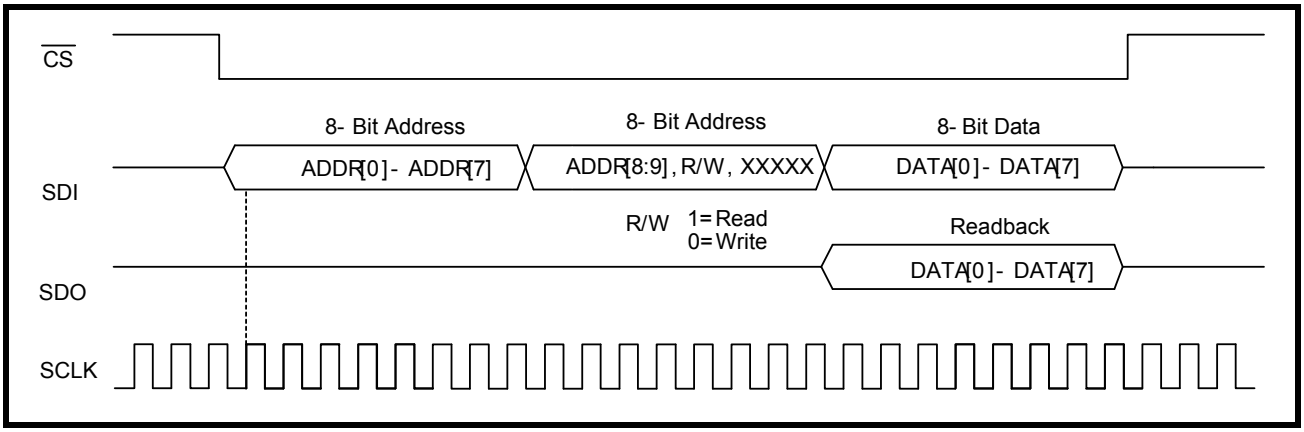
FIGURE 36. SIMPLIFIED BLOCK DIAGRAM OF THE SERIAL MICROPROCESSOR INTERFACE



6.1.1 Serial Timing Information

The serial port requires 24 bits of data applied to the SDI (Serial Data Input) pin. The Serial Microprocessor samples SDI on the rising edge of SCLK (Serial Clock Input). The data is not latched into the device until all 24 bits of serial data have been sampled. A timing diagram of the Serial Microprocessor is shown in Figure 37.

FIGURE 37. TIMING DIAGRAM FOR THE SERIAL MICROPROCESSOR INTERFACE



NOTE: *For applications without a free running SCLK, a minimum of 1 SCLK pulse must be applied when $\overline{CS}$ is "High", befrore pulling $\overline{CS}$ "Low".*

6.1.2 24-Bit Serial Data Input Descritption

The serial data input is sampled on the rising edge of SCLK. In readback mode, the serial data output is updated on the falling edge of SCLK. The serial data must be applied to the LIU LSB first. The 24 bits of serial data are described below.

6.1.3 ADDR[9:0] (SCLK1 - SCLK10)

The first 10 SCLK cycles are used to provide the address to which a Read or Write operation will occur. ADDR[0] (LSB) must be sent to the LIU first followed by ADDR[1] and so forth until all 10 address bits have been sampled by SCLK.

6.1.4 R/W (SCLK11)

The next serial bit applied to the LIU informs the microprocessor that a Read or Write operation is desired. If the R/W bit is set to “0”, the microprocessor is configured for a Write operation. If the R/W bit is set to “1”, the microprocessor is configured for a Read operation.

6.1.5 Dummy Bits (SCLK12 - SCLK16)

The next 5 SCLK cycles are used as dummy bits. Five bits were chosen so that the serial interface can easily be divided into three 8-bit words to be compliant with standard serial interface devices. The state of these bits are ignored and can hold either “0” or “1” during both Read and Write operations.

6.1.6 DATA[7:0] (SCLK17 - SCLK24)

The next 8 SCLK cycles are used to provide the data to be written into the internal register chosen by the address bits. DATA[0] (LSB) must be sent to the LIU first followed by DATA[1] and so forth until all 8 data bits have been sampled by SCLK. Once 24 SCLK cycles have been completed, the LIU holds the data until $\overline{CS}$ is pulled “High” whereby, the serial microprocessor latches the data into the selected internal register.

6.1.7 8-Bit Serial Data Output Description

The serial data output is updated on the falling edge of SCLK17 - SCLK24 if R/W is set to “1”. DATA[0] (LSB) is provided on SCLK17 to the SDO pin first followed by DATA[1] and so forth until all 8 data bits have been updated. The SDO pin allows the user to read the contents stored in individual registers by providing the desired address on the SDI pin during the Read cycle.

FIGURE 38. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE

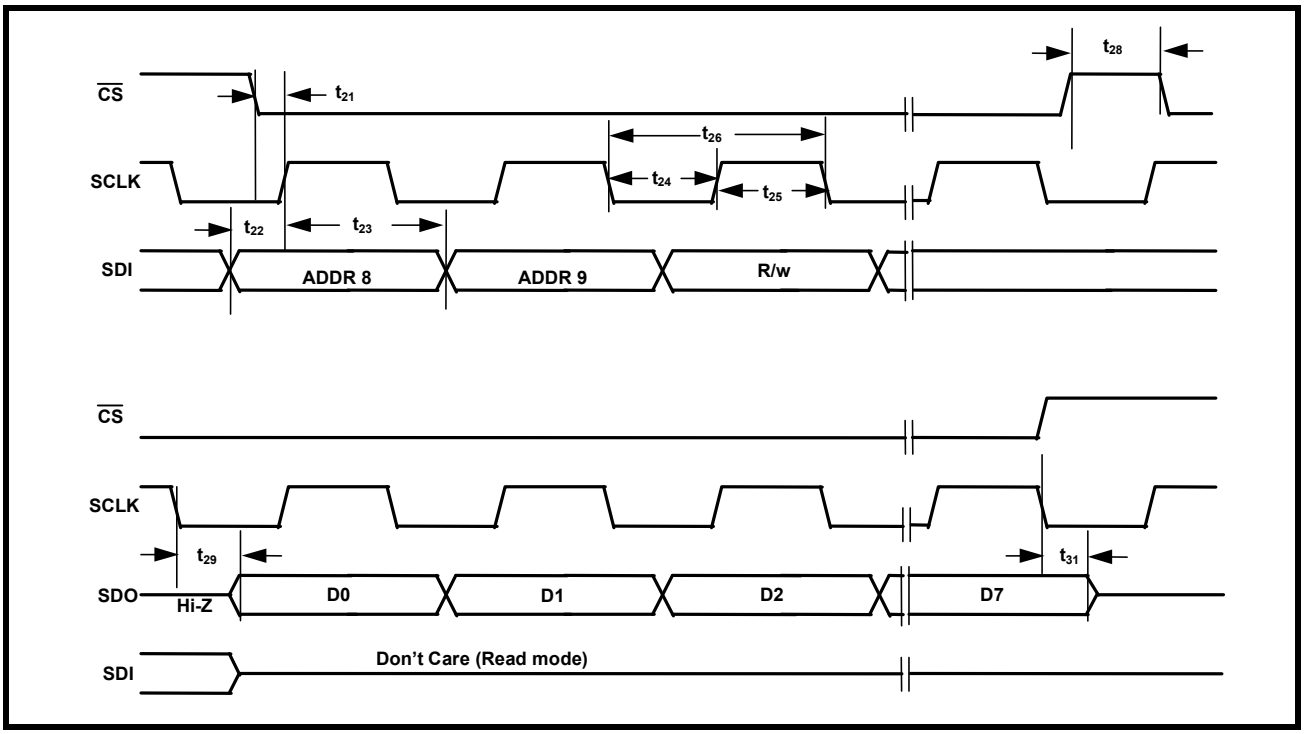


TABLE 14: MICROPROCESSOR SERIAL INTERFACE TIMINGS (T_A = 25^{0}C, V_{DD}=3.3V± 5% AND LOAD = 10PF)

SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNITS
t_{21}	$\overline{CS}$ Low to Rising Edge of SClk	5			ns
t_{22}	SDI to Rising Edge of SClk	5			ns
t_{23}	SDI to Rising Edge of SClk Hold Time	5			ns
t_{24}	SClk "Low" Time	20			ns
t_{25}	SClk "High" Time	20			ns
t_{26}	SClk Period	40			ns
t_{28}	$\overline{CS}$ Inactive Time	40			ns
t_{29}	Falling Edge of SClk to SDO Valid Time			5	ns
t_{31}	Rising edge of $\overline{CS}$ to High Z			5	ns

6.2 Parallel Microprocessor Interface Block

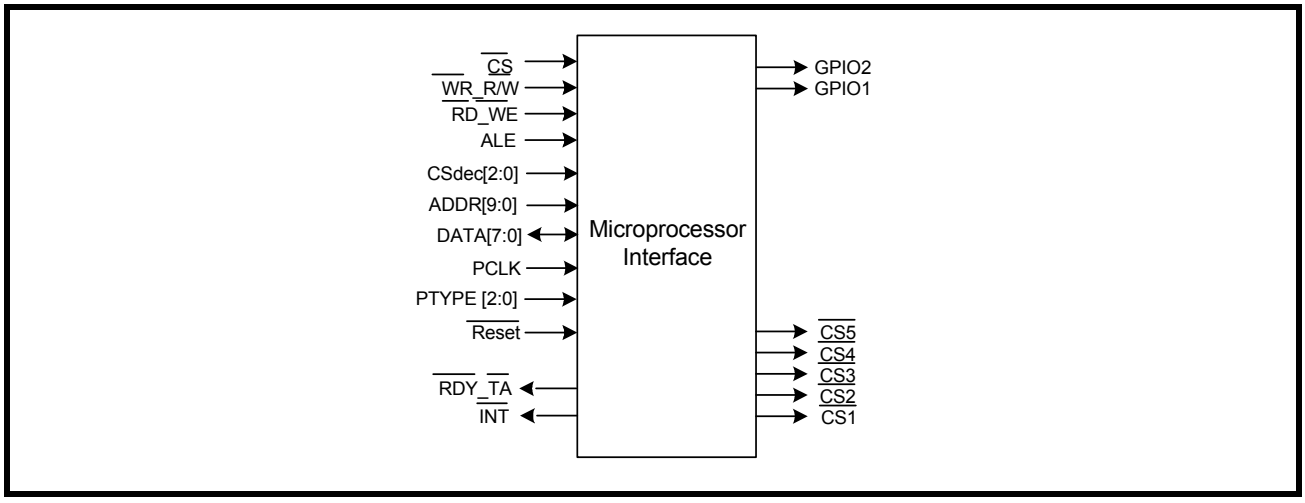
The Parallel Microprocessor Interface section supports communication between the local microprocessor (µP) and the LIU. The XRT83VSH316 supports an Intel asynchronous interface, Motorola 68K asynchronous, Power PC, and Motorola MPC8xx interface. The microprocessor interface is selected by the state of the PTYPE[2:0] input pins. Selecting the microprocessor interface is shown in Table 15.

TABLE 15: SELECTING THE MICROPROCESSOR INTERFACE MODE

PTYPE[2:0]	MICROPROCESSOR MODE
0h (000)	Intel 68HC11, 8051, 80C188 (Asynchronous)
1h (001)	Motorola 68K (Asynchronous)
5h (101)	Power PC (Synchronous)
7h (111)	Motorola MPC8260, MPC860 (Synchronous)

The XRT83VSH316 uses multipurpose pins to configure the device appropriately. The local µP configures the LIU by writing data into specific addressable, on-chip Read/Write registers. The microprocessor interface provides the signals which are required for a general purpose microprocessor to read or write data into these registers including two general purpose inputs/outputs (GPIO). The microprocessor interface also supports polled and interrupt driven environments. A simplified block diagram of the microprocessor is shown in Figure 39.

FIGURE 39. SIMPLIFIED BLOCK DIAGRAM OF THE MICROPROCESSOR INTERFACE BLOCK



6.3 The Microprocessor Interface Block Signals

The LIU may be configured into different operating modes and have its performance monitored by software through a standard microprocessor using data, address and control signals. These interface signals are described below in Table 16, Table 17, and Table 18. The microprocessor interface can be configured to operate in Intel mode or Motorola mode. When the microprocessor interface is operating in Intel mode, some of the control signals function in a manner required by the Intel 80xx family of microprocessors. Likewise, when the microprocessor interface is operating in Motorola mode, then these control signals function in a manner as required by the Motorola Power PC family of microprocessors. (For using a Motorola 68K asynchronous processor, see Figure 43 and Table 22) Table 16 lists and describes those microprocessor interface signals whose role is constant across the two modes. Table 17 describes the role of some of these signals when the microprocessor interface is operating in the Intel mode. Likewise, Table 18 describes the role of these signals when the microprocessor interface is operating in the Motorola Power PC mode.

TABLE 16: XRT83VSH316 MICROPROCESSOR INTERFACE SIGNALS COMMON TO BOTH INTEL AND MOTOROLA MODES

PIN NAME	TYPE	DESCRIPTION
PTYPE[2:0]	I	**Microprocessor Interface Mode Select Input pins** These three pins are used to specify the microprocessor interface mode. The relationship between the state of these three input pins, and the corresponding microprocessor mode is presented in Table 15.
DATA[7:0]	I/O	**Bi-Directional Data Bus for register "Read" or "Write" Operations.**
CSdec[2:0]	I	**Chip Select Decoder Inputs** The state of these 3 pins enable the Chip Selects for additional LIU devices. ***NOTE:*** *See the 84-Channel Application Section of this datasheet.*
ADDR[9:0]	I	**Nine-Bit Address Bus Inputs** The XRT83VSH316 LIU microprocessor interface uses a direct address bus. This address bus is provided to permit the user to select an on-chip register for Read/Write access.
$\overline{CS}$	I	**Chip Select Input** This active low signal selects the microprocessor interface of the XRT83VSH316 LIU and enables Read/Write operations with the on-chip register locations.

TABLE 17: INTEL MODE: MICROPROCESSOR INTERFACE SIGNALS

XRT83VSH316 PIN NAME	INTEL EQUIVALENT PIN	TYPE	DESCRIPTION
ALE_TS	ALE	I	**Address-Latch Enable:** This active high signal is used to latch the contents on the address bus ADDR[8:0]. The contents of the address bus are latched into the ADDR[8:0] inputs on the falling edge of ALE.
$\overline{RD}$_$\overline{WE}$	$\overline{RD}$	I	**Read Signal:** This active low input functions as the read signal from the local µP. When this pin is pulled “Low” (if $\overline{CS}$ is “Low”) the LIU is informed that a read operation has been requested and begins the process of the read cycle.
$\overline{WR}$_R/$\overline{W}$	$\overline{WR}$	I	**Write Signal:** This active low input functions as the write signal from the local µP. When this pin is pulled “Low” (if $\overline{CS}$ is “Low”) the LIU is informed that a write operation has been requested and begins the process of the write cycle.
$\overline{RDY}$_$\overline{TA}$	$\overline{RDY}$	O	**Ready Output:** This active low signal is provided by the LIU device. It indicates that the current read or write cycle is complete, and the LIU is waiting for the next command.

TABLE 18: MOTOROLA MODE: MICROPROCESSOR INTERFACE SIGNALS

XRT83VSH316 PIN NAME	MOTOROLA EQUIVALENT PIN	TYPE	DESCRIPTION
ALE_TS	TS	I	**Transfer Start:** This active high signal is used to latch the contents on the address bus ADDR[8:0]. The contents of the address bus are latched into the ADDR[8:0] inputs on the falling edge of TS.
$\overline{WR}$_R/$\overline{W}$	R/$\overline{W}$	I	**Read/Write:** This input pin from the local µP is used to inform the LIU whether a Read or Write operation has been requested. When this pin is pulled "High", $\overline{WE}$ will initiate a read operation. When this pin is pulled "Low", $\overline{WE}$ will initiate a write operation.
$\overline{RD}$_$\overline{WE}$	$\overline{WE}$	I	**Write Enable:** This active low input functions as the read or write signal from the local µP dependent on the state of R/$\overline{W}$. When $\overline{WE}$ is pulled "Low" (If $\overline{CS}$ is "Low") the LIU begins the read or write operation.
No Pin	$\overline{OE}$	I	**Output Enable:** This signal is not necessary for the XRT83VSH316 to interface to the MPC8260 or MPC860 Power PCs.
µPCLK	CLKOUT	I	**Synchronous Processor Clock:** This signal is used as the timing reference for the Power PC synchronous mode.
$\overline{RDY}$_$\overline{TA}$	$\overline{TA}$	O	**Transfer Acknowledge:** This active low signal is provided by the LIU device. It indicates that the current read or write cycle is complete, and the LIU is waiting for the next command.

6.4 Intel Mode Programmed I/O Access (Asynchronous)

If the LIU is interfaced to an Intel type µP, then it should be configured to operate in the Intel mode. Intel type Read and Write operations are described below.

Intel Mode Read Cycle

Whenever an Intel-type µP wishes to read the contents of a register, it should do the following.

1. Place the address of the target register on the address bus input pins ADDR[9:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the LIU, by toggling it "Low". This action enables further communication between the µP and the LIU microprocessor interface block.
3. Toggle the ALE input pin "High". This step enables the address bus input drivers, within the microprocessor interface block of the LIU.
4. The µP should then toggle the ALE pin "Low". This step causes the LIU to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.
5. Next, the µP should indicate that this current bus cycle is a Read operation by toggling the $\overline{RD}$ input pin "Low". This action also enables the bi-directional data bus output drivers of the LIU.
6. After the µP toggles the Read signal "Low", the LIU will toggle the $\overline{RDY}$ output pin "Low". The LIU does this in order to inform the µP that the data is available to be read by the µP, and that it is ready for the next command.
7. After the µP detects the $\overline{RDY}$ signal and has read the data, it can terminate the Read Cycle by toggling the $\overline{RD}$ input pin "High".

NOTE: *$\overline{ALE}$ can be tied "High" if this signal is not available.*

The Intel Mode Write Cycle

Whenever an Intel type µP wishes to write a byte or word of data into a register within the LIU, it should do the following.

1. Place the address of the target register on the address bus input pins ADDR[9:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the LIU, by toggling it "Low". This action enables further communication between the µP and the LIU microprocessor interface block.
3. Toggle the ALE input pin "High". This step enables the address bus input drivers, within the microprocessor interface block of the LIU.
4. The µP should then toggle the ALE pin "Low". This step causes the LIU to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.
5. The µP should then place the byte or word that it intends to write into the target register, on the bi-directional data bus DATA[7:0].
6. Next, the µP should indicate that this current bus cycle is a Write operation by toggling the $\overline{WR}$ input pin "Low". This action also enables the bi-directional data bus input drivers of the LIU.
7. After the µP toggles the Write signal "Low", the LIU will toggle the $\overline{RDY}$ output pin "Low". The LIU does this in order to inform the µP that the data has been written into the internal register location, and that it is ready for the next command.

NOTE: *$\overline{ALE}$ can be tied "High" if this signal is not available.*

The Intel Read and Write timing diagram is shown in Figure 41. The timing specifications are shown in Table 20.

FIGURE 40. INTEL MP INTERFACE TIMING DURING PROGRAMMED I/O READ AND WRITE OPERATIONS WHEN ALE IS NOT TIED 'HIGH'

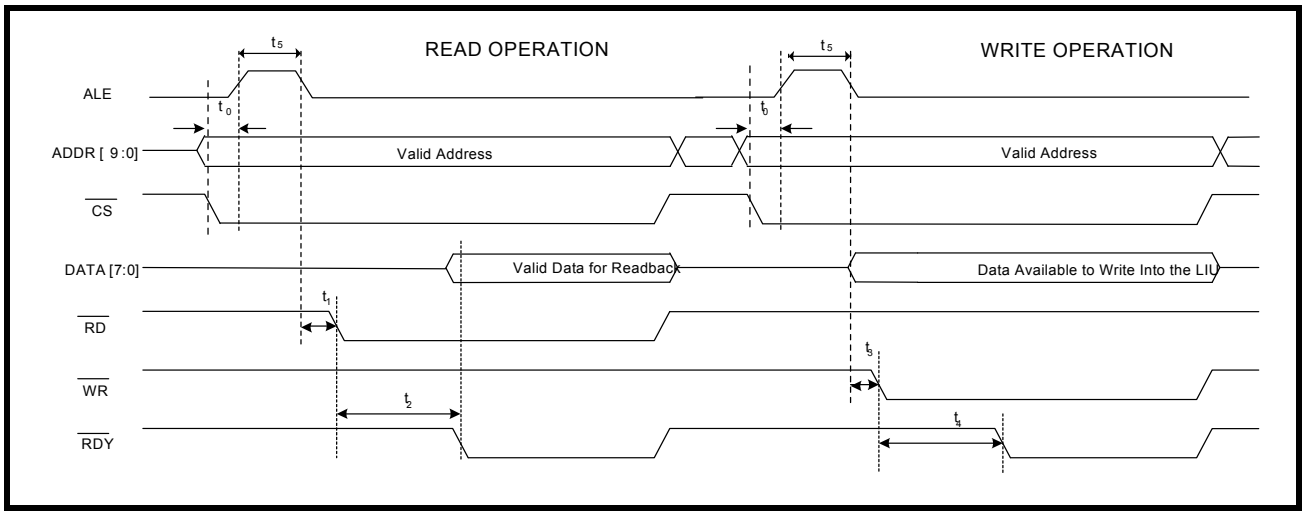


TABLE 19: INTEL MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge and ALE Rising Edge	0	-	ns
t_1	ALE Falling Edge to $\overline{RD}$ Assert	5	-	ns
t_2	$\overline{RD}$ Assert to $\overline{RDY}$ Assert	-	90	ns
NA	$\overline{RD}$ Pulse Width (t_2)	90	-	ns
t_3	ALE Falling Edge to $\overline{WR}$ Assert	5	-	ns
t_4	$\overline{WR}$ Assert to $\overline{RDY}$ Assert	-	90	ns
NA	$\overline{WR}$ Pulse Width (t_4)	90	-	ns
t_5	ALE Pulse Width(t_5)	10		ns

FIGURE 41. INTEL MP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS WITH ALE=HIGH

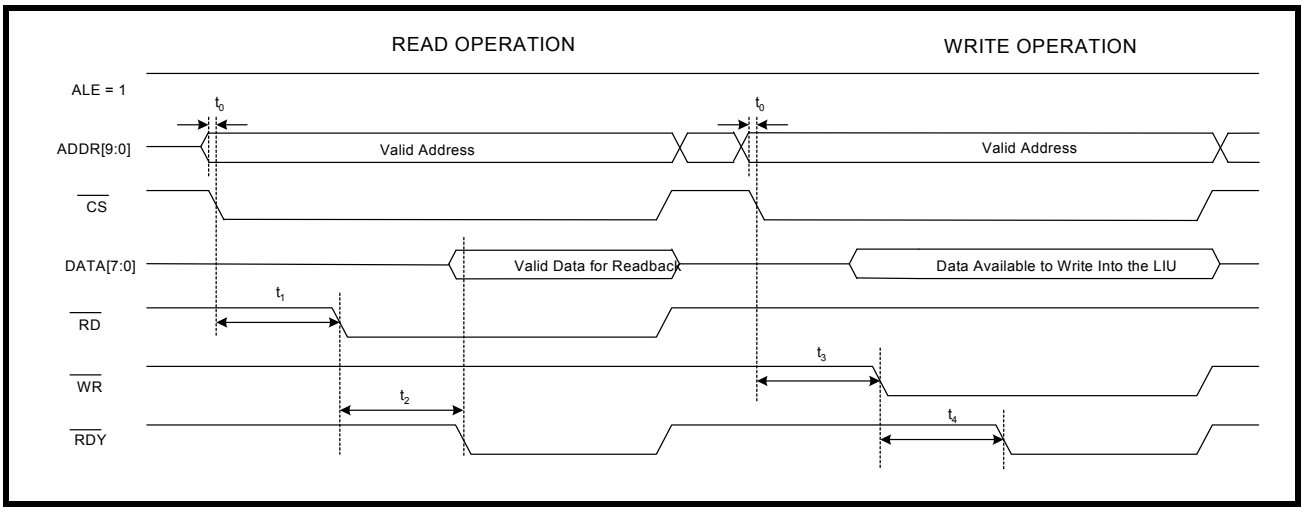


TABLE 20: INTEL MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{RD}$ Assert	65	-	ns
t_2	$\overline{RD}$ Assert to $\overline{RDY}$ Assert	-	90	ns
NA	$\overline{RD}$ Pulse Width (t_2)	90	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{WR}$ Assert	65	-	ns
t_4	$\overline{WR}$ Assert to $\overline{RDY}$ Assert	-	90	ns
NA	$\overline{WR}$ Pulse Width (t_4)	90	-	ns

6.5 MPC86X Mode Programmed I/O Access (Synchronous)

If the LIU is interfaced to a MPC86X type µP, it should be configured to operate in the MPC86X mode. MPC86X Read and Write operations are described below.

MPC86X Mode Read Cycle

1. Place the address of the target register on the address bus input pins ADDR[9:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the LIU, by toggling it "Low". This action enables further communication between the µP and the LIU microprocessor interface block.
3. Next, the µP should indicate that this current bus cycle is a Read operation by pulling the R/$\overline{W}$ input pin "High".
4. The LIU will toggle the $\overline{TA}$ output pin "Low". The LIU does this in order to inform the µP that the data is available to be read by the µP.
5. After the µP detects the $\overline{TA}$ signal and has read the data, it can terminate the Read Cycle by toggling the $\overline{CS}$ input pin "High".

MPC86X Mode Write Cycle

1. Place the address of the target register on the address bus input pins ADDR[9:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the LIU, by toggling it "Low". This action enables further communication between the µP and the LIU microprocessor interface block.
3. Next, the µP should indicate that this current bus cycle is a Write operation by pulling the R/$\overline{W}$ input pin "Low".
4. Toggle the $\overline{WE}$ input pin "Low".
5. After the µP toggles the $\overline{WE}$ signal "Low", the LIU will toggle the $\overline{TA}$ output pin "Low". The LIU does this in order to inform the µP that the data has been written into the internal register location.
6. After the µP detects the $\overline{TA}$ signal, the Write operation is completed by toggling both $\overline{WE}$ and $\overline{CS}$ pins “High”.

The Motorola Read and Write timing diagram is shown in Figure 42. The timing specifications are shown in Table 21.

FIGURE 42. MOTOROLA MPC86X MP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

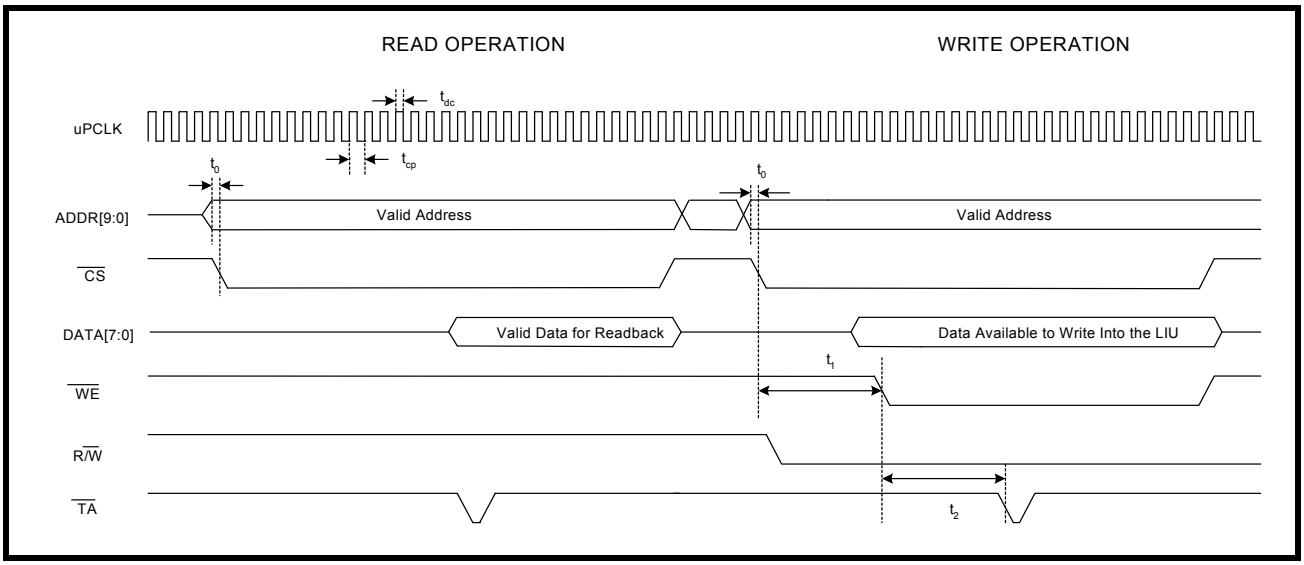


TABLE 21: MOTOROLA MPC86X MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{WE}$ Assert	0	-	ns
t_2	$\overline{WE}$ Assert to $\overline{TA}$ Assert	-	90	ns
t_{dc}	µPCLK Duty Cycle	40	60	%
t_{cp}	µPCLK Clock Period	20		ns

FIGURE 43. MOTOROLA 68K MP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

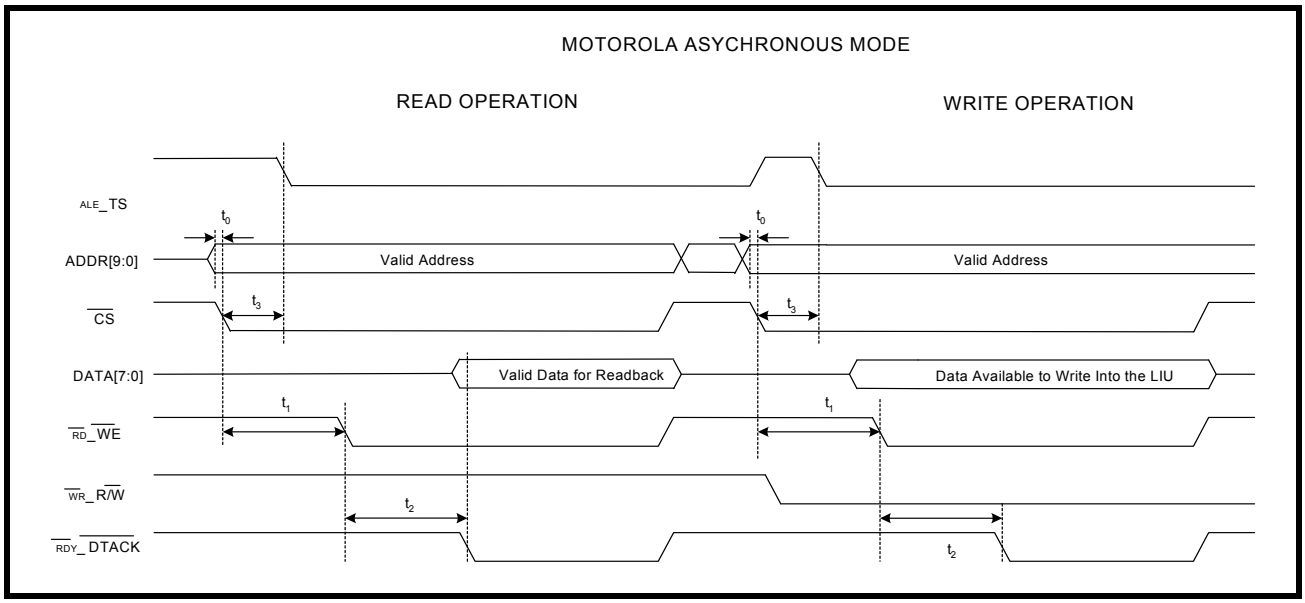


TABLE 22: MOTOROLA 68K MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{DS}$ (Pin $\overline{RD}_\overline{WE}$) Assert	65	-	ns
t_2	$\overline{DS}$ Assert to $\overline{DTACK}$ Assert	-	90	ns
NA	$\overline{DS}$ Pulse Width (t_2)	90	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{AS}$ (Pin ALE_TS) Falling Edge	0	-	ns

7.0 REGISTER DESCRIPTIONS

To use any of the diagnostic features for the Line or System interface, the LIU must be placed in Single Rail mode. The following table is intended to be used as a simplified register map which summarizes the address locations of the LIU features.

TABLE 23: MICROPROCESSOR REGISTER ADDRESS (ADDR[8:0])

REGISTER NUMBER	ADDRESS (HEX)	FUNCTION
1 - 16	0x000 - 0x00F	Global Configuration Registers
17 - 36	0x020 - 0x033	Channel 0 Registers
37 - 56	0x040 - 0x053	Channel 1 Registers
57 - 76	0x060 - 0x073	Channel 2 Registers
77 - 96	0x080 - 0x093	Channel 3 Registers
97 - 116	0x0A0 - 0x0B3	Channel 4 Registers
117 - 136	0x0C0 - 0x0D3	Channel 5 Registers
137 - 156	0x0E0 - 0x0F3	Channel 6 Registers
157 - 176	0x100 - 0x113	Channel 7 Registers
177 - 196	0x120 - 0x133	Channel 8 Registers
197 - 216	0x140 - 0x153	Channel 9 Registers
217 - 236	0x160 - 0x173	Channel 10 Registers
237 - 256	0x180 - 0x193	Channel 11 Registers
257 - 276	0x1A0 - 0x1B3	Channel 12 Registers
277 - 296	0x1C0 - 0x1D3	Channel 13 Registers
297 - 316	0x1E0 - 0x1F3	Channel 14 Registers
317 - 336	0x200 - 0x213	Channel 15 Registers
337	0x3FE	Device ID
338	0x3FF	Revision ID

NOTE: *All register addresses NOT listed above are reserved and are NOT intended to be used as a scratch pad. Values may be written into reserved registers, but they may not be retrievable.*

7.1 Global Configuration Registers (0x000 - 0x00F)

TABLE 24: MICROPROCESSOR REGISTER GLOBAL DESCRIPTION

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
Global Control Registers for All 16 Channels										
1	0x000	R/W	SR/DR	ATAOS	RCLKE	TCLKE	DATAP	Reserved	GIE	SRESET
2	0x001	R/W	Reserved					RxMUTE	EXLOS	ICT
3	0x002	R/W	Reserved	RxTCNTL	Reserved		SYS_EXLOS	Reserved		
4	0x003	R/W	Reserved				SL<1>	SL<0>	Reserved	Reserved
5	0x004	R/W	MCLKT1out[1:0]		MCLKE1out[1:0]		Reserved			
6	0x005	R/W	LCV_OFLW	Reserved		LCVen	LCVCH[3:0]			
7	0x006	R/W	Reserved			allRST	allUPDATE	Reserved	chUPDATE	chRST
8	0x007	RO	LCVCNT[7:0]							
9	0x008	RO	LCVCNT[15:8]							
10	0x009	R/W	Reserved			TCLKCNL	CLKSEL[3:0]			
11	0x00A	RUR	GCHIS[7:0]							
12	0x00B	RUR	GCHIS[15:8]							
13	0x00C	R/W	Reserved			Recovered Clock Selects [4:0]				
14	0x00D	R/W	GPIODIR[1:0]		GPIO[1:0]		Reserved			
15	0x00E	R/W	Reserved							
16	0x00F	R/W	Reserved							

7.2 Channel Control Registers (Line and System Side)

TABLE 25: MICROPROCESSOR REGISTER CHANNEL DESCRIPTION

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
Control and Line Side Diagnostics										
17	0xN00	R/W	QRSS/ PRBS	Reserved	RxON	EQC[4:0]				
18	0xN01	R/W	RxTSEL	TxTSEL	TERSEL[1:0]		JASEL[1:0]		JABW	FIFOS
19	0xN02	R/W	INVQRSS	TxTEST[2:0]			TxON	LOOP[2:0]		
20	0xN03	R/W	RxRES[1:0]		CODES	Reserved	E1Arben	INSBPV	INSBER	Reserved
21	0xN04	R/W	Reserved	DMOIE	FLSIE	LCV_OFIE	Reserved	AISDIE	RLOSIE	QRPDIE
22	0xN05	RO	Reserved	DMO	FLS	LCV_OF	Reserved	AISD	RLOS	QRPD
23	0xN06	RUR	Reserved	DMOIS	FLSIS	LCV_OFIS	Reserved	AISDIS	RLOSIS	QRPDIS
24	0xN07	RO	Reserved							
25	0xN08	R/W	Reserved	1SEG[6:0]						
26	0xN09	R/W	Reserved	2SEG[6:0]						
27	0xN0A	R/W	Reserved	3SEG[6:0]						
28	0xN0B	R/W	Reserved	4SEG[6:0]						
29	0xN0C	R/W	Reserved	5SEG[6:0]						
30	0xN0D	R/W	Reserved	6SEG[6:0]						
31	0xN0E	R/W	Reserved	7SEG[6:0]						
32	0xN0F	R/W	Reserved	8SEG[6:0]						
System Side Diagnostics										
33	0xN10	R/W	Reserved					SAISDIE	SRLOSIE	SQRPDIE
34	0xN11	RO	Reserved					SAISD	SRLOS	SQRPD
35	0xN12	RUR	Reserved					SAISDIS	SRLOSIS	SQRPDIS
36	0xN13	R/W	SQRSS/ SPRBS	RxTEST[1:0]		ALARM[2:0]			SINVPRBS	SINSBER
Device ID and Revision ID										
337	0x3FE	RO	**Device "ID"**							
338	0x3FF	RO	**Device "Revision ID"**							

7.3 Offset for Programming the Channel Number, N

The offset for programming the channel number can be added to the register value for determining the actual address. Address = Offset + Register Value. The offset is the following: Channel 0 = 0x020, Channel 1 = 0x040, Channel 2 = 0x060, Channel 3 = 0x080, Channel 4 = 0x0A0, Channel 5 = 0x0C0, Channel 6 = 0x0E0, Channel 7 = 0x100, Channel 8 = 0x120, Channel 9 = 0x140, Channel 10 = 0x160, Channel 11 = 0x180, Channel 12 = 0x1A0, Channel 13 = 0x1C0, Channel 14 = 0x1E0, and Channel 15 = 0x200.

Example: Channel 10, Register 0xN13 in Table 25, 0x160 + 0xN13 = 0x173. See Table 23 for more details.

7.4 Global Control Registers

TABLE 26: MICROPROCESSOR REGISTER 0X000H BIT DESCRIPTION

GLOBAL REGISTER (0X000H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	SR/$\overline{DR}$	**Single Rail/Dual Rail Mode** This bit sets the LIU to receive and transmit digital data in a single rail or a dual rail format. 0 = Dual Rail Mode 1 = Single Rail Mode ***NOTE:*** *Any time the LIU is used to generate diagnostic patterns, the part is automatically placed in SR mode. In addition, to detect diagnostic patterns, the LIU must be placed in SR mode by setting this bit to "1". This applies to both the Line Side and System Side.*	R/W	0
D6	ATAOS	**Line Automatic Transmit All Ones** If ATAOS is selected, an all ones pattern will be transmitted on TTIP/TRING for any channel that experiences an RLOS condition. If an RLOS condition does not occur, TAOS will remain inactive. 0 = Disabled 1 = Enabled	R/W	0
D5	RCLKE	**Receive Clock Data** 0 = RPOS/RNEG data is updated on the rising edge of RCLK 1 = RPOS/RNEG data is updated on the falling edge of RCLK	R/W	0
D4	TCLKE	**Transmit Clock Data** 0 = TPOS/TNEG data is sampled on the falling edge of TCLK 1 = TPOS/TNEG data is sampled on the rising edge of TCLK	R/W	0
D3	DATAP	**Data Polarity** 0 = Transmit input and receive output data is active "High" 1 = Transmit input and receive output data is active "Low"	R/W	0
D2	Reserved	This Register Bit is Not Used	R/W	0
D1	GIE	**Global Interrupt Enable** The global interrupt enable is used to enable/disable all interrupt activity for all 16 channels. This bit must be set "High" for the interrupt pin to operate. 0 = Disable all interrupt generation 1 = Enable interrupt generation to the individual channel registers	R/W	0
D0	SRESET	**Software Reset** Writing a "1" to this bit for more than 10µS initiates a device reset for all internal circuits except the microprocessor register bits. To reset the registers to their default setting, use the Hardware Reset pin (See the pin description for more details).	R/W	0

TABLE 27: MICROPROCESSOR REGISTER 0X001H BIT DESCRIPTION

GLOBAL REGISTER (0X001H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7 - D3	Reserved	These Register Bits are Not Used	R/W	0
D2	RxMUTE	**Receiver Output Mute Enable** If RxMUTE is selected, RPOS/RNEG will be pulled "Low" for any channel that experiences an RLOS condition. If an RLOS condition does not occur, RxMUTE will remain inactive. 0 = Disabled 1 = Enabled	R/W	0
D1	EXLOS	**Line Extended Loss of Zeros** The number of zeros required to declare a Digital Loss of Signal is extended to 4,096. 0 = Normal Operation 1 = Enables the EXLOS function	R/W	0
D0	ICT	**In Circuit Testing** 0 = Normal Operation 1 = Sets all output pins to "High" impedance for in circuit testing	R/W	0

TABLE 28: MICROPROCESSOR REGISTER 0X002H BIT DESCRIPTION

GLOBAL REGISTER (0X002H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	R/W	0
D6	RxTCNTL	**Receive Termination Select Control** This bit sets the LIU to control the RxTSEL function with either the individual channel register bit or the global hardware pin. 0 = Control of the receive termination is set to the register bits 1 = Control of the receive termination is set to the hardware pin	R/W	0
D[5:4]	Reserved	These Register Bits are Not Used	R/W	0
D3	SYS_EXLOS	**System Extended Loss of Zeros** The number of zeros required to declare a Digital Loss of Signal is extended to 4,096. 0 = Normal Operation 1 = Enables the SYS_EXLOS function	R/W	0
D[2:0]	Reserved	These Register Bits are Not Used	R/W	0

TABLE 29: MICROPROCESSOR REGISTER 0X003H BIT DESCRIPTION

GLOBAL REGISTER (0X003H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D[7:4]	Reserved	These Register Bits are Not Used	R/W	0
D3 D2	SL<1> SL<0>	**Slicer Level Select** 00 = 60% 01 = 65% 10 = 70% 11 = 55%	R/W	0 0
D[7:0]	Reserved	These Register Bits are Not Used	R/W	0

TABLE 30: MICROPROCESSOR REGISTER 0X004H BIT DESCRIPTION

GLOBAL REGISTER (0X004H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7 D6	MCLKT1out1 MCLKT1out0	**MCLKT1Nout Select** MclkT1out[1:0] is used to program the MCLKT1out pin. By default, the output clock is 1.544MHz. 00 = 1.544MHz 01 = 3.088MHz 10 = 6.176MHz 11 = 12.352MHz	R/W	0 0
D5 D4	MCLKE1out1 MCLKE1out0	**MCLKE1Nout Select** MclkE1out[1:0] is used to program the MCLKE1Nout pin. By default, the output clock is 2.048MHz. 00 = 2.048MHz 01 = 4.096MHz 10 = 8.192MHz 11 = 16.384MHz	R/W	0 0
D[3:0]	Reserved	These Register Bits are Not Used	R/W	0

TABLE 31: MICROPROCESSOR REGISTER 0X005H BIT DESCRIPTION

GLOBAL REGISTER (0X005H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	LCV_OFLW	**Line Code Violation / Counter Overflow Monitor Select** This bit is used to select the monitoring activity between the LCV and the counter overflow status. When the 16-bit LCV counter saturates, the counter overflow condition is activated. By default, the LCV activity is monitored by bit D4 in register 0xN05h. 0 = Monitoring LCV 1 = Monitoring the counter overflow status	R/W	0
D6	Reserved		R/W	0
D5	Reserved	This Register Bit is Not Used	R/W	0
D4	LCVen	**Line Code Violation Counter Enable** This bit is used to enable the LCV counters for all 16 channels within the device. By default, all 16 LCV counters are disabled. 0 = Disabled 1 = LCV Counters Enabled (For all 16 Channels)	R/W	0
D3 D2 D1 D0	LCVCH3 LCVCH2 LCVCH1 LCVCH0	**Line Code Violation Counter Select** These bits are used to select which channel is to be addressed for reading the contents in register 0x0007h (LSB) and 0x0008 (MSB). It is also used to address the counter for a given channel when performing an update or reset on a per channel basis. By default, Channel 0 is selected. 0000 = Channel 0 0001 = Channel 1 0010 = Channel 2 0011 = Channel 3 0100 = Channel 4 0101 = Channel 5 0110 = Channel 6 0111 = Channel 7 1000 = Channel 8 1001 = Channel 9 1010 = Channel 10 1011 = Channel 11 1100 = Channel 12 1101 = Channel 13 1110 = Channel 14 1111 = Channel 15	R/W	0 0 0 0

TABLE 32: MICROPROCESSOR REGISTER 0X006H BIT DESCRIPTION

GLOBAL REGISTER (0X006H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D[7:5]	Reserved	These Register Bits are Not Used	R/W	0
D4	allRST	**LCV Counter Reset for All Channels** This bit is used to reset all internal LCV counters to their default state 0x0000h. This bit must be set to "1" for 1μS. 0 = Normal Operation 1 = Resets all Counters	R/W	0
D3	allUPDATE	**LCV Counter Update for All Channels** This bit is used to latch the contents of all 16 counters into holding registers so that the value of each counter can be read. The channel is addressed by using bits D[3:0] in register 0x0005h. 0 = Normal Operation 1 = Updates all Counters	R/W	0
D2	Reserved	**This bit is not used**	R/W	0
D1	chUPDATE	**LCV Counter Update Per Channel** This bit is used to latch the contents of the counter for a given channel into a holding register so that the value of the counter can be read. The channel is addressed by using bits D[3:0] in register 0x0005h. 0 = Normal Operation 1 = Updates the Selected Channel	R/W	0
D0	ChRST	**LCV Counter Reset Per Channel** This bit is used to reset the LCV counter of a given channel to its default state 0x0000h. The channel is addressed by using bits D[3:0] in register 0x0005h. This bit must be set to "1" for 1μS. 0 = Normal Operation 1 = Resets the Selected Channel	R/W	0

TABLE 33: MICROPROCESSOR REGISTER 0X007H BIT DESCRIPTIO

GLOBAL REGISTER (0X007H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	LCVCNT7	**Line Code Violation Byte Contents[7:0]** These bits contain the LSB (bits [7:0]) of the LCV counter contents for a selected channel. The channel is addressed by using bits D[3:0] in register 0x0005h.	RO	0
D6	LCVCNT6			0
D5	LCVCNT5			0
D4	LCVCNT4			0
D3	LCVCNT3			0
D2	LCVCNT2			0
D1	LCVCNT1			0
D0	LCVCNT0			0

TABLE 34: MICROPROCESSOR REGISTER 0X008H BIT DESCRIPTION

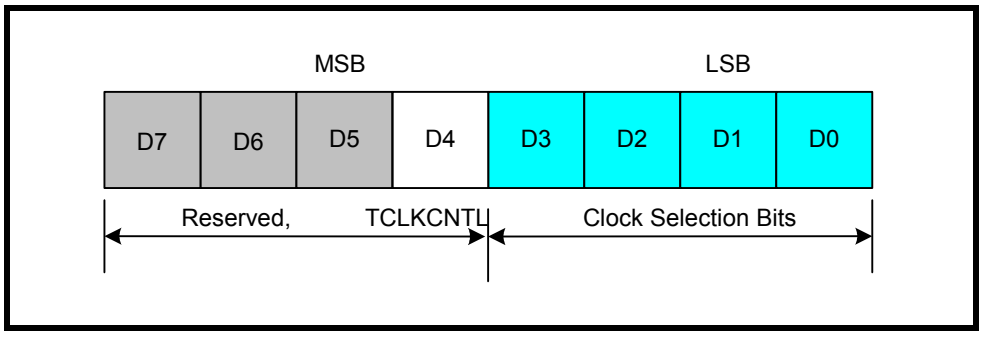
GLOBAL REGISTER (0X008H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	LCVCNT15	**Line Code Violation Byte Contents[15:8]**	RO	0
D6	LCVCNT14	These bits contain the MSB (bits [15:8]) of the LCV counter contents for a selected channel. The channel is addressed by using bits D[3:0] in register 0x0005h.		0
D5	LCVCNT13			0
D4	LCVCNT12			0
D3	LCVCNT11			0
D2	LCVCNT10			0
D1	LCVCNT9			0
D0	LCVCNT8			0

CLOCK SELECT REGISTER

The input clock source is used to generate all the necessary clock references internally to the LIU. The microprocessor timing is derived from a PLL output which is chosen by programming the Clock Select Bits in register 0x0009h. Therefore, if the clock selection bits are being programmed, the frequency of the PLL output will be adjusted accordingly. During this adjustment, it is important to "Not" write to any other bit location within the same register while selecting the input/output clock frequency. For best results, register 0x0009h can be broken down into two sub-registers with the MSB being bit D4 and the LSB being bits D[3:0] as shown in Figure 44.

NOTE: *Bits D[7:5] are reserved.*

FIGURE 44. REGISTER 0X0009H SUB REGISTERS



Programming Examples:

Example 1: Changing bits D[7:4]

If bit D4 is the only values within the register that will change in a WRITE process, the microprocessor only needs to initiate ONE write operation.

Example 2: Changing bits D[3:0]

If bits D[3:0] are the only values within the register that will change in a WRITE process, the microprocessor only needs to initiate ONE write operation.

Example 3: Changing bits within the MSB and LSB

In this scenario, one must initiate TWO write operations such that the MSB and LSB do not change within ONE write cycle. It is recommended that the MSB and LSB be treated as two independent sub-registers. One can either change the clock selection bits D[3:0] (LSB) and then change bit D4 (MSB) on the SECOND write, or vice-versa. No order or sequence is necessary.

TABLE 35: MICROPROCESSOR REGISTER 0X009H BIT DESCRIPTION

GLOBAL REGISTER (0X009H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7 - D5	Reserved	These Register Bits are Not Used	R/W	0
D4	TCLKCNL	**Transmit Clock Control** When this bit is pulled "High" and there is no TCLK signal present on the transmit input path, TTIP/TRING will Transmit All "Ones" (TAOS). By default, TTIP/TRING will Transmit All Zeros. 0 = All Zeros 1 = All Ones	R/W	0
D3 D2 D1 D0	CLKSEL3 CLKSEL2 CLKSEL1 CLKSEL0	**Clock Input Select** CLKSEL[3:0] is used to select the input clock source used as the internal timing reference. 0000 = 2.048 MHz 0001 = 1.544 MHz 1000 = 4.096 Mhz 1001 = 3.088 Mhz 1010 = 8.192 Mhz 1011 = 6.176 Mhz 1100 = 16.384 Mhz 1101 = 12.352 Mhz 1110 = 2.048 Mhz 1111 = 1.544 Mhz	R/W	0 0 0 0

TABLE 36: MICROPROCESSOR REGISTER 0X00AH BIT DESCRIPTION

GLOBAL REGISTER (0X00AH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	GCHIS7	**Global Channel Interrupt Status for Channel 7** 0 = No interrupt activity from channel 7 1 = Interrupt was generated from channel 7	RUR	0
D6	GCHIS6	**Global Channel Interrupt Status for Channel 6** 0 = No interrupt activity from channel 6 1 = Interrupt was generated from channel 6	RUR	0
D5	GCHIS5	**Global Channel Interrupt Status for Channel 5** 0 = No interrupt activity from channel 5 1 = Interrupt was generated from channel 5	RUR	0
D4	GCHIS4	**Global Channel Interrupt Status for Channel 4** 0 = No interrupt activity from channel 4 1 = Interrupt was generated from channel 4	RUR	0

TABLE 36: MICROPROCESSOR REGISTER 0X00AH BIT DESCRIPTION

GLOBAL REGISTER (0X00AH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D3	GCHIS3	**Global Channel Interrupt Status for Channel 3** 0 = No interrupt activity from channel 3 1 = Interrupt was generated from channel 3	RUR	0
D2	GCHIS2	**Global Channel Interrupt Status for Channel 2** 0 = No interrupt activity from channel 2 1 = Interrupt was generated from channel 2	RUR	0
D1	GCHIS1	**Global Channel Interrupt Status for Channel 1** 0 = No interrupt activity from channel 1 1 = Interrupt was generated from channel 1	RUR	0
D0	GCHIS0	**Global Channel Interrupt Status for Channel 0** 0 = No interrupt activity from channel 0 1 = Interrupt was generated from channel 0	RUR	0

TABLE 37: MICROPROCESSOR REGISTER 0X00BH BIT DESCRIPTION

GLOBAL REGISTER (0X00BH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	GCHIS15	**Global Channel Interrupt Status for Channel 15** 0 = No interrupt activity from channel 15 1 = Interrupt was generated from channel 15	RUR	0
D6	GCHIS14	**Global Channel Interrupt Status for Channel 14** 0 = No interrupt activity from channel 14 1 = Interrupt was generated from channel 14	RUR	0
D5	GCHIS13	**Global Channel Interrupt Status for Channel 13** 0 = No interrupt activity from channel 13 1 = Interrupt was generated from channel 13	RUR	0
D4	GCHIS12	**Global Channel Interrupt Status for Channel 12** 0 = No interrupt activity from channel 12 1 = Interrupt was generated from channel 12	RUR	0
D3	GCHIS11	**Global Channel Interrupt Status for Channel 11** 0 = No interrupt activity from channel 11 1 = Interrupt was generated from channel 11	RUR	0
D2	GCHIS10	**Global Channel Interrupt Status for Channel 10** 0 = No interrupt activity from channel 10 1 = Interrupt was generated from channel 10	RUR	0

TABLE 37: MICROPROCESSOR REGISTER 0X00BH BIT DESCRIPTION

GLOBAL REGISTER (0X00BH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D1	GCHIS9	**Global Channel Interrupt Status for Channel 9** 0 = No interrupt activity from channel 9 1 = Interrupt was generated from channel 9	RUR	0
D0	GCHIS8	**Global Channel Interrupt Status for Channel 8** 0 = No interrupt activity from channel 8 1 = Interrupt was generated from channel 8	RUR	0

TABLE 38: RECOVERED CLOCK SELECT 0X00CH BIT DESCRIPTION

RECOVERED CLOCK SELECT REGISTER (0X00CH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D[7:5]	Reserved			
D[4:0]	RCLKOUT	**Recovered Clock Select** These register bits are used to select the recovered clock from one of the RCLK[15:0] lines and output it on the RCLKOUT pin.	R/W	0

Recovered Clock Select [4:0]	Selected RCLK
0XXXX	Input
10000	RCLK0
10001	RCLK1
10010	RCLK2
10011	RCLK3
10100	RCLK4
10101	RCLK5
10110	RCLK6
10111	RCLK7
11000	RCLK8
11001	RCLK9
11010	RCLK10
11011	RCLK11
11100	RCLK12
11101	RCLK13
11110	RCLK14
11111	RCLK15

TABLE 39: GPIO SELECT 0X00DH BIT DESCRIPTION

GPIO SELECT REGISTER (0X00DH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7 D6	GPIODIR1 GPIODIR0	**GPIO Direction Select** These bits select the direction of the external GPIO pins on the LIU. These pins can be used for general purpose. By default, the hardware pins are set as inputs. 0 = Input 1 = Output	R/W	0 0
D5 D4	GPIO1 GPIO0	**GPIO Control Status** These pins are used to set/monitor the GPIO pins. If the direction is input, then these bits monitor the GPIO hardware pins. If the direction is output, then these bits set the status of the output pins.	R/W	0 0
D[3:0]	Reserved	**These bits are reserved**		

TABLE 40: RESERVED REGISTER 0X00EH BIT DESCRIPTION

RESERVED REGISTER (0X00EH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D[7:0]	Reserved	**These bits are reserved**		

TABLE 41: RESERVED 0X00FH BIT DESCRIPTION

RESERVED REGISTER (0X00FH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D[7:0]	Reserved	**These bits are reserved**		

7.5 Control and Line Side Diagnostic Registers

TABLE 42: MICROPROCESSOR REGISTER 0XN00H BIT DESCRIPTION

CHANNEL N (0XN00H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	QRSS/PRBS	**QRSS/PRBS Select Bits** These bits are used to select between QRSS and PRBS. 0 = PRBS 1 = QRSS	R/W	0
D6	Reserved	**This Bit is Reserved**	R/W	0
D5	RxON	**Receiver ON/OFF** Upon power up, the receiver is powered OFF. RxON is used to turn the receiver ON or OFF if the hardware pin RxON is pulled "High". If the hardware pin is pulled "Low", all receivers are turned off. 0 = Receiver is Powered Off 1 = Receiver is Powered On	R/W	0
D4 D3 D2 D1 D0	EQC4 EQC3 EQC2 EQC1 EQC0	**Cable Length Settings** The Cable Length Settting bits are shown in Table 43 below.	R/W	0 0 0 0 0

TABLE 43: CABLE LENGTH SETTINGS

EQC[4:0]	T1/E1 MODE/RECEIVE SENSITIVITY	TRANSMIT LBO	CABLE	CODING
0x08h	T1 Short Haul	0 to 133 feet (0.6dB)	100Ω TP	B8ZS
0x09h	T1 Short Haul	133 to 266 feet (1.2dB)	100Ω TP	B8ZS
0x0Ah	T1 Short Haul	266 to 399 feet (1.8dB)	100Ω TP	B8ZS
0x0Bh	T1 Short Haul	399 to 533 feet (2.4dB)	100Ω TP	B8ZS
0x0Ch	T1 Short Haul	533 to 655 feet (3.0dB)	100Ω TP	B8ZS
0x0Dh	T1 Short Haul	Arbitrary Pulse	100Ω TP	B8ZS
0x1Ch	E1 Short Haul	ITU G.703	75Ω Coax	HDB3
0x1Dh	E1 Short Haul	ITU G.703	120Ω TP	HDB3

TABLE 44: MICROPROCESSOR REGISTER 0XN01H BIT DESCRIPTION

<table>
<tr><th colspan="5">CHANNEL N (0XN01H)</th></tr>
<tr><th>BIT</th><th>NAME</th><th>FUNCTION</th><th>Register Type</th><th>Default Value (HW reset)</th></tr>
<tr><td>D7</td><td>RxTSEL</td><td>Receive Termination Select
Upon power up, the receiver is in "High" impedance. RxTSEL is used to switch between the internal termination and "High" impedance.
0 = External Termination
1 = Internal Termination</td><td>R/W</td><td>0</td></tr>
<tr><td>D6</td><td>TxTSEL</td><td>Transmit Termination Select
Upon power up, the transmitter is in "High" impedance. TxTSEL is used to switch between the internal termination and "High" impedance.
0 = "High" Impedance
1 = Internal Termination</td><td>R/W</td><td>0</td></tr>
<tr><td>D5
D4</td><td>TERSEL1
TERSEL0</td><td>Receive Line Impedance Select
TERSEL[1:0] are used to select the line impedance for T1/J1/E1.
<table><tr><th>TERSEL1</th><th>TERSEL0</th><th>LINE IMPEDANCE</th></tr><tr><td>0</td><td>0</td><td>100Ω</td></tr><tr><td>0</td><td>1</td><td>110Ω</td></tr><tr><td>1</td><td>0</td><td>75Ω</td></tr><tr><td>1</td><td>1</td><td>120Ω</td></tr></table></td><td>R/W</td><td>0
0</td></tr>
<tr><td>D3
D2</td><td>JASEL1
JASEL0</td><td>Jitter Attenuator Select
JASEL[1:0] are used to enable the jitter attenuator in the receive or transmit path. By default, the jitter attenuator is disabled.
<table><tr><th>JASEL1</th><th>JASEL0</th><th>JA PATH</th></tr><tr><td>0</td><td>0</td><td>Disabled</td></tr><tr><td>0</td><td>1</td><td>Transmit Path</td></tr><tr><td>1</td><td>0</td><td>Receive Path</td></tr><tr><td>1</td><td>1</td><td>Receive Path</td></tr></table></td><td>R/W</td><td>0</td></tr>
</table>

TABLE 44: MICROPROCESSOR REGISTER 0XN01H BIT DESCRIPTION

CHANNEL N (0XN01H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D1	JABW	**Jitter Bandwidth (E1 Mode Only, T1 is permanently set to 3Hz)** The jitter bandwidth is a global setting that is applied to both the receiver and transmitter jitter attenuator. 0 = 10Hz 1 = 1.5Hz	R/W	0
D0	FIFOS	**FIFO Depth Select** The FIFO depth select is used to configure the part for a 32-bit or 64-bit FIFO (within the jitter attenuator blocks). The delay of the FIFO is equal to ½ the FIFO depth. This is a global setting that is applied to both the receiver and transmitter FIFO. 0 = 32-Bit 1 = 64-Bit	R/W	0

TABLE 45: MICROPROCESSOR REGISTER 0XN02H BIT DESCRIPTION

CHANNEL N (0XN02H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	INVQRSS	**QRSS inversion** INVQRSS is used to invert the transmit QRSS or PRBS pattern set by the TxTEST[2:0] bits. By default (bit D7=0), INVQRSS is disabled for PRBS and enabled for QRSS. 0 = Disabled for PRBS 0 = Enabled for QRSS 1 = Disabled for QRSS 1 = Enabled for PRBS	R/W	0
D6 D5 D4	TxTEST2 TxTEST1 TxTEST0	**Test Code Pattern** TxTEST[2:0] are used to select a diagnostic test pattern to the line side (transmit outputs). If these bits are selected, the LIU is automatically placed in single rail mode. 0XX = No Pattern 100 = Tx QRSS 101 = Tx TAOS 110 = Tx LOS (All Zeros) 111 = Reserved	R/W	0 0 0

TABLE 45: MICROPROCESSOR REGISTER 0XN02H BIT DESCRIPTION

CHANNEL N (0XN02H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D3	TxOn	**Transmit ON/OFF** Upon power up, the transmitters are powered off. This bit is used to turn the transmitter for this channel On or Off if the TxON pin is pulled "High". If the TxON pin is pulled "Low", all 16 transmitters are powered off. 0 = Transmitter is Powered OFF 1 = Transmitter is Powered ON	R/W	0
D2 D1 D0	LOOP2 LOOP1 LOOP0	**Loopback Diagnostic Select** LOOP[2:0] are used to select the loopback mode. 0XX = No Loopback 100 = Dual Loopback 101 = Analog Loopback 110 = Remote Loopback 111 = Digital Loopback	R/W	0 0 0

TABLE 46: MICROPROCESSOR REGISTER 0XN03H BIT DESCRIPTION

CHANNEL N (0XN03H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7 D6	RxRES1 RxRES0	**Receive External Fixed Resistor** RxRES[1:0] are used to select the value for a high precision external resistor to improve return loss. 00 = None 01 = 240Ω 10 = 210Ω 11 = 150Ω	R/W	0 0
D5	CODES	**Encoding/Decoding Select (Single Rail Mode Only)** 0 = HDB3 (E1), B8ZS (T1) 1 = AMI Coding	R/W	0
D4	Reserved	**This Bit is Reserved**		
D3	E1Arben	**E1 Arbitrary Pulse Enable** This bit is used to enable the Arbitrary Pulse Generator for shaping the transmit pulse shape when E1 mode is selected. If this bit is set to "1", this channel will be configured for the Arbitrary Mode. Each channel is individually controlled by programming the channel registers 0xN08 through 0xN0F, where n is the number of the channel. "0" = Disabled (Normal E1 Pulse Shape ITU G.703) "1" = Arbitrary Pulse Enabled	R/W	0

TABLE 46: MICROPROCESSOR REGISTER 0XN03H BIT DESCRIPTION

CHANNEL N (0XN03H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D2	INSBPV	**Insert Bipolar Violation** When this bit transitions from a "0" to a "1", a bipolar violation will be inserted in the transmitted data from TPOS, QRSS/PRBS pattern. The state of this bit will be sampled on the rising edge of TCLK. To ensure proper operation, it is recommended to write a "0" to this bit before writing a "1".	R/W	0
D1	INSBER	**Insert Bit Error** When this bit transitions from a "0" to a "1", a bit error will be inserted in the transmitted QRSS/PRBS pattern. The state of this bit will be sampled on the rising edge of TCLK. To ensure proper operation, it is recommended to write a "0" to this bit before writing a "1".	R/W	0
D0	Reserved	**This Bit is Reserved**	R/W	0

TABLE 47: MICROPROCESSOR REGISTER 0XN04H BIT DESCRIPTION

CHANNEL N (0XN04H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D7	Reserved	**This Bit is Reserved**	R/W	0
D6	DMOIE	**Digital Monitor Output Interrupt Enable** 0 = Masks the DMO function 1 = Enables Interrupt Generation	R/W	0
D5	FLSIE	**FIFO Limit Status Interrupt Enable** 0 = Masks the FLS function 1 = Enables Interrupt Generation	R/W	0
D4	LCV_OFIE	**Line Code Violation / Counter Overflow Interrupt Enable** 0 = Masks the LCV_OF function 1 = Enables Interrupt Generation	R/W	0
D3	Reserved	**This Bit is Reserved**	R/W	0
D2	AISDIE	**Alarm Indication Signal Detection Interrupt Enable** 0 = Masks the AIS function 1 = Enables Interrupt Generation	R/W	0
D1	RLOSIE	**Receiver Loss of Signal Interrupt Enable** 0 = Masks the RLOS function 1 = Enables Interrupt Generation	R/W	0
D0	QRPDIE	**Quasi Random Pattern Detect Interrupt Enable** 0 = Masks the QRPD function 1 = Enables Interrupt Generation	R/W	0

NOTE: The GIE bit in the global register 0x0000h must be set to "1" in addition to the individual register bits to enable the interrupt pin.

TABLE 48: MICROPROCESSOR REGISTER 0XN05H BIT DESCRIPTION

CHANNEL N (0XN05H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	**This Bit is Reserved**	RO	0
D6	DMO	**Digital Monitor Output** The digital monitor output is always active regardless if the interrupt generation is disabled. This bit indicates the DMO activity. An interrupt will not occur unless the DMOIE is set to "1" in the channel register 0xN04h and GIE is set to "1" in the global register 0x0000h. 0 = No Alarm 1 = Transmit output driver has failures	RO	0
D5	FLS	**FIFO Limit Status** The FIFO limit status is always active regardless if the interrupt generation is disabled. This bit indicates whether the RD/WR pointers are within 3-Bits. An interrupt will not occur unless the FLSIE is set to "1" in the channel register 0xN04h and GIE is set to "1" in the global register 0x0000h. 0 = No Alarm 1 = RD/WR FIFO pointers are within ±3-Bits	RO	0
D4	LCV_OF	**Line Code Violation / Counter Overflow** This bit serves a dual purpose. By default, this bit monitors the line code violation activity. However, if bit 7 in register 0x0005h is set to a "1", this bit monitors the overflow status of the internal LCV counter. An interrupt will not occur unless the LCV_OFIE is set to "1" in the channel register 0xN04h and GIE is set to "1" in the global register 0x0000h. 0 = No Alarm 1 = A line code violation, bipolar violation, or excessive zeros has occurred	RO	0
D3	Reserved	**This Bit is Reserved**	RO	0
D2	AISD	**Alarm Indication Signal Detection** The alarm indication signal detection is always active regardless if the interrupt generation is disabled. This bit indicates the AIS activity. An interrupt will not occur unless the AISIE is set to "1" in the channel register 0xN04h and GIE is set to "1" in the global register 0x0000h. 0 = No Alarm 1 = An all ones signal is detected	RO	0

NOTE: The GIE bit in the global register 0x0000h must be set to "1" in addition to the individual register bits to enable the interrupt pin.

TABLE 48: MICROPROCESSOR REGISTER 0XN05H BIT DESCRIPTION

CHANNEL N (0XN05H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D1	RLOS	**Receiver Loss of Signal** The receiver loss of signal detection is always active regardless if the interrupt generation is disabled. This bit indicates the RLOS activity. An interrupt will not occur unless the RLOSIE is set to "1" in the channel register 0xN04h and GIE is set to "1" in the global register 0x0000h. 0 = No Alarm 1 = An RLOS condition is present	RO	0
D0	QRPD	**Quasi Random Pattern Detection** The quasi random pattern detection is always active regardless if the interrupt generation is disabled. This bit indicates that a QRPD has been detected. An interrupt will not occur unless the QRPDIE is set to "1" in the channel register 0xN04h and GIE is set to "1" in the global register 0x0000h. 0 = No Alarm 1 = A QRP is detected	RO	0

TABLE 49: MICROPROCESSOR REGISTER 0XN06H BIT DESCRIPTION

CHANNEL N (0XN06H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	**This Bit is Reserved**	RUR	0
D6	DMOIS	**Digital Monitor Output Interrupt Status** 0 = No change 1 = Change in status occurred	RUR	0
D5	FLSIS	**FIFO Limit Interrupt Status** 0 = No change 1 = Change in status occurred	RUR	0
D4	LCV_OFIS	**Line Code Violation / Overflow Interrupt Status** 0 = No change 1 = Change in status occurred	RUR	0
D3	Reserved	**This Bit is Reserved**	RUR	0
D2	AISDIS	**Alarm Indication Signal Detection Interrupt Status** 0 = No change 1 = Change in status occurred	RUR	0

TABLE 49: MICROPROCESSOR REGISTER 0XN06H BIT DESCRIPTION

CHANNEL N (0XN06H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D1	RLOSIS	**Receiver Loss of Signal Interrupt Status** 0 = No change 1 = Change in status occurred	RUR	0
D0	QRPDIS	**Quasi Random Pattern Detection Interrupt Status** 0 = No change 1 = Change in status occurred	RUR	0

NOTE: *Any change in status will generate an interrupt (if enabled in channel register 0xN04h and GIE is set to "1" in the global register 0x0000h). The status registers are reset upon read (RUR).*

TABLE 50: MICROPROCESSOR REGISTER 0XN07H BIT DESCRIPTION

CHANNEL N (0XN07H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D[7:0]	Reserved	**These Bits are Reserved**	RO	0

TABLE 51: MICROPROCESSOR REGISTER 0XN08H BIT DESCRIPTION

CHANNEL N (0XN08H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	0
D6 D5 D4 D3 D2 D1 D0	1SEG6 1SEG5 1SEG4 1SEG3 1SEG2 1SEG1 1SEG0	**Arbitrary Pulse Generation** The transmit output pulse is divided into 8 individual segments. This register is used to program the first segment which corresponds to the overshoot of the pulse amplitude. There are four segments for the top portion of the pulse and four segments for the bottom portion of the pulse. Segment number 5 corresponds to the undershoot of the pulse. The MSB of each segment is the sign bit. Bit 6 = 0 = Negative Direction Bit 6 = 1 = Positive Direction	R/W	0 0 0 0 0 0 0

TABLE 52: MICROPROCESSOR REGISTER 0XN09H BIT DESCRIPTION

CHANNEL N (0XN09H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	0
D[6:0]	2SEG[6:0]	**Segment Number Two, Same Description as Register 0xN08h**	R/W	

TABLE 53: MICROPROCESSOR REGISTER 0XN0AH BIT DESCRIPTION

CHANNEL N (0XN0AH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	0
D[6:0]	3SEG[6:0]	**Segment Number Three, Same Description as Register 0xN08h**	R/W	

TABLE 54: MICROPROCESSOR REGISTER 0XN0BH BIT DESCRIPTION

CHANNEL N (0XN0BH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	0
D[6:0]	4SEG[6:0]	**Segment Number Four, Same Description as Register 0xN08h**	R/W	

TABLE 55: MICROPROCESSOR REGISTER 0XN0CH BIT DESCRIPTION

CHANNEL N (0XN0CH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	0
D[6:0]	5SEG[6:0]	**Segment Number Five, Same Description as Register 0xN08h**	R/W	

TABLE 56: MICROPROCESSOR REGISTER 0XN0DH BIT DESCRIPTION

CHANNEL N (0XN0DH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	0
D[6:0]	6SEG[6:0]	**Segment Number Six, Same Description as Register 0xN08h**	R/W	

TABLE 57: MICROPROCESSOR REGISTER 0XN0EH BIT DESCRIPTION

CHANNEL N (0XN0EH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	0
D[6:0]	7SEG[6:0]	**Segment Number Seven, Same Description as Register 0xN08h**	R/W	

TABLE 58: MICROPROCESSOR REGISTER 0XN0FH BIT DESCRIPTION

CHANNEL N (0XN0FH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	0
D[6:0]	8SEG[6:0]	**Segment Number Eight, Same Description as Register 0xN08h**	R/W	

7.6 System Side Diagnostic Channel Control Registers

TABLE 59: SYSTEM SIDE INTERRUPT ENABLE REGISTER (0XN10H)

SYSTEM SIDE INTERRUPT ENABLE REGISTER (0XN10H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D[7:3]	Reserved	**These Bits are Reserved**		
D2	SAISDIE	**System Side Alarm Indication Signal Detection Interrupt Enable** 0 = Masks the SAIS function 1 = Enables Interrupt Generation	R/W	0
D1	SRLOSIE	**System Side Receiver Loss of Signal Interrupt Enable** 0 = Masks the SRLOS function 1 = Enables Interrupt Generation	R/W	0
D0	SQRPDIE	**System Side Quasi Random Pattern Detect Interrupt Enable** 0 = Masks the SQRPD function 1 = Enables Interrupt Generation	R/W	0

TABLE 60: SYSTEM SIDE INTERRUPT DETECTION REGISTER (0XN11H)

SYSTEM SIDE INTERRUPT DETECTION REGISTER (0XN11H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D[7:3]	Reserved	**These Bits are Reserved**		
D2	SAISD	**System Side Alarm Indication Signal Detection** The alarm indication signal detection is always active regardless if the interrupt generation is disabled. This bit indicates the SAIS activity. An interrupt will not occur unless the SAISIE is set to "1" in the channel register 0xN10h and GIE is set to "1" in the global register 0x0000h. 0 = No Alarm 1 = An all ones signal is detected	RO	0

TABLE 60: SYSTEM SIDE INTERRUPT DETECTION REGISTER (0XN11H)

SYSTEM SIDE INTERRUPT DETECTION REGISTER (0XN11H)				
D1	SRLOS	**System Side Receiver Loss of Signal** The transmitter loss of signal detection is always active regardless if the interrupt generation is disabled. This bit indicates the SRLOS activity. An interrupt will not occur unless the SRLOSIE is set to "1" in the channel register 0xN10h and GIE is set to "1" in the global register 0x0000h. 0 = No Alarm 1 = AN SRLOS condition is present	RO	0
D0	SQRPD	**System Side Quasi Random Pattern Detection** The quasi random pattern detection is always active regardless if the interrupt generation is disabled. This bit indicates that a SQRPD has been detected. An interrupt will not occur unless the SQRPDIE is set to "1" in the channel register 0xN10h and GIE is set to "1" in the global register 0x0000h. 0 = No Alarm 1 = A SQRP is detected	RO	0

TABLE 61: SYSTEM SIDE INTERRUPT STATUS REGISTER (0XN12H)

SYSTEM SIDE INTERRUPT STATUS REGISTER (0XN12H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D[7:3]	Reserved	**These Bits are Reserved**		
D2	SAISDIS	**System Side Alarm Indication Signal Detection Interrupt Status** 0 = No change 1 = Change in status occurred	RUR	0
D1	SRLOSIS	**System Side Receiver Loss of Signal Interrupt Status** 0 = No change 1 = Change in status occurred	RUR	0
D0	SQRPDIS	**System Side Quasi Random Pattern Detection Interrupt Status** 0 = No change 1 = Change in status occurred	RUR	0

TABLE 62: SYSTEM SIDE TEST PATTERN SELECT REGISTER 0XN13H BIT DESCRIPTION

SYSTEM SIDE TEST PATTERN SELECT REGISTER (0XN13H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	SQRSS/ SPRBS	**System QRSS/PRBS Select Bits** These bits are used to select between QRSS and PRBS for the system side interface. 0 = PRBS 1 = QRSS	R/W	0
D6 D5	RxTEST1 RxTEST0	**Receive System Side Test Code Pattern** RxTEST[2:0] are used to select a diagnostic test pattern to the system side (receive outputs). If these bits are selected, the LIU is automatically placed in single rail mode. 00 = RTip/Rring 01 = Rx SAIS 10 = Rx SLOS (All Zeros) 11 = Rx SQRSS/SPRBS	R/W	0 0 0
D4 D3 D2	ALARM2 ALARM1 ALARM0	**Alarm Report Output (Pin RNEG, SR mode Only)** These bits are used to select which alram will be reported to the RNEG pin in single rail mode. 000 = LCV/EXZ 001 = Line AIS 010 = Line QRPD 011 = Line RLOS 100 = System SAIS 101 = System SQRPD/SPRPD 110 = System SLOS 111 = GND	R/W	0 0 0
D1	SINVPRBS	**System Invert PRBS/QRSS** This bit is used to select between a normal test pattern or inverted test pattern whenever the PRBS/QRSS is selected. 0 = Normal 1 = Inverted PRBS/QRSS		
D0	SINSBER	**System Insert Bit Error** When this bit transitions from a "0" to a "1", a bit error will be inserted in the Received QRSS/PRBS pattern. The state of this bit will be updated on the rising edge of RCLK. To ensure proper operation, it is recommended to write a "0" to this bit before writing a "1".	R/W	0

TABLE 63: MICROPROCESSOR REGISTER 0X3FEH BIT DESCRIPTION

DEVICE "ID" REGISTER (0X3FEH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Device "ID"	The device "ID" of the XRT83VSH316 short haul LIU is 0xE8h. Along with the revision "ID", the device "ID" is used to enable software to identify the silicon adding flexibility for system control and debug.	RO	1
D6				1
D5				1
D4				0
D3				1
D2				0
D1				0
D0				0

TABLE 64: MICROPROCESSOR REGISTER 0X3FFH BIT DESCRIPTION

REVISION "ID" REGISTER (0X3FFH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Revision "ID"	The revision "ID" of the XRT83VSH316 LIU is used to enable software to identify which revision of silicon is currently being tested. The revision "ID" for the first revision of silicon will be 0x01h. ***NOTE:*** *The value contained in this register is subject to change when a newer revision of the silicon has been issued.*	RO	0
D6				0
D5				0
D4				0
D3				0
D2				0
D1				0
D0				1

8.0 ELECTRICAL CHARACTERISTICS

TABLE 65: ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C
Supply Voltage	-0.5V to +3.8V
Vin	-0.5V to +5.5V
Maximum Junction Temperature	125°C
Theta Ja (No Air Flow)	20 °C/W
Theta Ja (100 lfpm, 0.5 m/s)	17.2 °C/W
Theta Ja (200 lfpm, 1.0 m/s)	16.0 °C/W
Theta Ja (400 lfpm, 2.0 m/s)	14.8 °C/W
Theta Jc	9.5 °C/W

TABLE 66: DC DIGITAL INPUT AND OUTPUT ELECTRICAL CHARACTERISTICS

VDD=3.3V ±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**
Power Supply Voltage	VDD	3.13	3.3	3.46	V
Input High Voltage	V_{IH}	2.0	-	5.0	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Output High Voltage IOH=-2.0mA	V_{OH}	2.4	-		V
Output Low Voltage IOL=2.0mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_L	-	-	±10	µA
Input Capacitance	C_I	-	5.0		pF
Output Lead Capacitance	C_L	-	-	25	pF

NOTE: *Input leakage current excludes pins that are internally pulled "Low" or "High"*

TABLE 67: AC ELECTRICAL CHARACTERISTICS

VDD=3.3V ±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**
MCLKin Clock Duty Cycle		40	-	60	%
MCLKin Clock Tolerance		-	±50	-	ppm

TABLE 68: POWER CONSUMPTION

VDD=3.3V ±5%, T_A=25°C, INTERNAL IMPEDANCE, UNLESS OTHERWISE SPECIFIED								
MODE	SUPPLY VOLTAGE	IMPEDANCE	RECEIVER	TRANSMITTER	TYP	MAX	UNIT	TEST CONDITION
E1	3.3V	75Ω	1:1	1:2	2.8	3.6	W	100% ones
E1	3.3V	120Ω	1:1	1:2	2.5	3.3	W	100% ones
T1	3.3V	100Ω	1:1	1:2	2.9	4.0	W	100% ones
NOTE: The typical power consumption of the 1.8V supply represents ~ 82mW of the above listed.								

TABLE 69: E1 RECEIVER ELECTRICAL CHARACTERISTICS

(VDD=3.3V±5%, TA=25°C UNLESS OTHERWISE SPECIFIED)					
PARAMETER	MIN	TYP.	MAX	UNIT	TEST CONDITIONS
Receiver loss of signal:					
Number of consecutive zeros before LOS is set	-	32	-	bit	Cable attenuation @1024KHz ITU-G.775, ETS1 300 233
Input signal level at LOS	13	16	-	dB	
RLOS Clear	12.5	-	-	% ones	
Receiver Sensitivity	9	-	-	dB	With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω application.
Interference Margin	-18	-14	-	dB	With 6dB cable loss
Input Impedance	15		-	KΩ	
Jitter Tolerance: 1 Hz 10KHz---100KHz	 37 0.3	 - -	 - -	 UIpp UIpp	 ITU G.823
Recovered Clock Jitter Transfer Corner Frequency Peaking Amplitude	-	20	36 0.5	KHz dB	ITU G.736
Jitter Attenuator Corner Frequency(-3dB curve) JABW=0 JSBW=1	 - -	 10 1.5	 - -	 Hz Hz	ITU G.736
Return Loss: 51KHz --- 102KHz 102KHz --- 2048KHz 2048KHz --- 3072KHz	 12 8 8	 - - -	 - - -	 dB dB dB	 ITU G.703

TABLE 70: T1 RECEIVER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=25°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
Receiver loss of signal:					
Number of consecutive zeros before RLOS is set		175			
Input signal level at RLOS	13	16	-	dB	Cable attenuation @772kHz
RLOS Clear	12.5	-	-	% ones	ITU-G.775, ETSI 300 233
Receiver Sensitivity	9	-	-	dB	With nominal pulse amplitude of 3.0V for 100Ω termination
Interference Margin	-18	-14	-	dB	With 6db of cable loss
Input Impedance	15	-	-	kW	
Jitter Tolerance: 1Hz 10kHz - 100kHz	 138 0.4	 - -	 - -	 UIpp	 AT&T Pub 62411
Recovered Clock Jitter Transfer Corner Frequency Peaking Amplitude	 - -	 10	 - 0.1	 KHz dB	 TR-TSY-000499
Jitter Attenuator Corner Frequency (-3dB curve)	-	3		Hz	AT&T Pub 62411
Return Loss: 51kHz - 102kHz 102kHz - 2048kHz 2048kHz - 3072kHz	 14 20 16	 - - -	 - - -	 dB dB dB	

TABLE 71: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD=3.3V ±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**	**TEST CONDITION**
AMI Output Pulse Amplitude 75Ω 120Ω	 2.13 2.70	 2.37 3.00	 2.60 3.30	 V V	 1:2 Transformer
Output Pulse Width	224	244	264	ns	
Output Pulse Width Ratio	0.95	-	1.05		ITU-G.703
Output Pulse Amplitude Ratio	0.95	-	1.05		ITU-G.703

TABLE 71: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD=3.3V ±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**	**TEST CONDITION**
Jitter Added by the Transmitter Output	-	0.025	0.05	UI_{p-p}	Broad Band with jitter free TCLK applied to the input.
Output Return Loss					
51kHz - 102kHz	15	-	-	dB	ETSI 300 166
102kHz - 2048kHz	9	-	-	dB	
2048kHz - 3072kHz	8	-	-	dB	

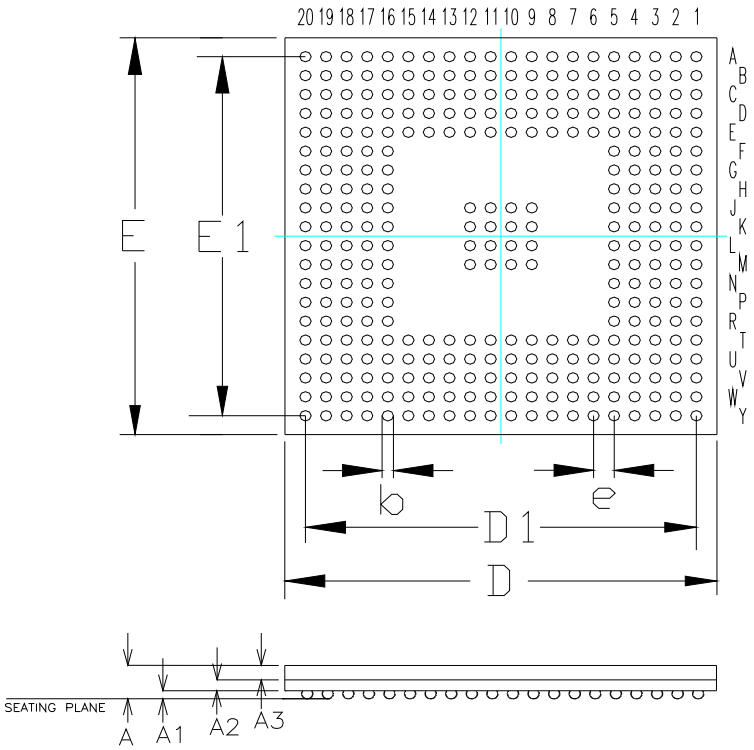
TABLE 72: T1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD=3.3V ±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**	**TEST CONDITION**
AMI Output Pulse Amplitude	2.4	3.0	3.6	V	1:2 Transformer measured at DSX-1
Output Pulse Width	338	350	362	ns	ANSI T1.102
Output Pulse Width Imbalance	-	-	20		ANSI T1.102
Output Pulse Amplitude Imbalance	-	-	±200	mV	ANSI T1.102
Jitter Added by the Transmitter Output	-	0.025	0.05	UI_{p-p}	Broad Band with jitter free TCLK applied to the input.
Output Return Loss					
51kHz - 102kHz	17	-	-	dB	
102kHz - 2048kHz	12	-	-	dB	
2048kHz - 3072kHz	10	-	-	dB	

ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT83VSH316IB-F	316 Shrink Thin Ball Grid Array (21.0 mm x 21.0 mm, STBGA)	-40°C to +85°C

PACKAGE DIMENSIONS (BOTTOM VIEW)



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.056	0.067	1.41	1.69
A1	0.011	0.015	0.28	0.38
A2	0.019	0.022	0.48	0.56
A3	0.026	0.030	0.65	0.75
D	0.819	0.835	20.80	21.20
D1	0.7480 BSC		19.00 BSC	
E	0.819	0.835	20.80	21.20
E1	0.7480 BSC		19.00 BSC	
b	0.018	0.022	0.45	0.55
e	0.0394 BSC		1.00 BSC	

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
1.0.0	10/26/07	Final release of the 16-Channel LIU Datasheet.
1.0.1	02/04/09	Updated Figure #3 with new CMPOUT filter component values (C3=0.01uf) and adding the Net_Tran_Support @exar.com technical contact info to last page.
1.0.2	03/24/15	Updated part number to include "-F"; Updated Exar logo, changed technical contact to "comtechsupport@exar.com". ECN 1513-07

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