

LTM4630EY-1 High Efficiency, PolyPhase 140A Step-Down Power μ Module™ Regulator

DESCRIPTION

Demonstration Circuit 2164A-C features a PolyPhase® design using the LTM®4630EY-1 (A-grade), the high efficiency, high density, dual 18A, switch mode step-down power module regulator. The input voltage is from 4.5V to 15V. The output voltage is jumper selectable from 0.9V to 1.8V. DC2164A-C can deliver nominal 140A output current. As explained in the data sheet, output current derating is necessary for certain V_{IN} , V_{OUT} , and thermal conditions. The LTM4630-1A on DC2164A-C always operate in continuous conduction mode. The switching frequency can be programmed through a resistor or can be synchronized to an external clock signal. The board allows the user to program how its output voltage ramps up and down through the TRACK pin. The output voltage

is tightly regulated between V_0^+ and V_0^- through remote output voltage sensing which improves output voltage regulation at heavy loads. The LTM4630-1A has $\pm 0.8\%$ total DC errors. These features and the availability of the LTM4630EY-1 in a compact 16mm \times 16mm \times 5.01mm BGA package make it ideal for use in many high-density point-of-load regulation applications. The LTM4630-1 data sheet must be read in conjunction with this demo manual for working on or modifying the demo circuit DC2164A-C.

Design files for this circuit board are available at <http://www.linear.com/demo/DC2164A-C>

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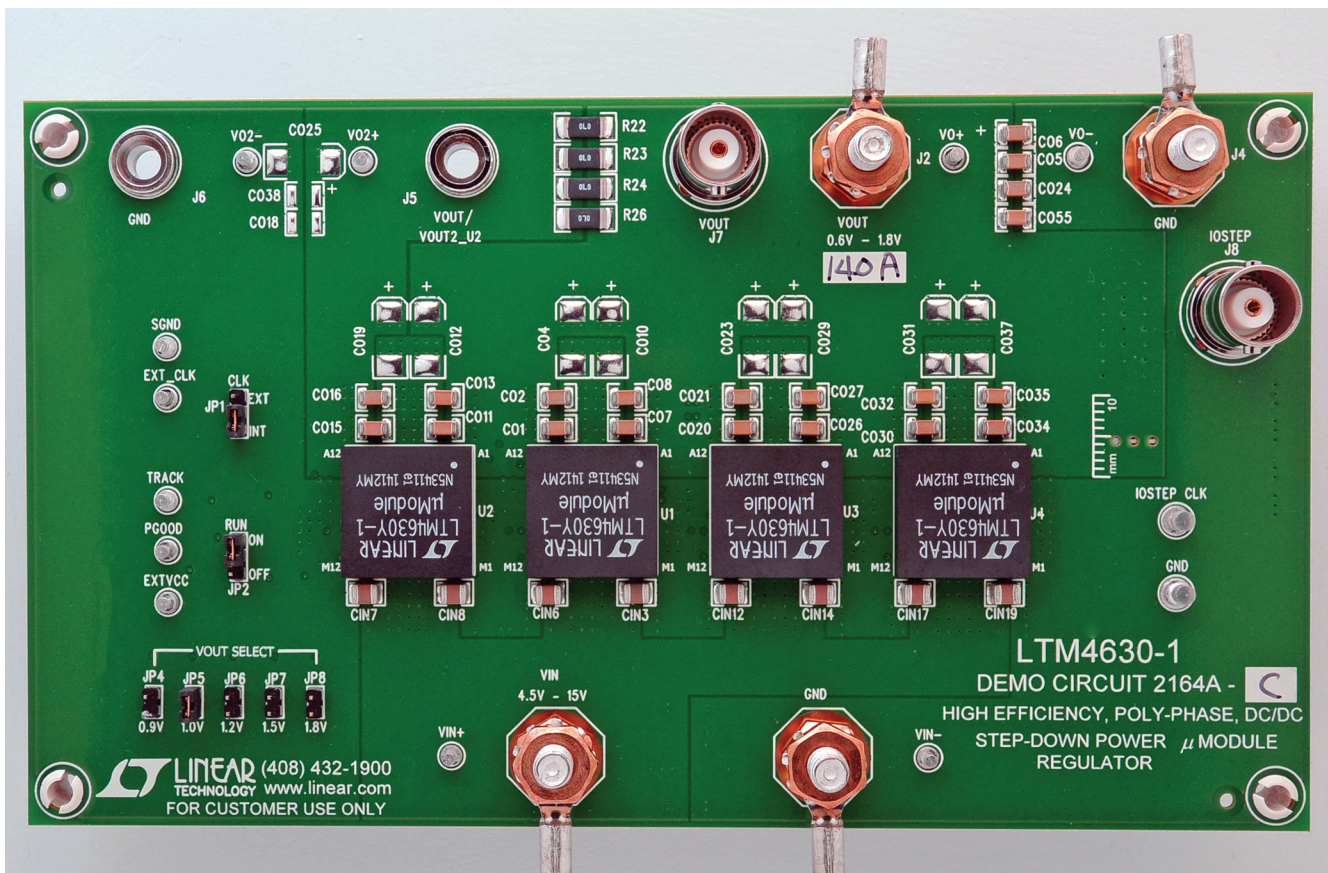


Figure 1. 140A PolyPhase LTM4630-1/DC2164A-C Demo Board

DEMO MANUAL DC2164A-C

PERFORMANCE SUMMARY Specifications are at T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		4.5		15	V
Output Voltage V _{OUT}	V _{IN} = 4.5 ~ 15V, I _{OUT} = 0A ~ 140A, JP5: 1V		1 ±0.8% (0.992 ~ 1.008)		V
Maximum Continuous Output Current	Derating Is Necessary for Certain V _{IN} , V _{OUT} and Thermal Conditions, See Data Sheet for Detail		140		A
Default Operating Frequency			400		kHz
Resistor Programmable Frequency Range		400		780	kHz
External Clock Sync. Frequency Range		400		780	kHz
Efficiency	V _{IN} = 12V, V _{OUT} = 1V, I _{OUT} = 140A, f _{SW} = 400kHz		84.4 (See Figure 3)		%
Load Transient	V _{IN} = 12V, V _{OUT} = 1V, I _{STEP} = 0A ~ 35A		<49.4 (See Figure 4)		mV

QUICK START PROCEDURE

Demonstration circuit 2164A-C is easy to set up to evaluate the performance of PolyPhase operation of the LTM4630EY-1. Due to the high input/output current, user should select the proper input supply/load/cable which can sustain the full load operation. It's recommended to pull load current from J2 and J4. The load current pulled from J5 and J6 shouldn't exceed 18A. Please refer to Figure 2 for proper measurement setup and follow the procedure below:

- Place jumpers in the following positions for a typical 1V_{OUT} application:

JP1	JP2	JP4 ~ JP8
CLK	RUN	VOUT SELECT
INT	OFF	ON JP5/1.0V

- With power off, connect the input power supply, load and meters as shown in Figure 2. Preset the load to 0A and V_{IN} supply to 12V.
- Turn on the power supply at the input. Place JP2 to ON position. The output voltage between V_O⁺ and V_O⁻ should be 1V ±0.8% (0.992V ~ 1.008V).
- Once the proper output voltage is established, adjust the load within the operating range and observe the output voltage regulation, output voltage ripple, efficiency

and other parameters. Output voltage ripple should be measured at J7 with BNC cables. 50Ω termination should be set on the oscilloscope or BNC cables.

- (Optional) For optional load transient test, apply an adjustable pulse signal between IOSTEP CLK and GND test point. Pulse amplitude (3V ~ 3.5V) sets the load step current amplitude. The output transient current can be monitored at the BNC connector J8 (5mV/A). The pulse signal should be very small duty cycle (<10%) to limit the thermal stress on the transient load circuit.
- (Optional) LTM4630-1 can be synchronized to an external clock signal. Place the JP1 jumper on EXT and apply a clock signal (0V ~ 5V, square wave) on the EXT_CLK test point.
- (Optional) The outputs of LTM4630-1 can track another supply. The output voltage tracks the voltage on TRACK when a valid signal is applied on the test point.
- (Optional) DC2164A-C can be configured to a dual outputs configuration with V_O at 122A load current and V_{O2} at 18A load current. Stuff 0Ω resistor on R61 and 0.1μF on C14. Remove R22, R23, R24, R26, R27, R28, R32, R33, R35. Output voltage V_{O2} is set by R37 based on the equation V_{O2} = 0.6V (1 + 60.4k/R37).

QUICK START PROCEDURE

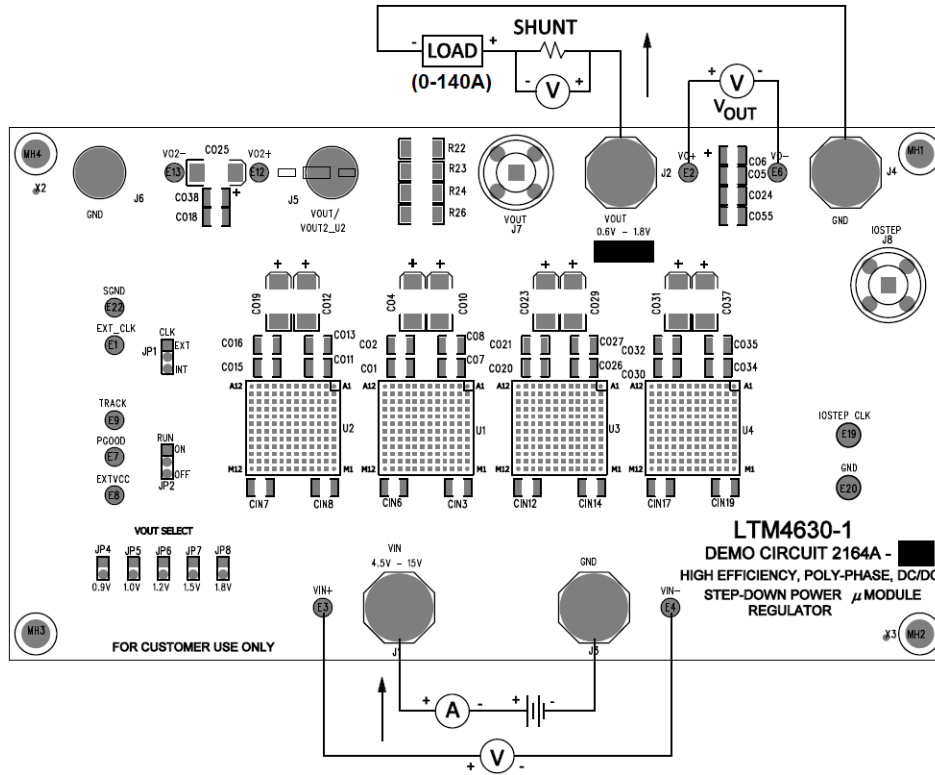


Figure 2. Test Setup of DC2164A-C

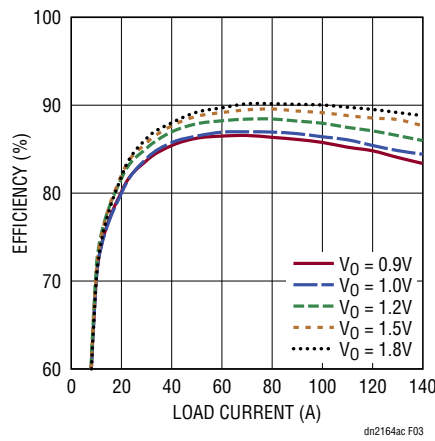


Figure 3. Measured Efficiency $V_{IN} = 12V$, $f_{SW} = 400kHz$

QUICK START PROCEDURE

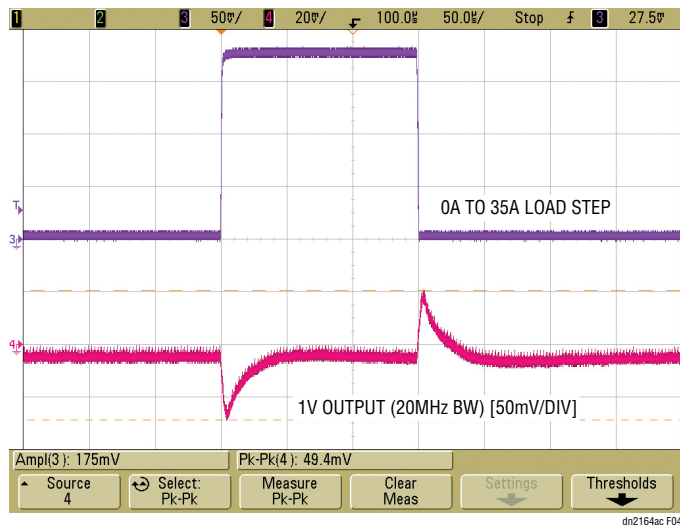


Figure 4. Load Transient 0A to 35A ($V_{IN} = 12V$, $V_{OUT} = 1V$)

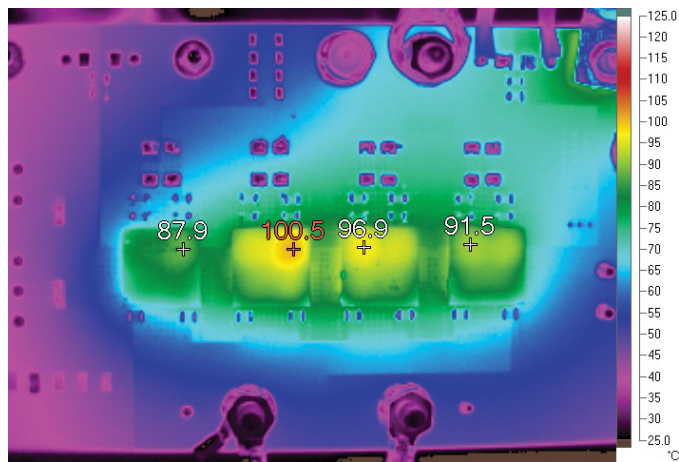


Figure 5. Thermal Capture at 12V_{IN}, 1V_{OUT}, 140A ($T_A = 25^\circ C$, 400 LFM Airflow and No Heat Sink)

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	CIN1	CAP, 150 μ F 25% 25V ALUM	SUN ELECT., 25CE150AX
2	2	CIN2, CIN11	CAP, 1206 1 μ F 10% 25V X5R	TAIYO YUDEN, TMK316BJ105KL-T
3	16	CIN3-CIN10, CIN12-CIN19	CAP, 1210 22 μ F 10% 25V X5R	AVX, 12103D226KAT2A
4	24	C01, C02, C05, C06, C07, C08, C011, C013, C015, C016, C056, C057, C020, C021, C026, C027, C024, C058, C030, C032, C034, C035, C055, C059	CAP, 1206 220 μ F 20% 4V X5R	MURATA, GRM31CR60G227ME11L
5	1	C1	CAP, 0603 330pF 10% 50V NPO	AVX, 06035A331KAT2A
6	4	C4, C10, C18, C22	CAP, 0603 2.2 μ F 20% 10V X5R	TAIYO YUDEN, LMK107BJ225MA-T
7	6	C6, C11, C19, C23, C27, C28	CAP, 0603 1 μ F 10% 10V X7R	TAIYO YUDEN, LMK107BJ105KA-T
8	2	C7, C25	CAP, 0603 0.1 μ F 10% 25V X7R	AVX, 06033C104KAT2A
9	2	C24, C31	CAP, 0603 0.01 μ F 10% 100V X7R	AVX, 06031C103KAT2A
10	2	Q1, Q2	MOSFET, N-CH D-S 30V TO252	VISHAY, SUD50N04-8M8P-4GE3
11	4	R1, R3, R25, R29	RES, 0603 10 Ω 5% 1/10W	VISHAY, CRCW060310R0JNEA
12	5	R2, R14, R21, R39, R47	RES, 0603 121k 1% 1/10W	VISHAY, CRCW0603121KFKEA
13	4	R4, R36, R41, R54	RES, 0603 10k 5% 1/10W	VISHAY, CRCW060310K0JNEA
14	4	R9, R31, R43, R51	RES, 0603 100k 1% 1/10W	VISHAY, CRCW0603100KFKEA
15	1	R11	RES, 0603 2.32k 1% 1/10W	VISHAY, CRCW06032K32FKEA
16	1	R15	RES, 0603 90.9k 1% 1/10W	VISHAY, CRCW060390K9FKEA
17	1	R16	RES, 0603 60.4k 1% 1/10W	VISHAY, CRCW060360K4FKEA
18	1	R17	RES, 0603 40.2k 1% 1/10W	VISHAY, CRCW060340K2FKEA
19	1	R18	RES, 0603 30.1k 1% 1/10W	VISHAY, CRCW060330K1FKEA
20	2	R56, R57	RES, 2512 0.010 Ω 1% 1W	VISHAY, WSL2512R01000FEA
21	4	U1, U2, U3, U4	IC, VOLTAGE REGULATOR, BGA	LINEAR TECH., LTM4630IY-1A#PBF

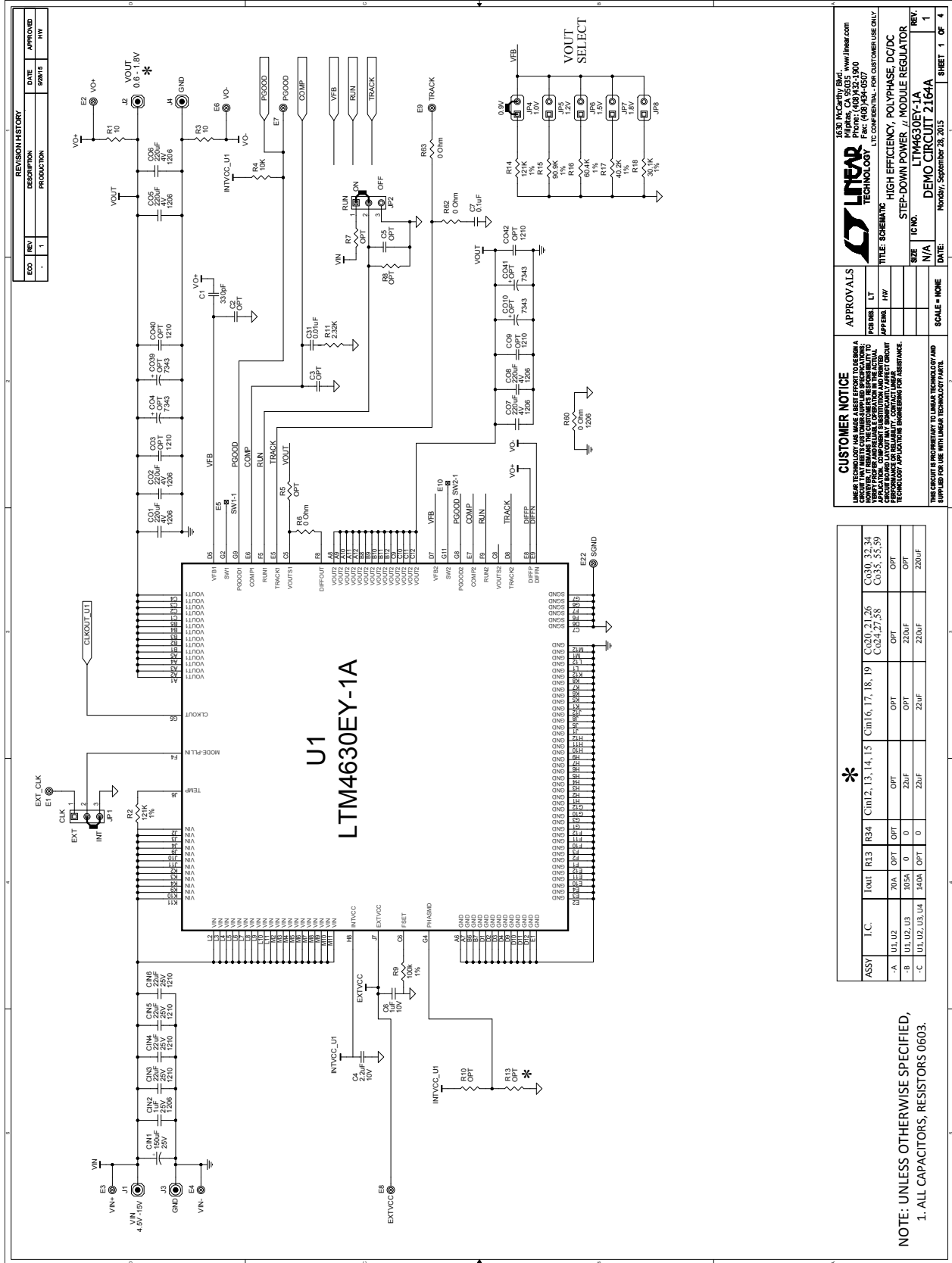
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PARTS LIST

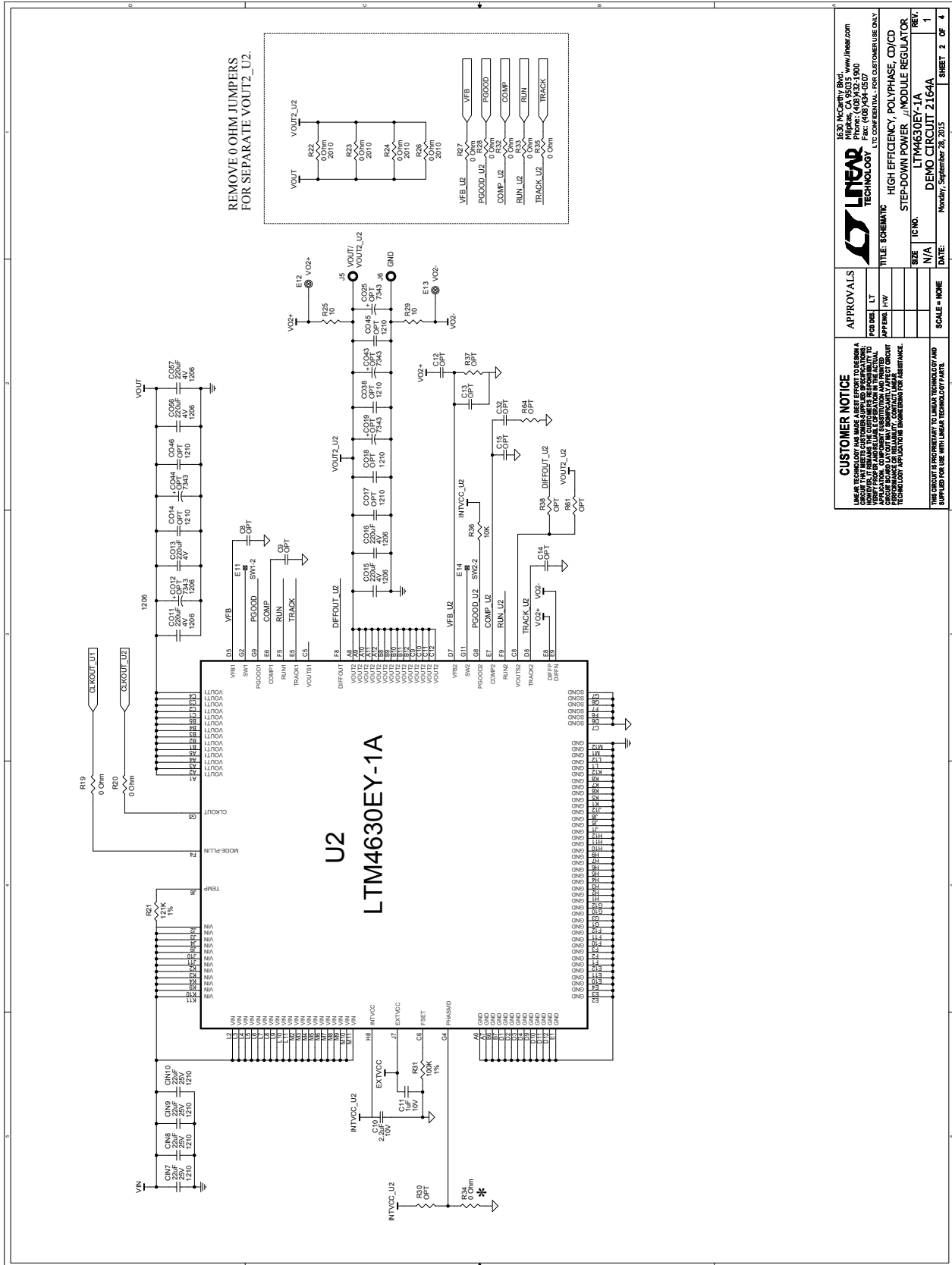
ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Additional Demo Board Circuit Components				
1	0	C03, C09, C014, C017, C018, C022, C028, C033, C036, C038, C040, C042, C045, C046, C048, C050, C052, C054	CAP, 1210 OPTION	OPTION
2	0	C04, C010, C012, C019, C023, C025, C029, C031, C037, C039, C041, C043, C044, C047, C049, C051, C053	CAP, 7343 OPTION	OPTION
3	0	C2, C3, C5, C8, C9, C12-, C17, C20, C21, C26, C29, C30, C32	CAP, 0603 OPTION	OPTION
4	0	R5, R7, R8, R10, R30, R37, R38, R42, R44, R48-R50, R52, R53, R55, R61, R64	RES, 0603 OPTION	OPTION
5	13	R6, R19, R20, R27, R28, R32, R33-R35, R40, R45, R62, R63	RES, 0603 0Ω JUMPER	VISHAY, CRCW06030000Z0EA
6	0	R13	RES, 0603 OPTION	OPTION
7	4	R22, R23, R24, R26	RES, 2010 0Ω JUMPER	VISHAY, CRCW20100000ZEA9
8	0	R58, R59	RES, 2512 OPTION	OPTION
9	1	R60	RES, 1206 0Ω JUMPER	VISHAY, CRCW12060000Z0EA
Hardware: For Demo Board Only				
1	11	E1-E4, E6-E9, E12, E13, E22	TESTPOINT, TURRET, 0.063"	MILL MAX, 2308-2-00-80-00-00-07-0
2	2	E19, E20	TESTPOINT, TURRET, 0.094"	MILL MAX, 2501-2-00-80-00-00-07-0
3	2	JP1, JP2	HEADER, 3 PIN 0.079 SINGLE ROW	SULLINS, NRPN031PAEN-RC
4	5	JP4, JP5, JP6, JP7, JP8	HEADER, 2 PIN 0.079 SINGLE ROW	SAMTEC, TMM-102-02-L-S
5	4	J1, J2, J3, J4	STUD, TEST PIN	PEM, KFH-032-10
6	8	J1, J2, J3, J4 (x2)	NUT, BRASS PL #10-32	ANY, 10-32M/S BR PL
7	4	J1, J2, J3, J4	LUG RING, #10	KEystone, 8205
8	4	J1, J2, J3, J4	WASHER, TIN PLATED BRASS	ANY, #10EXT BZ TN
9	2	J5, J6	JACK, BANANA	KEystone, 575-4
10	2	J7, J8	CON, BNC, 5 PINS	CONNEX, 112404
11	3	XJP1, XJP2, XJP4	SHUNT	SAMTEC, 2SN-BK-G

DEMO MANUAL DC2164A-C

SCHEMATIC DIAGRAM

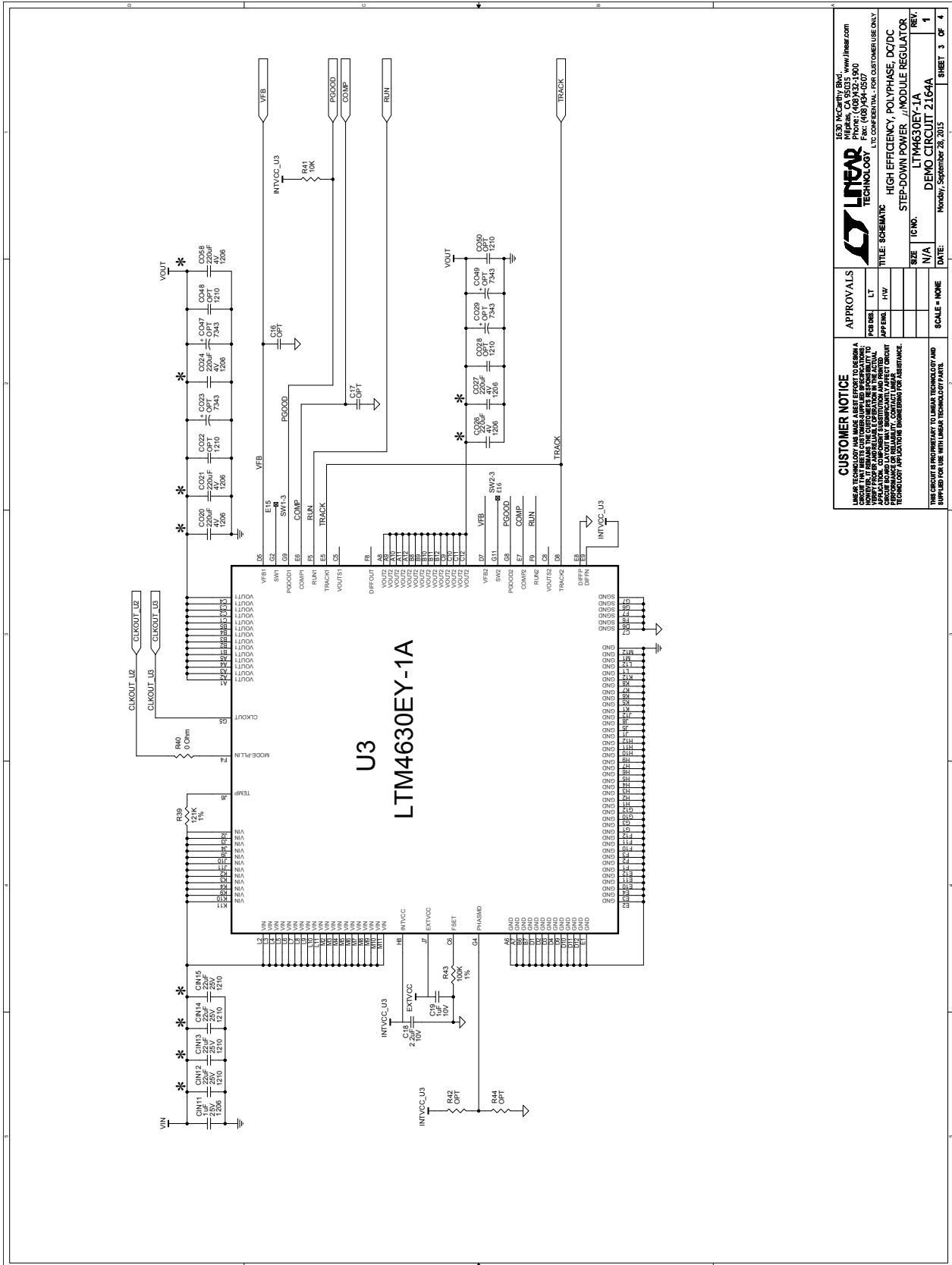


SCHEMATIC DIAGRAM



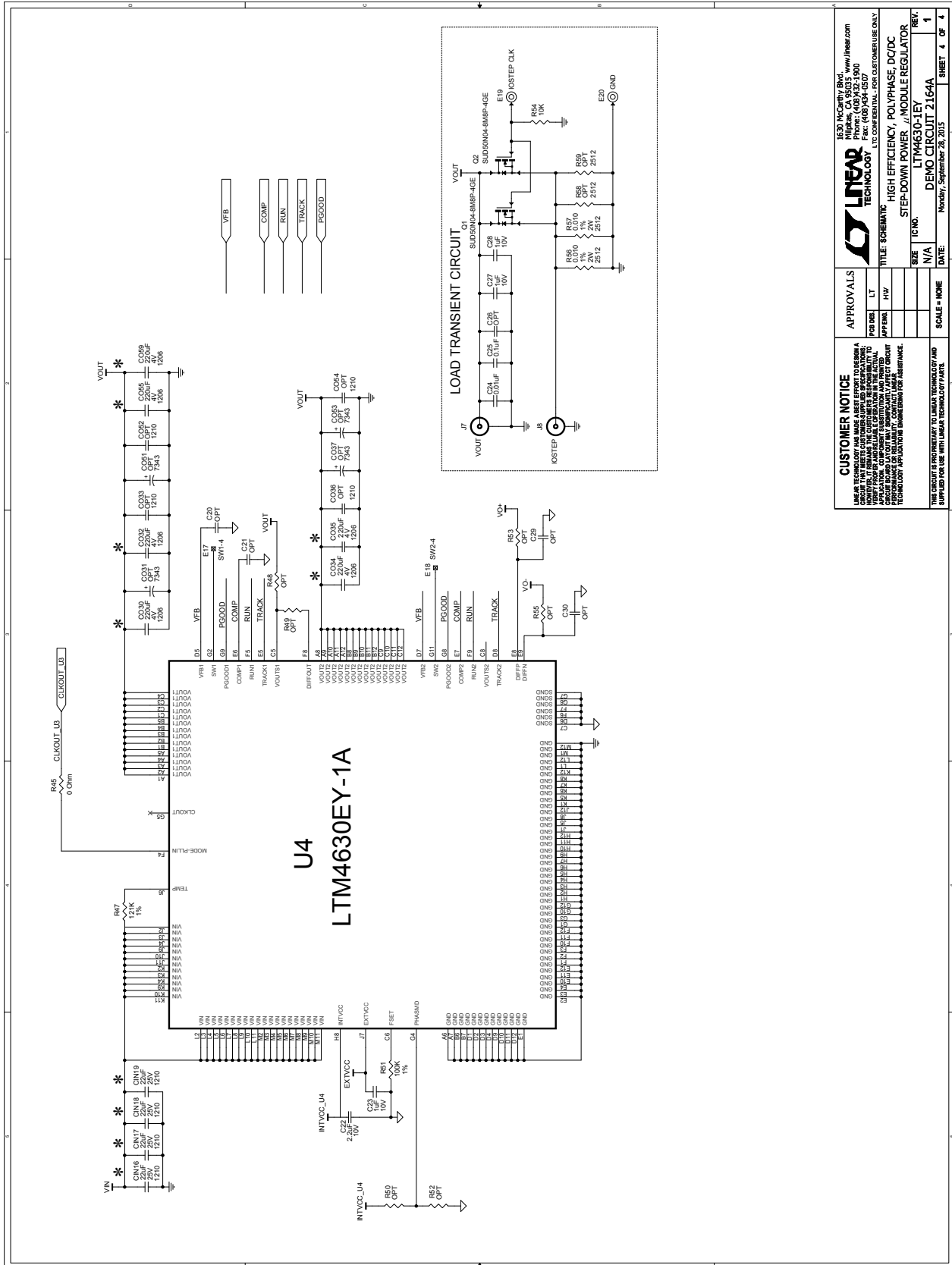
DEMO MANUAL DC2164A-C

SCHEMATIC DIAGRAM



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SCHEMATIC DIAGRAM



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TITLE: SCHEMATIC, HIGH EFFICIENCY, POLYPHASE, DC/DC STEP-DOWN POWER, //MIDDLE REGULATOR

U4: LTM4630-EY

DEMO CIRCUIT 2164A

DATE: Monday, September 28, 2015

SCALE: NONE

APPROVALS

DESIGNER	LT
APP'D	HV
DATE	
SCALE	NONE
SHEET	4
OF	4



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DEMO MANUAL DC2164A-C

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