

1.8V Operating Voltage Fundamental Quartz Crystal Oscillator IC with Input Tolerant Function

GENERAL DESCRIPTION

The NJU6221 series is a C-MOS quartz crystal oscillator IC realized excellent frequency stability for fundamental (up to 60MHz) oscillation, and consists of an oscillation amplifier, a 6-stage divider, a 3-state output buffer, a built-in LDO and a input tolerant circuit. The operating voltage is from 1.62V to 3.63V, and the LDO holds down the characteristic change of the oscillation amplifier for operating voltage variation, and has been stabilized oscillation frequency. ($\pm 1\text{ppm}@V_{DD}\pm 10\%$)

The 6-stage divider generates only one frequency selected at the factory shipment of f_0 , $f_0/2$, $f_0/4$, $f_0/8$, $f_0/16$, $f_0/32$ and $f_0/64$ internal circuits is output. The 3-state output buffer is C-MOS compatible.

The input tolerant circuit ensures that 0 to 3.63 V can be applied to CONT terminal without regard to the supply voltage. The oscillation stopping current is very low stand-by mode, therefore, it is suitable for the portable items of the communication equipment and the like.

PACKAGE OUTLINE

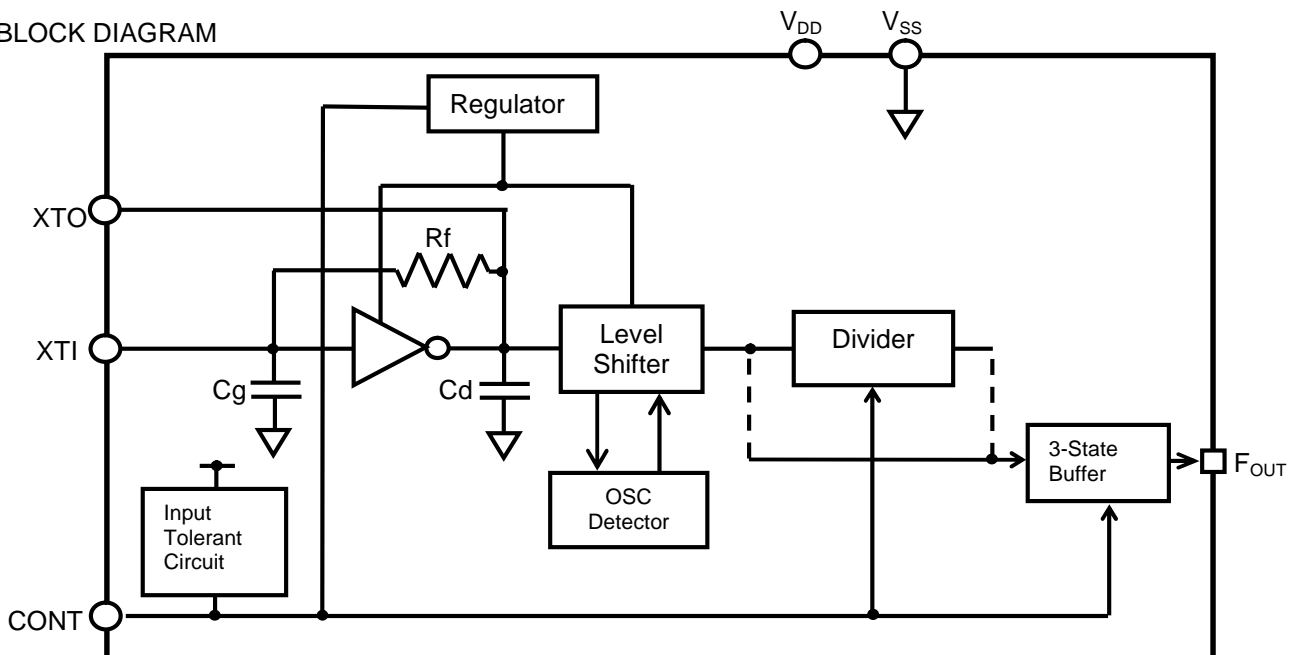


NJU6221XxC-V

FEATURES

Maximum Oscillation Frequency	60MHz(Fundamental)
Frequency Stability	$\pm 1\text{ppm}@V_{DD}\pm 10\%$
Wide Operating Voltage	1.62 to 3.63V
Low Operating Current	2mA typ. @60MHz/3.3V
6-Stage Divider	Maximum Divider $f_0/64$
Built-in LDO	
Input Tolerant Circuit	0 to 3.63V@CONT Term.
Oscillation Stop and Output Stand-by Function	
3-State Output Buffer	
Variable Pull-up Resistance on-Die (CONT: Pull-up Resistance large at the Stand-by mode.)	
Oscillation Capacitors C_g and C_g on-Die	
C-MOS Technology	
Package Outline	Die/Wafer

BLOCK DIAGRAM

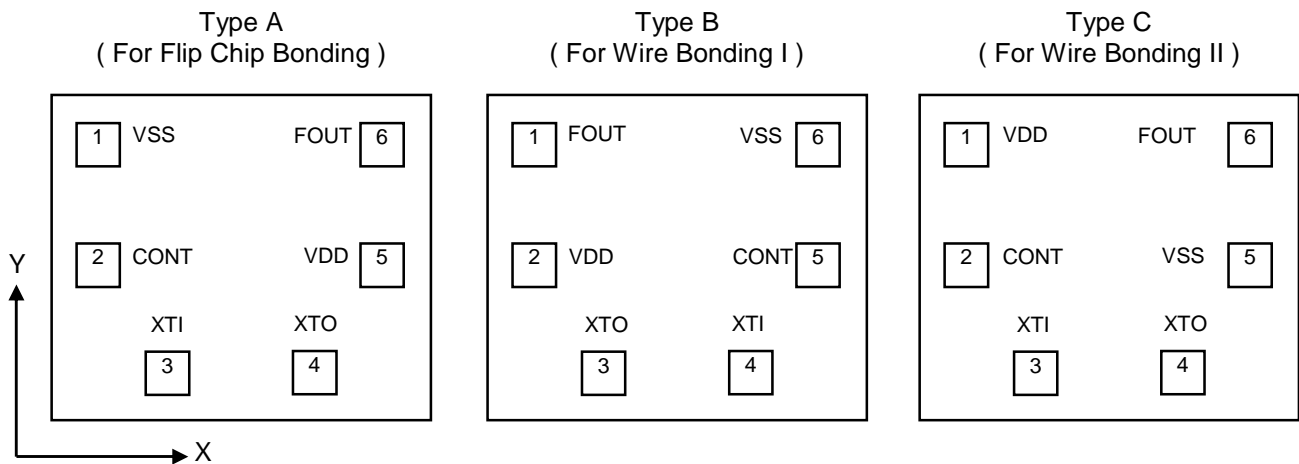


LINE-UP TABLE

Type No.	F _{OUT}	Version		
		Type A	Type B	Type C
NJU6221	f ₀	A1	B1	C1
	f ₀ /2	A2*	B2*	C2*
	f ₀ /4	A3*	B3*	C3*
	f ₀ /8	A4*	B4*	C4*
	f ₀ /16	A5*	B5*	C5*
	f ₀ /32	A6*	B6*	C6*
	f ₀ /64	A7*	B7*	C7*

* Under development

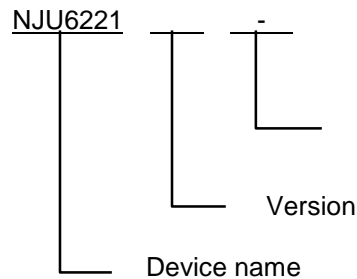
PAD LOCATION



COORDINATES

Pad No.	X	Y
1	-261.5	198.5
2	-261.5	-21.5
3	-146.5	-211.5
4	144.5	-211.5
5	260.5	-21.5
6	260.5	198.5

PART NUMBER



W-H: Wafer (200μm)
 W-B: Wafer (160μm)
 WS4-V: 1/4Wafer(130μm)
 C-V: Chip(130μm)

Starting Point: Die Center Unit[μm]
 Die Size: 0.73x0.63mm
 Die Thickness (C-V): 130±15μm
 Wafer Thickness(WS4-V): 130±15μm
 Wafer Thickness (W-B): 160±20μm
 Wafer Thickness (W-H): 200±20μm
 Pad size: 80x80μm
 Die Substrate: V_{SS} level

($V_{DD}=1.62$ to $3.63V$, $V_{SS}=0V$, $T_a=+25^{\circ}C$)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	
Operating Current	I_{DD}	x1 version (f_0) No load CONT=Open $f_0=60MHz$ $F_{out}=60MHz$	$V_{DD}=1.8V$		1.250	1.875	mA
			$V_{DD}=2.5V$		1.625	2.500	
			$V_{DD}=3.3V$		2.000	3.000	
		x2 version ($f_0/2$) *	$V_{DD}=1.8V$		1.125	1.750	
			$V_{DD}=2.5V$		1.500	2.250	
			$V_{DD}=3.3V$		1.875	2.875	
		x3 version ($f_0/4$) *	$V_{DD}=1.8V$		1.000	1.500	
			$V_{DD}=2.5V$		1.25	1.875	
			$V_{DD}=3.3V$		1.625	2.500	
		x4 version ($f_0/8$) *	$V_{DD}=1.8V$		0.940	1.440	
			$V_{DD}=2.5V$		1.125	1.750	
			$V_{DD}=3.3V$		1.375	2.125	
		x5 version ($f_0/16$) *	$V_{DD}=1.8V$		0.875	1.375	
			$V_{DD}=2.5V$		1.060	1.625	
			$V_{DD}=3.3V$		1.310	2.000	
		x6 version ($f_0/32$) *	$V_{DD}=1.8V$		0.875	1.375	
			$V_{DD}=2.5V$		1.060	1.625	
			$V_{DD}=3.3V$		1.250	1.875	
		x7 version ($f_0/64$) *	$V_{DD}=1.8V$		0.875	1.375	
			$V_{DD}=2.5V$		1.060	1.625	
			$V_{DD}=3.3V$		1.250	1.875	
Oscillation Stopping Current	I_{STB}	CONT= V_{SS} , No load			10	μA	
Output Voltage	V_{OH}	$I_{OH}=4mA$	$V_{DD}-0.4$			V	
	V_{OL}	$I_{OL}=4mA$			0.4	V	
Input Voltage	V_{IH}	CONT Input Tolerant Function	$0.7V_{DD}$			V	
	V_{IL}	CONT			$0.3V_{DD}$	V	
Input Current Note4)	I_{IN}	CONT= $3.63V$			1	μA	
		CONT= $0.8V_{DD}$			8	μA	
		CONT= $0.2V_{DD}$			5	μA	
3-state Off Leakage Current	I_{OZ}	CONT= V_{SS} , $F_{OUT}=V_{DD}$ or V_{SS}			± 0.1	μA	

* Under development and tentative value.

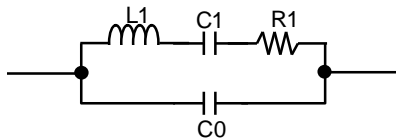
Note1) Absolute value.

($V_{DD}=1.62$ to $3.63V$, $V_{SS}=0V$, $T_a=+25^{\circ}C$)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	
Feedback Resistance	Rf			545		k Ω	
Internal Capacitor	Cg	fosc=60MHz		7.5		pF	
	Cd	fosc=60MHz		8.5		pF	
Oscillation Frequency	fosc	Recommendation Note1)			60	MHz	
Output Signal Symmetry	SYM	$C_L=15pF$, @ $V_{DD}/2$	45	50	55	%	
Output Signal Rise Time	tr	$C_L=15pF$ $0.1V_{DD}$ to $0.9V_{DD}$	$V_{DD}=1.8V$		3.2	5.0	ns
			$V_{DD}=2.5V$		2.2	3.7	ns
			$V_{DD}=3.3V$		1.8	3.0	ns
Output Signal Fall Time	tf	$C_L=15pF$ $0.9V_{DD}$ to $0.1V_{DD}$	$V_{DD}=1.8V$		3.2	5.0	ns
			$V_{DD}=2.5V$		2.2	3.7	ns
			$V_{DD}=3.3V$		1.8	3.0	ns
Output Disable time	t _{POZ}	$C_L=15pF$, $R_L=1k\Omega$			100	ns	
Output Enable Time	t _{PZO}	$C_L=15pF$			1	ms	

Note1) The oscillation frequency range has used NJRC's standard crystal for measurement. However it is not guaranteed. (Refer to EXAMPLE OF CRYSTAL PARAMETERS FOR MEASUREMENT CIRCUITS)

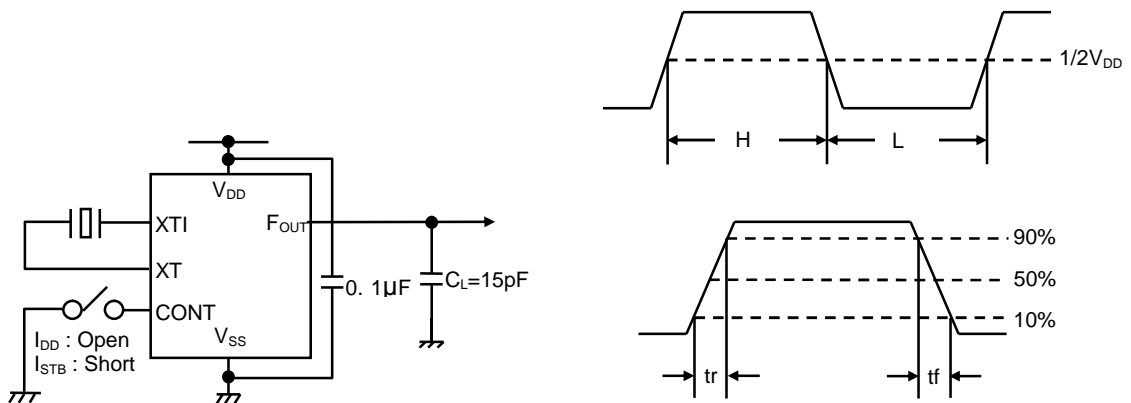
EXAMPLE OF CRYSTAL PARAMETERS FOR MEASUREMENT CIRCUITS



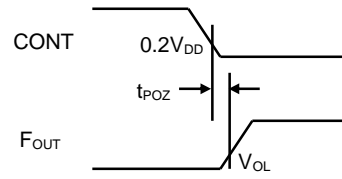
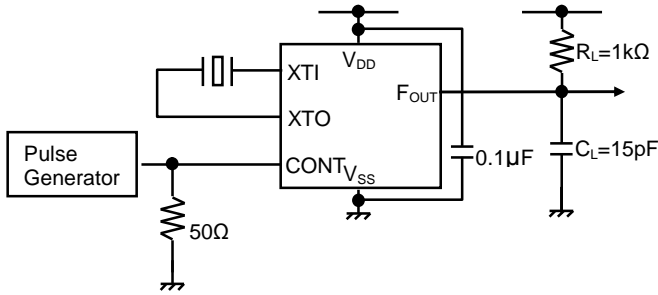
f[MHz]	R1[Ω]	L1[mH]	C1[fF]	C0[pF]
60	31.18	3.75	1.87	0.92

MEASUREMENT CIRCUITS

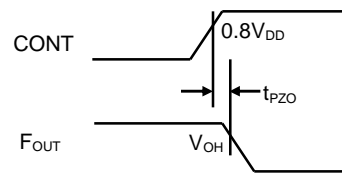
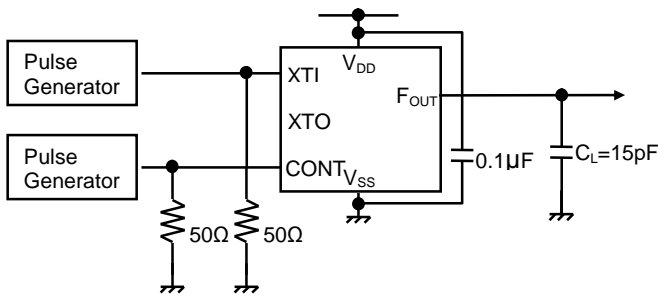
(1) Operating Current ($C_L=0pF$), Output Signal Symmetry ($C_L=15pF$), Output Signal Rise/Fall Time ($C_L=15pF$)



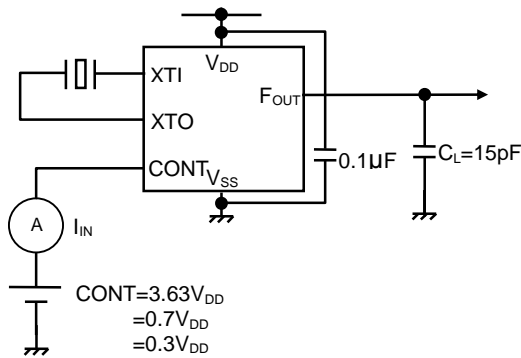
(2) Output Disable Time ($C_L=15\text{pF}, R_L=1\text{k}\Omega$)



(3) Output Enable Time ($C_L=15\text{pF}$)



(4) Input Current ($C_L=15\text{pF}$)



[CAUTION]
 The specifications on this data book are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this data book are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.