NBSG86A

2.5V/3.3V SiGe Differential Smart Gate with Output Level Select

The NBSG86A is a multi−function differential Logic Gate which can be configured as an AND/NAND, OR/NOR, XOR/XNOR, or 2:1 MUX. This device is part of the GigaComm™ family of high performance Silicon Germanium products. The device is housed in a low profile 4x4 mm, 16−pin, flip−chip BGA or a 3x3 mm 16 pin QFN package.

Differential inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), LVCMOS/LVTTL, CML, or LVDS. The OLS input is used to program the peak−to−peak output amplitude between 0 and 800 mV in five discrete steps.

The NBSG86A employs input default circuitry so that under open input conditions (D_x, $\overline{D_x}$, $\overline{VTD_x}$, VTD_x, VTSEL) the outputs of the device will remain stable.

- Maximum Input Clock Frequency > 8 GHz Typical
- Maximum Input Data Rate > 8 Gb/s Typical
- 165 ps Typical Propagation Delay
- 40 ps Typical Rise and Fall Times
- Selectable Swing PECL Output with Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- Selectable Swing NECL Output with NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = −2.375 V to −3.465 V
- Selectable Output Level (0 V, 200 mV, 400 mV, 600 mV, or 800 mV Peak−to−Peak Output)
- 50 Ω Internal Input Termination Resistors

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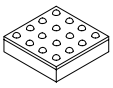
MARKING DIAGRAM*



FCBGA−16
BA SUFFIX
CASE 489

QFN−16
MN SUFFIX
CASE 485G

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For further details, refer to Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping†
NBSG86ABA	4x4 mm FCBGA−16	100 Units/Tray
NBSG86ABAR2	4x4 mm FCBGA−16	500/ Tape & Reel
NBSG86AMN	3x3 mm QFN−16	123 Units/Rail
NBSG86AMNR2	3x3 mm QFN−16	3000/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Board	Description
NBSG86ABAEVB	NBSG86ABA Evaluation Board

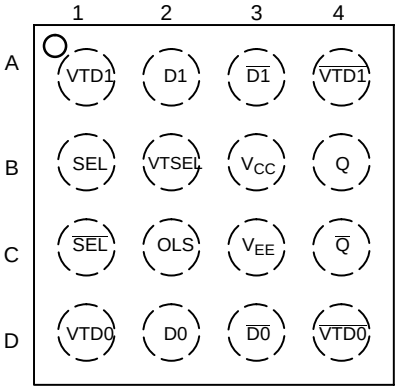


Figure 1. BGA−16 Pinout (Top View)

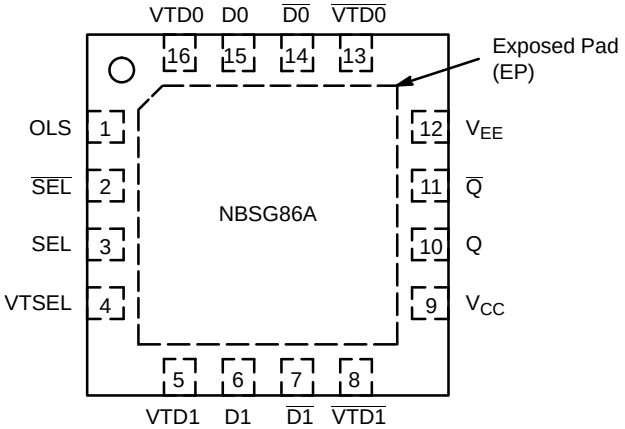


Figure 2. QFN−16 Pinout (Top View)

Table 1. Pin Description

Pin				
BGA	**QFN**	**Name**	**I/O**	**Description**
C2	1	OLS (Note 3)	Input	Input Pin for the Output Level Select (OLS). See Table 2.
C1	2	$\overline{SEL}$	ECL, CML, LVCMOS, LVDS, LVTTL Input	Inverted Differential Select Logic Input.
B1	3	SEL	ECL, CML, LVCMOS, LVDS, LVTTL Input	Noninverted Differential Select Logic Input.
B2	4	VTSEL	−	Common Internal 50 Ω Termination Pin for SEL/$\overline{SEL}$. See Table 7. (Note 1)
A1	5	VTD1	−	Internal 50 Ω termination pin. See Table 7. (Note 1)
A2	6	D1	ECL, CML, LVCMOS, LVDS, LVTTL Input	Noninverted Differential Input 1. Internal 75 kΩ to V_{EE}.
A3	7	$\overline{D1}$	ECL, CML, LVCMOS, LVDS, LVTTL Input	Inverted Differential Input 1. Internal 75 kΩ to V_{EE} and 36.5 kΩ to V_{CC}.
A4	8	$\overline{VTD1}$	−	Internal 50 Ω Termination Pin. See Table 7. (Note 1)
B3	9	V_{CC}	−	Positive Supply Voltage (Note 2)
B4	10	Q	RSECL Output	Noninverted Differential Output. Typically Terminated with 50 Ω Resistor to $V_{TT} = V_{CC} - 2$ V.
C4	11	$\overline{Q}$	RSECL Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to $V_{TT} = V_{CC} - 2$ V
C3	12	V_{EE}	−	Negative Supply Voltage (Note 2)
D4	13	$\overline{VTD0}$	−	Internal 50 Ω Termination Pin. See Table 7. (Note 1)
D3	14	$\overline{D0}$	ECL, CML, LVCMOS, LVDS, LVTTL Input	Inverted Differential Input 0. Internal 75 kΩ to V_{EE} and 36.5 kΩ to V_{CC}.
D2	15	D0	ECL, CML, LVCMOS, LVDS, LVTTL Input	Noninverted Differential Input 0. Internal 75 kΩ to V_{EE}.
D1	16	VTD0	−	Internal 50 Ω Termination Pin. See Table 7. (Note 1)
N/A	−	EP	−	Exposed Pad. The thermally exposed pad on package bottom (see case drawing) must be attached to a heat−sinking conduit.

1. In the differential configuration when the input termination pins (VTDx, $\overline{VTDx}$, VTSEL) are connected to a common termination voltage, and if no signal is applied then the device will be susceptible to self−oscillation.
2. All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.
3. When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0$ V, 2 kΩ resistor should be connected from OLS pin to V_{EE}.

Table 2. OUTPUT LEVEL SELECT OLS

OLS	Q/Q VPP	OLS Sensitivity
V_{CC}	800 mV	OLS − 75 mV
V_{CC} − 0.4 V	200 mV	OLS ± 150 mV
V_{CC} − 0.8 V	600 mV	OLS ± 100 mV
V_{CC} − 1.2 V	0	OLS ± 75 mV
V_{EE} (Note 4)	400 mV	OLS ± 100 mV
Float	600 mV	N/A

4. When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0$ V, 2.0 kΩ resistor should be connected from OLS to V_{EE}.

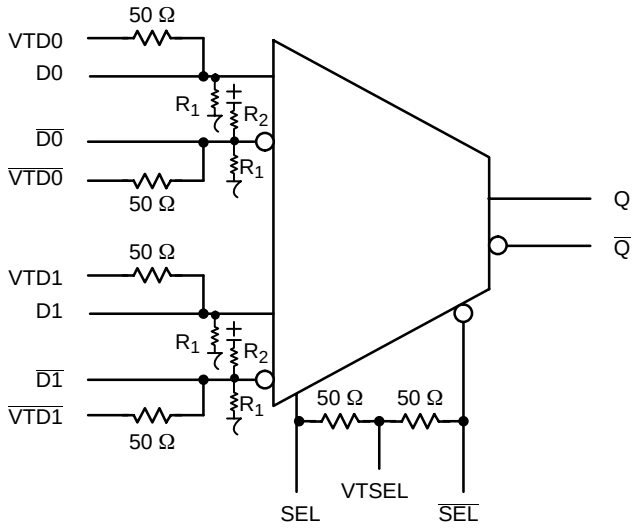


Figure 3. Logic Diagram

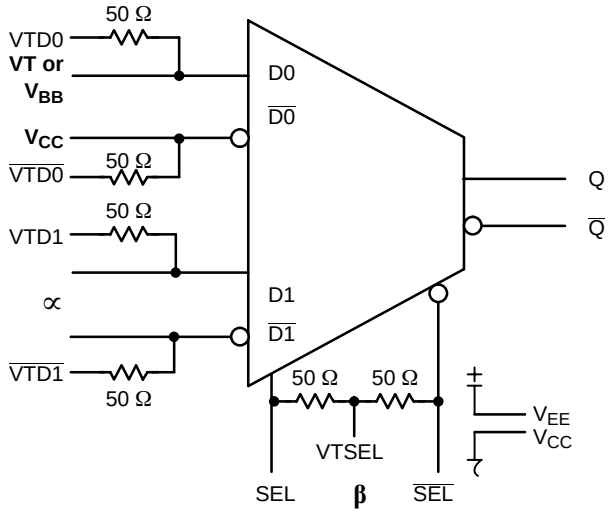


Figure 4. Configuration for AND/NAND Function

Table 3. AND/NAND TRUTH TABLE (Note 5)

	∝	β	∝ * β
D0	**D1**	**SEL**	**Q**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1

5. $\overline{D0}$, $\overline{D1}$, $\overline{SEL}$ are inverse of D0, D1, SEL unless specified otherwise.

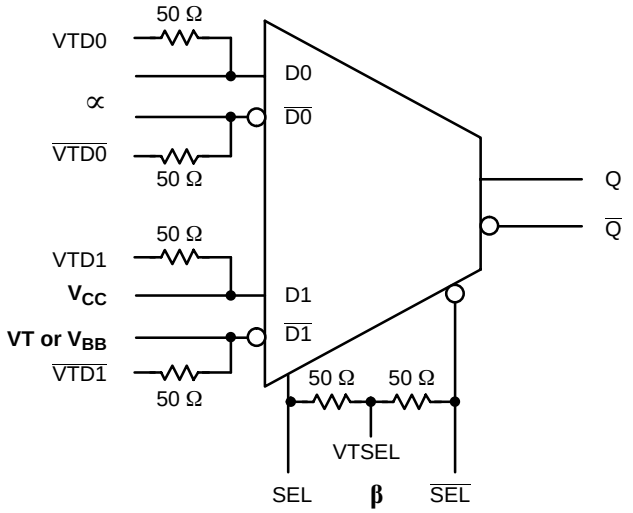


Figure 5. Configuration for OR/NOR Function

Table 4. OR/NOR TRUTH TABLE**

∝		β	∝ or β
D0	**D1**	**SEL**	**Q**
0	1	0	0
0	1	1	1
1	1	0	1
1	1	1	1

** $\overline{D0}$, $\overline{D1}$, $\overline{SEL}$ are inverse of D0, D1, SEL unless specified otherwise.

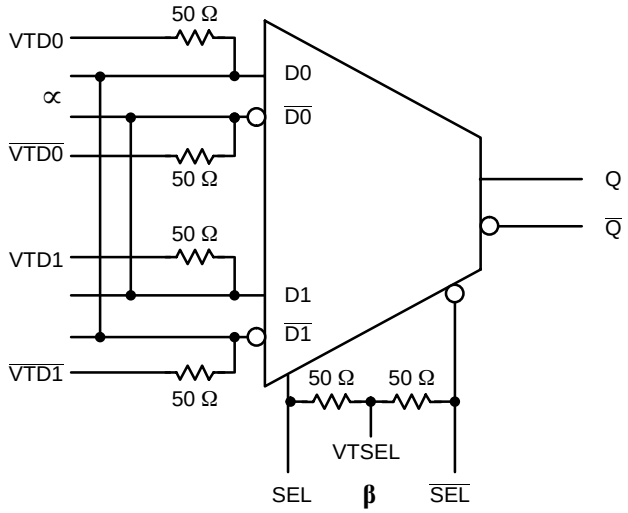


Figure 6. Configuration for XOR/XNOR Function

Table 5. XOR/XNOR TRUTH TABLE**

∝		β	∝ XOR β
D0	**D1**	**SEL**	**Q**
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0

** $\overline{D0}$, $\overline{D1}$, $\overline{SEL}$ are inverse of D0, D1, SEL unless specified otherwise.

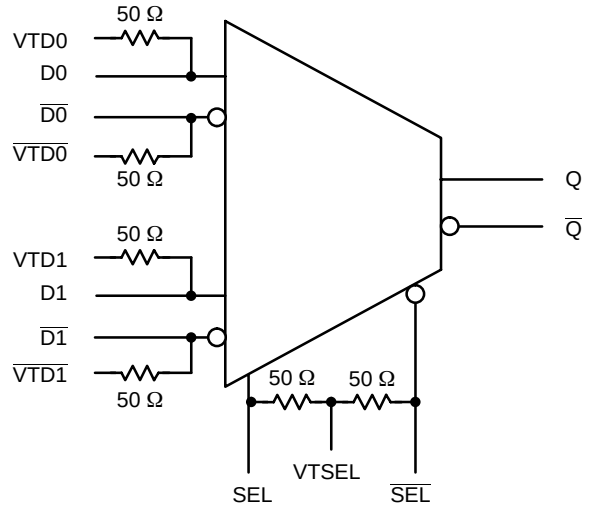


Figure 7. Configuration for 2:1 MUX Function

Table 6. 2:1 MUX TRUTH TABLE**

SEL	Q
1	D1
0	D0

** $\overline{D0}$, $\overline{D1}$, $\overline{SEL}$ are inverse of D0, D1, SEL unless specified otherwise.

Table 7. Interfacing Options

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTD0, VTD1, VTSEL and $\overline{VTD0}$, $\overline{VTD1}$ to V_{CC}
LVDS	Connect VTD0, VTD1, $\overline{VTD0}$ and $\overline{VTD1}$ together. Leave VTSEL open.
AC−COUPLED	Bias VTD0, VTD1, VTSEL and $\overline{VTD0}$, $\overline{VTD1}$ Inputs within (VIHCMR) Common Mode Range
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTL, LVCMOS	An external voltage should be applied to the unused complementary differential input. Nominal voltage 1.5 V for LVTTL and $V_{CC}/2$ for LVCMOS inputs.

Table 8. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistors	(R_1)	75 kΩ
Internal Input Pullup Resistor	(R_2)	37.5 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 1 KV > 50 V > 4 KV
Moisture Sensitivity (Note 6)	16−FCBGA 16−QFN	Level 3 Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		364
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

6. For additional information, see Application Note AND8003/D.

Table 9. MAXIMUM RATINGS (Note 7)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	V_{EE} = 0 V		3.6	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		−3.6	V
V_I	Positive Input Negative Input	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	3.6 −3.6	V V
V_{INPP}	Differential Input Voltage $\lvert D_n - \overline{D_n}\rvert$	$V_{CC} - V_{EE} \ge$ 2.8 V $V_{CC} - V_{EE} <$ 2.8 V		2.8 $\lvert V_{CC} - V_{EE}\rvert$	V V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA mA
I_{out}	Output Current	Continuous Surge		25 50	mA mA
TA	Operating Temperature Range	16−FCBGA 16−QFN		−40 to +70 −40 to +85	°C °C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 8)	0 LFPM 500 LFPM 0 LFPM 500 LFPM	16 FCBGA 16 FCBGA 16 QFN 16 QFN	108 86 41.6 35.2	°C/W °C/W °C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P (Note 8) 2S2P (Note 9)	16 FCBGA 16 QFN	5.0 4.0	°C/W °C/W
T_{sol}	Wave Solder	< 15 Sec.		225	°C

7. Maximum Ratings are those values beyond which device damage may occur.
8. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).
9. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 10. DC CHARACTERISTICS, INPUT WITH PECL OUTPUT V_{CC} = 2.5 V; V_{EE} = 0 V (Note 10)

Symbol	Characteristic	−40°C			25°C			70°C(BGA)/85°C(QFN)**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current	23	30	39	23	30	39	23	30	39	mA
V_{OH}	Output HIGH Voltage (Note 11)	1460	1510	1560	1490	1540	1590	1515	1565	1615	mV
V_{OL}	Output LOW Voltage (Note 11) (OLS = V_{CC}) (OLS = V_{CC} − 0.4 V) (OLS = V_{CC} − 0.8 V, OLS = FLOAT) (OLS = V_{CC} − 1.2 V) (OLS = V_{EE})	 555 1235 775 1455 1005	 705 1295 895 1505 1095	 855 1355 1015 1555 1185	 595 1270 810 1490 1040	 745 1330 930 1540 1130	 895 1390 1050 1590 1220	 625 1295 840 1510 1065	 775 1355 960 1560 1155	 925 1415 1080 1610 1245	mV
V_{OUTPP}	Output Voltage Amplitude (OLS = V_{CC}) (OLS = V_{CC} − 0.4 V) (OLS = V_{CC} − 0.8 V, OLS = FLOAT) (OLS = V_{CC} − 1.2 V) (OLS = V_{EE})	 715 125 525 0 325	 805 215 615 5 415		 705 120 520 0 320	 795 210 610 0 410		 700 120 515 0 320	 790 210 605 5 410		mV
V_{IH}	Input HIGH Voltage (Single−Ended) (Note 13) D, $\overline{D}$	V_{EE} + 1275	V_{CC} − 1000*	V_{CC}	V_{EE} + 1275	V_{CC} − 1000*	V_{CC}	V_{EE} + 1275	V_{CC}− 1000*	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single−Ended) (Note 14) D, $\overline{D}$	V_{EE}	V_{CC}− 1400*	V_{IH}− 150	V_{EE}	V_{CC}− 1400*	V_{IH}− 150	V_{EE}	V_{CC}− 1400*	V_{IH}− 150	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 12)	1.2		2.5	1.2		2.5	1.2		2.5	V
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@V_{IH}) D, $\overline{D}$ SEL		30 5	100 50		30 5	100 50		30 5	100 50	μA
I_{IL}	Input LOW Current (@V_{IL}) D, $\overline{D}$ SEL		20 5	100 50		20 5	100 50		20 5	100 50	μA

NOTE: GigaComm circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

10. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.125 V to −0.965 V.
11. All loading with 50 Ω to V_{CC} − 2.0 V.
12. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
13. V_{IH} cannot exceed V_{CC}.
14. V_{IL} always ≥ V_{EE}.

*Typicals used for testing purposes.

**The device packaged in FCBGA−16 have maximum ambient temperature specification of 70°C and devices packaged in QFN−16 have maximum ambient temperature specification of 85°C.

Table 11. DC CHARACTERISTICS, INPUT WITH PECL OUTPUT V_{CC} = 3.3 V; V_{EE} = 0 V (Note 15)

		−40°C			25°C			70°C(BGA)/85°C(QFN)***			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Negative Power Supply Current	23	30	39	23	30	39	23	30	39	mA
V_{OH}	Output HIGH Voltage (Note 16)	2260	2310	2360	2290	2340	2390	2315	2365	2415	mV
V_{OL}	Output LOW Voltage (Note 16)										mV
	($OLS = V_{CC}$)	1320	1470	1620	1360	1510	1660	1390	1540	1690	
	($OLS = V_{CC}$ − 0.4 V)	2030	2090	2150	2065	2125	2185	2090	2150	2210	
	($OLS = V_{CC}$ − 0.8 V, OLS = FLOAT)	1550	1670	1790	1585	1705	1825	1615	1735	1855	
	($OLS = V_{CC}$ − 1.2 V)	2260	2310	2360	2290	2340	2390	2315	2365	2415	
	**($OLS = V_{EE}$)	1785	1875	1965	1820	1910	2000	1850	1940	2030	
V_{OUTPP}	Output Voltage Amplitude										mV
	($OLS = V_{CC}$)	750	840		740	830		735	825		
	($OLS = V_{CC}$ − 0.4 V)	130	220		125	215		125	215		
	($OLS = V_{CC}$ − 0.8 V, OLS = FLOAT)	550	640		545	635		540	630		
	($OLS = V_{CC}$ − 1.2 V)	0	0		0	0		0	0		
	**($OLS = V_{EE}$)	345	435		340	430		335	425		
V_{IH}	Input HIGH Voltage (Single−Ended) (Note 18) D, $\overline{D}$	V_{EE} + 1275	V_{CC} − 1000*	V_{CC}	V_{EE} + 1275	V_{CC} − 1000*	V_{CC}	V_{EE} + 1275	V_{CC} − 1000*	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single−Ended) (Note 19) D, $\overline{D}$	V_{IH}− 2600	V_{CC}− 1400*	V_{IH}− 150	V_{IH}− 2600	V_{CC}− 1400*	V_{IH}− 150	V_{IH}− 2600	V_{CC}− 1400*	V_{IH}− 150	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 17)	1.2		3.3	1.2		3.3	1.2		3.3	V
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@V_{IH}) D, $\overline{D}$		30	100		30	100		30	100	μA
	SEL		5	50		5	50		5	50	
I_{IL}	Input LOW Current (@V_{IL}) D, $\overline{D}$		20	100		20	100		20	100	μA
	SEL		5	50		5	50		5	50	

NOTE: GigaComm circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

15. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925 V to −0.165 V.
16. All loading with 50 Ω to V_{CC} − 2.0 V.
17. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
18. V_{IH} cannot exceed V_{CC}.
19. V_{IL} always ≥ V_{EE}.

*Typicals used for testing purposes.

**When an output level of 400 mV is desired and V_{CC} − V_{EE} > 3.0 V, a 2 kΩ resistor should be connected from OLS to V_{EE}.

***The device packaged in FCBGA−16 have maximum ambient temperature specification of 70°C and devices packaged in QFN−16 have maximum ambient temperature specification of 85°C.

Table 12. DC CHARACTERISTICS, NECL INPUT WITH NECL OUTPUT V_{CC} = 0 V; V_{EE} = −3.465 V to −2.375 V (Note 20)

Symbol	Characteristic	−40°C			25°C			70°C(BGA)/85°C(QFN)***			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current	23	30	39	23	30	39	23	30	39	mA
V_{OH}	Output HIGH Voltage (Note 21)	−1040	−990	−940	−1010	−960	−910	−985	−935	−885	mV
V_{OL}	Output LOW Voltage (Note 21)										mV
	−3.465 V ≤ V_{EE} ≤ −3.0 V										
	(V_{OLS} = V_{CC})	−1980	−1830	−1680	−1940	−1790	−1640	−1910	−1760	−1610	
	(V_{OLS} = V_{CC} − 0.4 V)	−1270	−1210	−1150	−1235	−1175	−1115	−1210	−1150	−1090	
	(V_{OLS} = V_{CC} − 0.8 V, OLS = FLOAT)	−1750	−1630	−1510	−1715	−1595	−1475	−1685	−1565	−1445	
	(V_{OLS} = V_{CC} − 1.2 V)	−1040	−990	−940	−1010	−960	−910	−985	−935	−885	
	**(V_{OLS} = V_{EE})	−1515	−1425	−1335	−1480	−1390	−1300	−1450	−1360	−1270	
	−3.0 V < V_{EE} ≤ −2.375 V										
	(V_{OLS} = V_{CC})	−1945	−1795	−1645	−1905	−1755	−1605	−1875	−1725	−1575	
	(V_{OLS} = V_{CC} − 0.4 V)	−1265	−1205	−1145	−1230	−1170	−1110	−1205	−1145	−1085	
	(V_{OLS} = V_{CC} − 0.8 V, OLS = FLOAT)	−1725	−1605	−1485	−1690	−1570	−1450	−1660	−1540	−1420	
	(V_{OLS} = V_{CC} − 1.2 V)	−1045	−995	−945	−1010	−960	−910	−990	−940	−890	
	(V_{OLS} = V_{EE})	−1495	−1405	−1315	−1460	−1370	−1280	−1435	−1345	−1255	
V_{OUTPP}	Output Voltage Amplitude										mV
	−3.465 V ≤ V_{EE} ≤ −3.0 V										
	(V_{OLS} = V_{CC})	750	840		740	830		735	825		
	(V_{OLS} = V_{CC} − 0.4 V)	130	220		125	215		125	215		
	(V_{OLS} = V_{CC} − 0.8 V, OLS = FLOAT)	550	640		545	635		540	630		
	(V_{OLS} = V_{CC} − 1.2 V)	0	0		0	0		0	0		
	**(V_{OLS} = V_{EE})	345	435		340	430		335	425		
	−3.0 V < V_{EE} ≤ −2.375 V										
	(V_{OLS} = V_{CC})	715	805		705	795		700	790		
	(V_{OLS} = V_{CC} − 0.4 V)	125	215		120	210		120	210		
	(V_{OLS} = V_{CC} − 0.8 V, OLS = FLOAT)	525	615		520	610		515	605		
	(V_{OLS} = V_{CC} − 1.2 V)	0	5		0	0		0	5		
	(V_{OLS} = V_{EE})	325	415		320	410		320	410		
V_{IH}	Input HIGH Voltage (Single−Ended) (Note 23) D, $\overline{D}$	V_{EE} + 1275	V_{CC} − 1000*	V_{CC}	V_{EE} + 1275	V_{CC} − 1000*	V_{CC}	V_{EE} + 1275	V_{CC} − 1000*	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single−Ended) (Note 24) D, $\overline{D}$	V_{IH}− 2600	V_{CC}− 1400*	V_{IH}− 150	V_{IH}− 2600	V_{CC}− 1400*	V_{IH}− 150	V_{IH}− 2600	V_{CC}− 1400*	V_{IH}− 150	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 22)	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@V_{IH}) D, $\overline{D}$		30	100		30	100		30	100	μA
	SEL		5	50		5	50		5	50	
I_{IL}	Input LOW Current (@V_{IL}) D, $\overline{D}$		20	100		20	100		20	100	μA
	SEL		5	50		5	50		5	50	

NOTE: GigaComm circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

20. Input and output parameters vary 1:1 with V_{CC}.
21. All loading with 50 Ω to V_{CC} − 2.0 V.
22. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
23. V_{IH} cannot exceed V_{CC}.
24. V_{IL} always ≥ V_{EE}.

*Typicals used for testing purposes.
**When an output level of 400 mV is desired and V_{CC} − V_{EE} > 3.0 V, a 2 kΩ resistor should be connected from OLS to V_{EE}.
***The device packaged in FCBGA−16 have maximum ambient temperature specification of 70°C and devices packaged in QFN−16 have maximum ambient temperature specification of 85°C.

Table 13. AC CHARACTERISTICS for FCBGA−16

V_{CC} = 0 V; V_{EE} = −3.465 V to −2.375 V or V_{CC} = 2.375 V to 3.465 V; V_{EE} = 0 V

		−40°C			25°C			70°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Frequency (See Figure 8) (Note 25)	7	8		7	8		7	8		GHz
V_{OUTPP}	Output Voltage Amplitude (OLS = V_{CC}) $f_{in} \le 7$ GHz	550	740		500	720		450	700		mV
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential D/SEL → Q	110	160	210	115	165	215	120	170	220	ps
t_{SKEW}	Duty Cycle Skew (Note 26)		5	15		5	15		5	15	ps
t_{SKEW}	Channel Skew Q → D/SEL		5	20		5	20		5	20	ps
t_{JITTER}	RMS Random Clock Jitter (See Figure 8) (Note 25) $f_{in} \le 7$ GHz		0.5	1.5		0.5	1.5		0.5	1.5	ps
	Peak−to−Peak Data Dependent Jitter $f_{in} \le 7$ Gb/s		12			12			12		
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 27)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times (20% − 80%) (Q, $\overline{Q}$) @ 1 GHz	20	40	65	20	40	65	20	40	65	ps

25. Measured using a 500 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} − 2.0 V. Input edge rates 40 ps (20% − 80%).
26. $t_{SKEW} = |t_{PLH} - t_{PHL}|$ for a nominal 50% differential clock input waveform. See Figure 12.
27. V_{INPP} (max) cannot exceed $V_{CC} - V_{EE}$.

Table 14. AC CHARACTERISTICS for QFN−16

V_{CC} = 0 V; V_{EE} = −3.465 V to −2.375 V or V_{CC} = 2.375 V to 3.465 V; V_{EE} = 0 V

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Frequency (See Figure 8) (Note 28)	7	8		7	8		7	8		GHz
V_{OUTPP}	Output Voltage Amplitude $f_{in} \le 7$ GHz	590	730		470	720		540	700		mV
	(OLS = V_{CC}) f_{in} = 8 GHz	270	440		230	420		180	390		mV
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential D/SEL → Q	110	160	210	115	165	215	120	170	220	ps
t_{SKEW}	Duty Cycle Skew (Note 29)		5	15		5	15		5	15	ps
t_{SKEW}	Channel Skew Q → D/SEL		5	20		5	20		5	20	ps
t_{JITTER}	RMS Random Clock Jitter (See Figure 8) (Note 31) $f_{in} \le 7$ GHz		0.5	1.5		0.5	1.5		0.5	1.5	ps
	Peak−to−Peak Data Dependent Jitter (Note 32) $f_{in} \le 7$ Gb/s		12			12			12		
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 30)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times (20% − 80%) (Q, $\overline{Q}$)										ps
	@ 1 GHz t_r	30	45	60	30	45	60	30	45	60	
	t_f	17	35	65	17	35	65	17	35	65	

28. Measured using a 500 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} − 2.0 V. Input edge rates 40 ps (20% − 80%).
29. $t_{SKEW} = |t_{PLH} - t_{PHL}|$ for a nominal 50% differential clock input waveform. See Figure 12.
30. V_{INPP} (max) cannot exceed $V_{CC} - V_{EE}$.
31. Additive RMS jitter with 50% duty cycle clock signal at 7 GHz.
32. Additive Peak−to−Peak data dependent jitter with NRZ PRBS 2^{31}−1 data rate at 7 Gb/s.

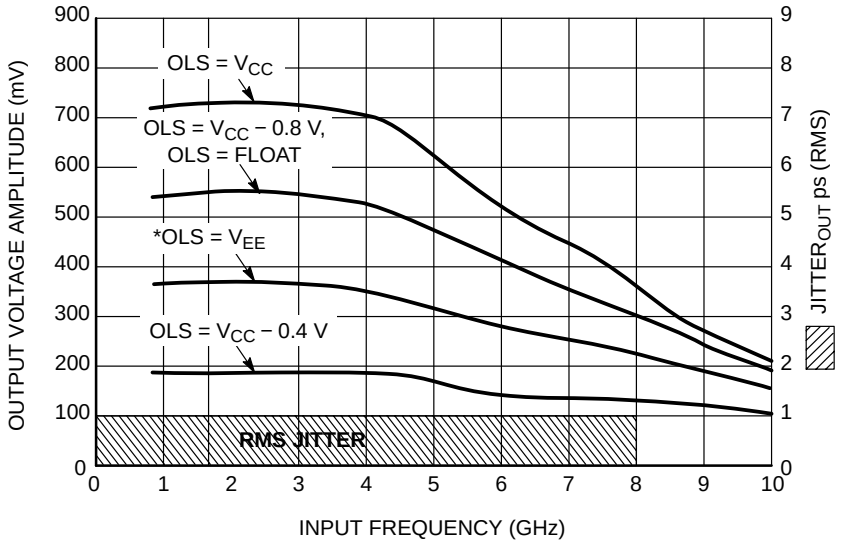


Figure 8. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) for 2:1 MUX Mode (V_{CC} − V_{EE} = 2.5 V @ 25°C; Repetitive 1010 Input Data Pattern)

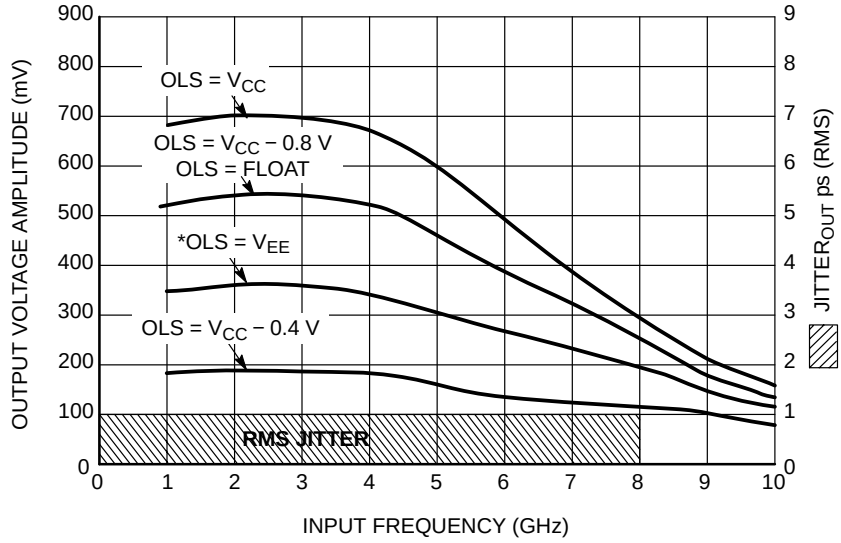


Figure 9. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) for 2:1 MUX Mode (V_{CC} − V_{EE} = 3.3 V @ 25°C; Repetitive 1010 Input Data Pattern)

*When an output level of 400 mV is desired and V_{CC} − V_{EE} > 3.0 V, a 2 kΩ resistor should be connected from OLS to V_{EE}.

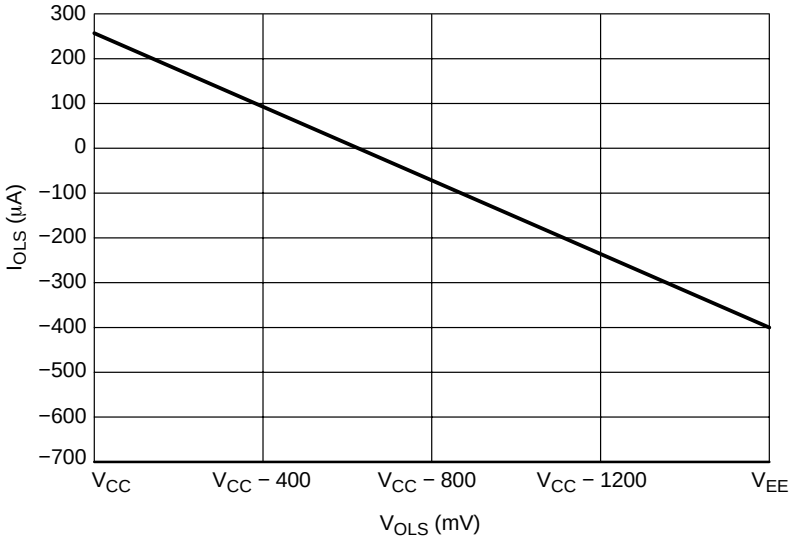


Figure 10. Typical OLS Input Current vs. OLS Input Voltage (V_{CC} − V_{EE} = 3.3 V @ 25°C)

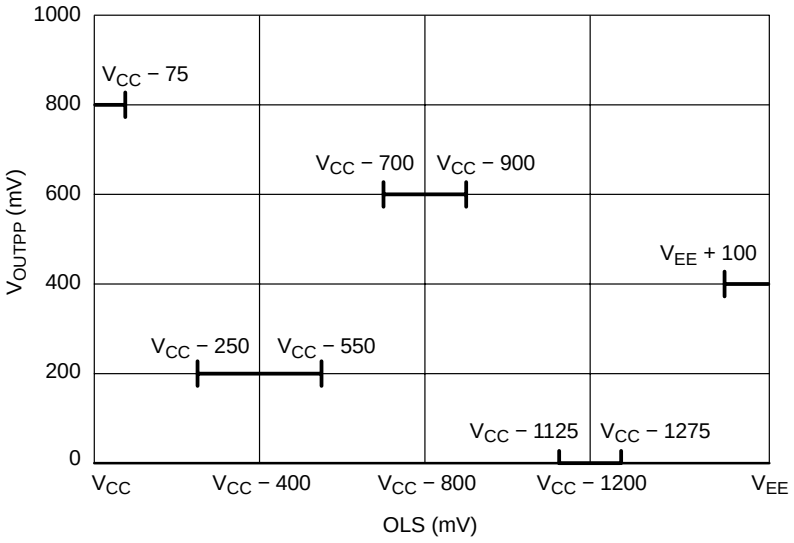


Figure 11. OLS Operating Area

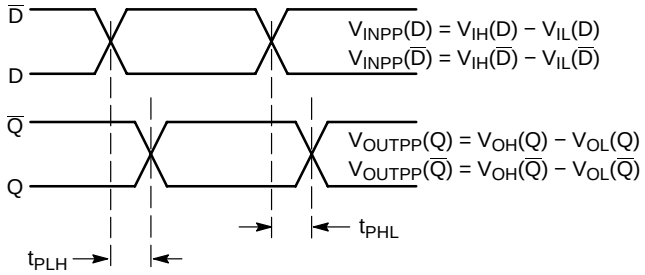


Figure 12. AC Reference Measurement

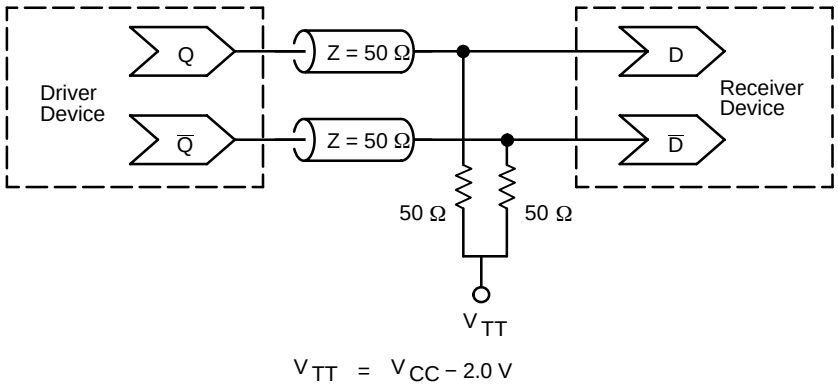
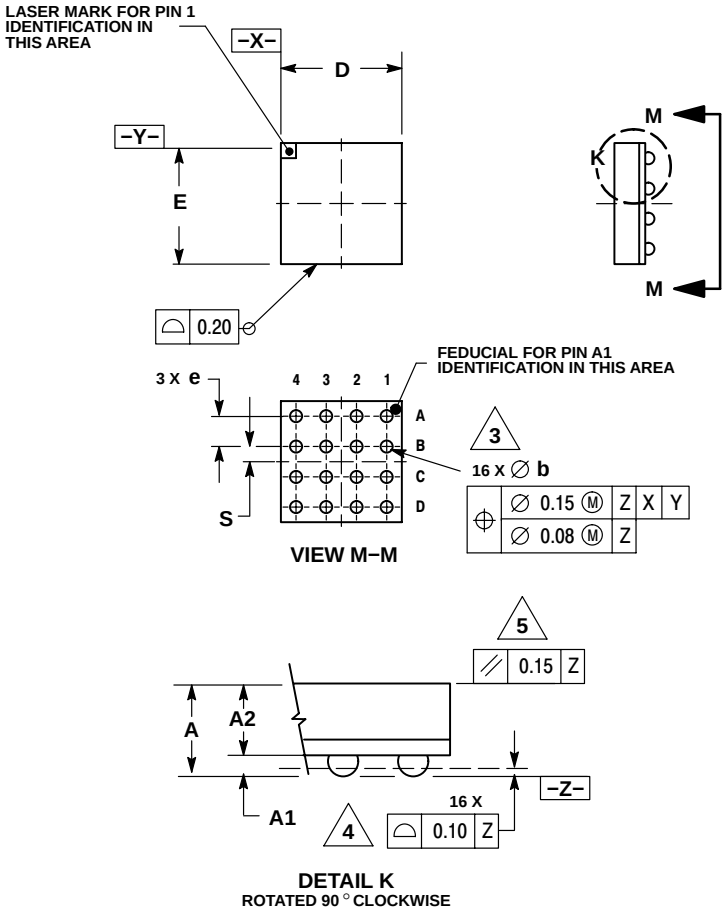


Figure 13. Typical Termination for Output Driver and Device Evaluation (Refer to Application Note AND8020 − Termination of ECL Logic Devices)

PACKAGE DIMENSIONS

FCBGA−16
BA SUFFIX
PLASTIC 4 X 4 (mm) BGA FLIP CHIP PACKAGE
CASE 489−01
ISSUE O

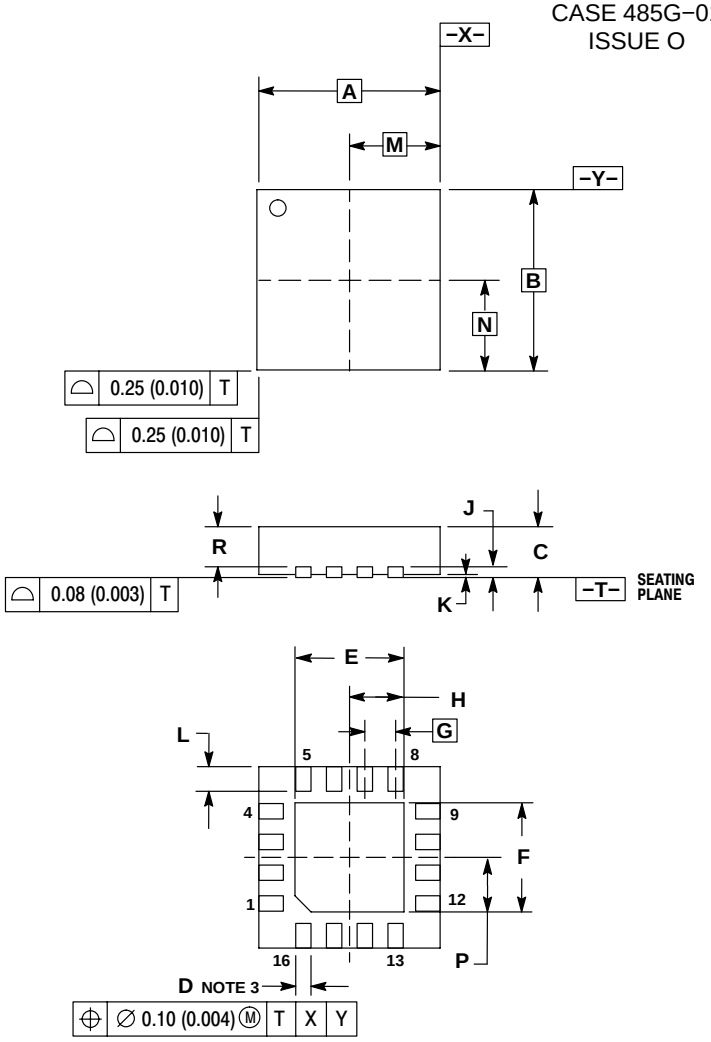


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MILLIMETERS	
DIM	MIN	MAX
A	1.40 MAX	
A1	0.25	0.35
A2	1.20 REF	
b	0.30	0.50
D	4.00 BSC	
E	4.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

PACKAGE DIMENSIONS

16 PIN QFN
MN SUFFIX
CASE 485G−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	3.00 BSC		0.118 BSC	
B	3.00 BSC		0.118 BSC	
C	0.80	1.00	0.031	0.039
D	0.23	0.28	0.009	0.011
E	1.75	1.85	0.069	0.073
F	1.75	1.85	0.069	0.073
G	0.50 BSC		0.020 BSC	
H	0.875	0.925	0.034	0.036
J	0.20 REF		0.008 REF	
K	0.00	0.05	0.000	0.002
L	0.35	0.45	0.014	0.018
M	1.50 BSC		0.059 BSC	
N	1.50 BSC		0.059 BSC	
P	0.875	0.925	0.034	0.036
R	0.60	0.80	0.024	0.031

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