General Description

The 87973 is a LVCMOS/LVTTL clock generator. The 87973 has three selectable inputs and provides fourteen LVCMOS/LVTTL outputs.

The 87973 is a highly flexible device. The three selectable inputs (1 differential and 2 single ended inputs) are often used in systems requiring redundant clock sources. Up to three different output frequencies can be generated among the three output banks.

The three output banks and feedback output each have their own output dividers which allows the device to generate a multitude of different bank frequency ratios and output-to-input frequency ratios. In addition, 2 outputs in Bank C (QC2, QC3) can be selected to be inverting or non-inverting. The output frequency range is 8.33MHz to125MHz. The input frequency range is 5MHz to 120MHz.

The 87973 also has a QSYNC output which can by used for system synchronization purposes. It monitors Bank A and Bank C outputs and goes low one period prior to coincident rising edges of Bank A and Bank C clocks. QSYNC then goes high again when the coincident rising edges of Bank A and Bank C occur. This feature is used primarily in applications where Bank A and Bank C are running at different frequencies, and is particularly useful when they are running at non-integer multiples of one another.

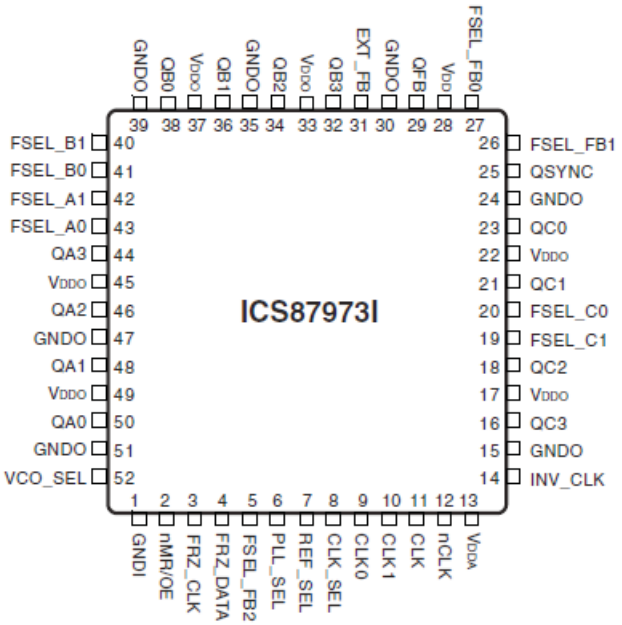
Example Applications:

1. *System Clock generator:* Use a 16.66MHz reference clock to generate eight 33.33MHz copies for PCI and four 100MHz copies for the CPU or PCI-X.
2. *Line Card Multiplier:* Multiply differential 62.5MHz from a back plane to single-ended 125MHz for the line Card ASICs and Gigabit Ethernet Serdes.
3. *Zero Delay buffer for Synchronous memory:* Fan out up to twelve 100MHz copies from a memory controller reference clock to the memory chips on a memory module with zero delay.

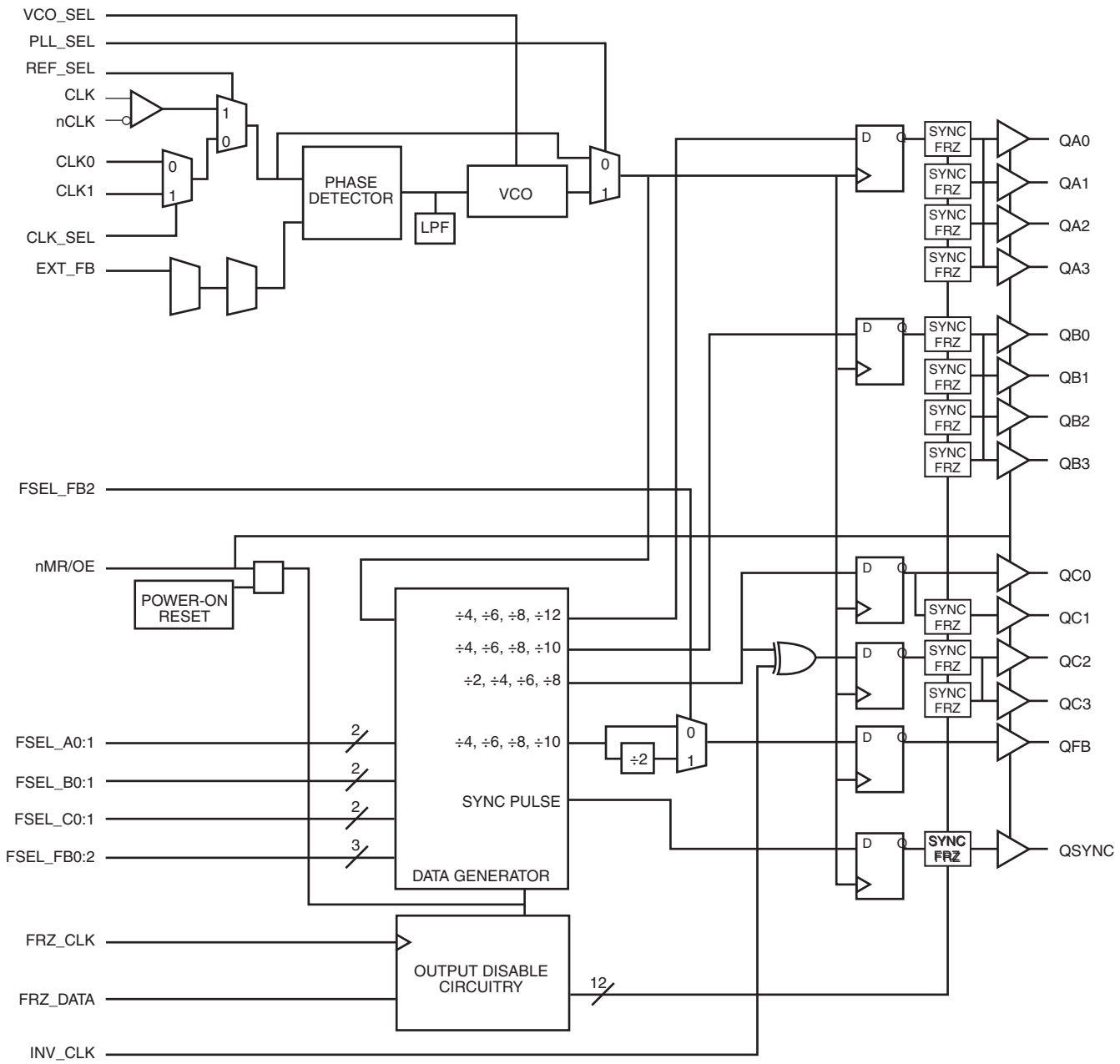
Features

- Fully integrated PLL
- Fourteen LVCMOS/LVTTL outputs; twelve clock outputs, one feedback, one sync
- Selectable LVCMOS/LVTTL or differential CLK, nCLK inputs
- CLK0, CLK1 can accept the following input levels: LVCMOS or LVTTL
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Output frequency range: 8.33MHz to 125MHz
- VCO range: 200MHz to 480MHz
- Output skew: 550ps (maximum)
- Cycle-to-cycle jitter: ±100ps (typical)
- Full 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in lead-free RoHS compliant package
- Compatible with PowerPC™ and Pentium™ Microprocessors

Pin Assignment



Block Diagram



Simplified Block Diagram

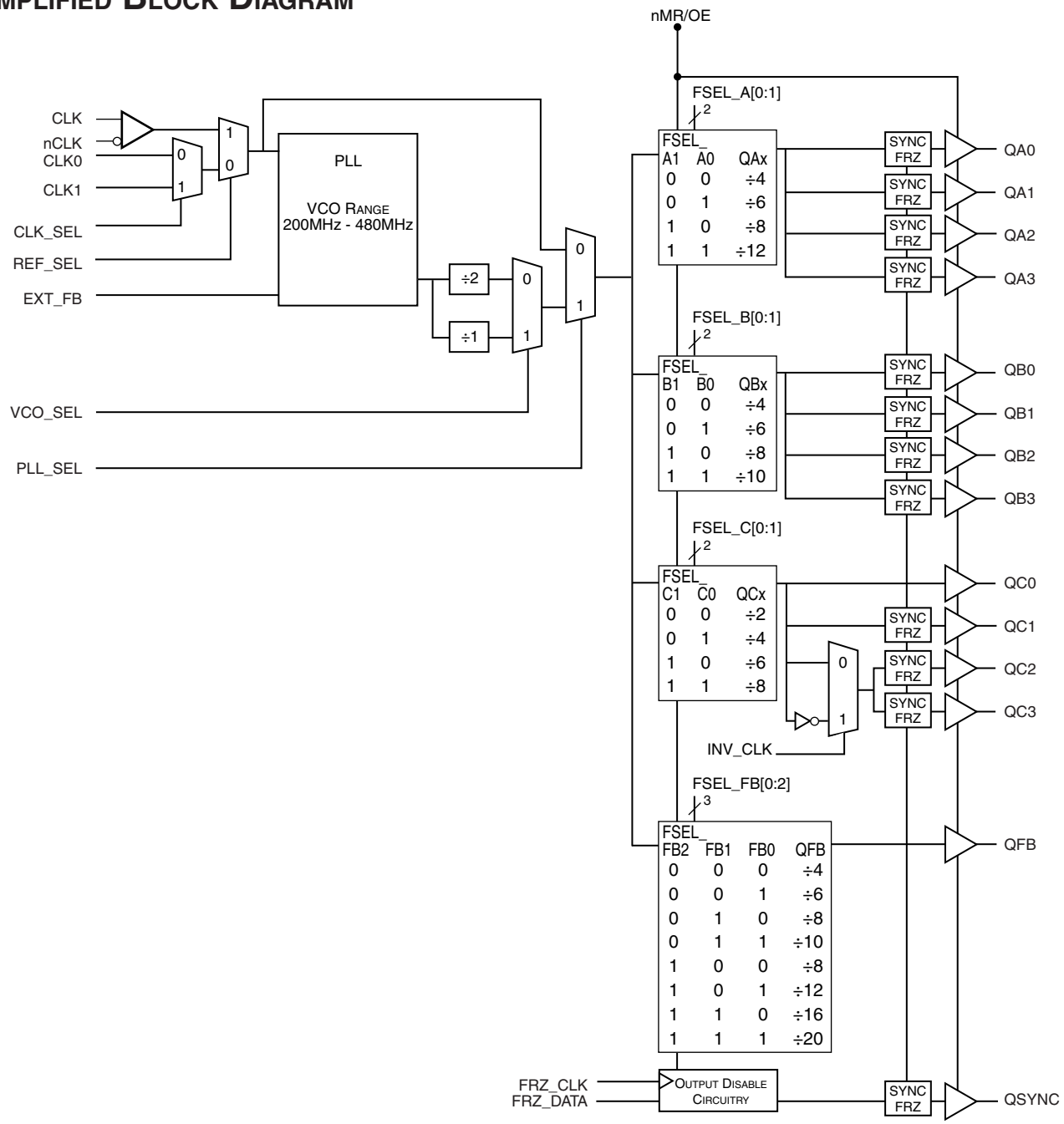


Table 1. Pin Descriptions

Number	Name	Type		Description
1	GNDI	Power		Power supply ground.
2	nMR/OE	Input	Pullup	Master reset and output enable. When HIGH, enables the outputs. When LOW, resets the outputs to tristate and resets output divide circuitry. Enables and disables all outputs. LVCMOS / LVTTL interface levels.
3	FRZ_CLK	Input	Pullup	Clock input for freeze circuitry. LVCMOS / LVTTL interface levels.
4	FRZ_DATA	Input	Pullup	Configuration data input for freeze circuitry. LVCMOS / LVTTL interface levels.
5, 26, 27	FSEL_FB2, FSEL_FB1, FSEL_FB0	Input	Pullup	Select pins control Feedback Divide value. LVCMOS / LVTTL interface levels.
6	PLL_SEL	Input	Pullup	Selects between the PLL and reference clocks as the input to the output dividers. When HIGH, selects PLL. When LOW, bypasses the PLL. LVCMOS / LVTTL interface levels.
7	REF_SEL	Input	Pullup	Selects between CLK0 or CLK1 and CLK, nCLK inputs. When HIGH, selects CLK, nCLK. When LOW, selects CLK0 or CLK1. LVCMOS / LVTTL interface levels.
8	CLK_SEL	Input	Pullup	Clock select input. Selects between CLK0 and CLK1 as phase detector reference. When LOW, selects CLK0. When HIGH, selects CLK1. LVCMOS / LVTTL interface levels.
9, 10	CLK0,CLK1	Input	Pullup	Reference clock inputs. LVCMOS / LVTTL interface levels.
11	CLK	Input	Pullup	Non-inverting differential clock input.
12	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
13	V_{DDA}	Power		Analog supply pin.
14	INV_CLK	Input	Pullup	Inverted clock select for QC2 and QC3 outputs. LVCMOS / LVTTL interface levels.
15, 24, 30, 35, 39, 47, 51	GNDO	Power		Power supply ground.
16, 18, 21, 23	QC3, QC2, QC1, QC0	Output		Bank C clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
17, 22, 33, 37, 45, 49	V_{DDO}	Power		Output supply pins.
19, 20	FSEL_C1, FSEL_C0	Input	Pullup	Select pins for Bank C outputs. LVCMOS / LVTTL interface levels.
25	QSYNC	Output		Synchronization output for Bank A and Bank C. Refer to Figure 1, Timing Diagrams. LVCMOS / LVTTL interface levels.
28	V_{DD}	Power		Core supply pins.
29	QFB	Output		Feedback clock output. LVCMOS / LVTTL interface levels.
31	EXT_FB	Input	Pullup	Extended feedback. LVCMOS / LVTTL interface levels.
32, 34, 36, 38	QB3, QB2, QB1, QB0	Output		Bank B clock outputs.7Ω typical output impedance. LVCMOS / LVTTL interface levels.
40, 41	FSEL_B1, FSEL_B0	Input	Pullup	Select pins for Bank B outputs. LVCMOS / LVTTL interface levels.
42, 43	FSEL_A1, FSEL_A0	Input	Pullup	Select pins for Bank A outputs. LVCMOS / LVTTL interface levels.
44, 46, 48, 50	QA3, QA2, QA1, QA0	Output		Bank A clock outputs.7Ω typical output impedance. LVCMOS / LVTTL interface levels.
52	VCO_SEL	Input	Pullup	Selects VCO. When HIGH, selects VCO ÷ 1. When LOW, selects VCO ÷ 2. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}/ $R_{PULLDOWN}$	Input Pullup/Pulldown Resistor			51		kW
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDA}, V_{DDO} = 3.465V			18	pF
R_{OUT}	Output Impedance		5	7	12	W

Table 3A. Output Bank Configuration Select Function Table

Inputs		Outputs	Inputs		Outputs	Inputs		Outputs
FSEL_A1	FSEL_A0	QA	FSEL_B1	FSEL_B0	QB	FSEL_C1	FSEL_C0	QC
0	0	÷4	0	0	÷4	0	0	÷2
0	1	÷6	0	1	÷6	0	1	÷4
1	0	÷8	1	0	÷8	1	0	÷6
1	1	÷12	1	1	÷10	1	1	÷8

Table 3B. Feedback Configuration Select Function Table

Inputs			Outputs
FSEL_FB2	FSEL_FB1	FSEL_FB0	QFB
0	0	0	÷4
0	0	1	÷6
0	1	0	÷8
0	1	1	÷10
1	0	0	÷8
1	0	1	÷12
1	1	0	÷16
1	1	1	÷20

Table 3C. Control Input Select Function Table

Control Pin	Logic 0	Logic 1
VCO_SEL	VCO/2	VCO
REF_SEL	CLK0 or CLK1	CLK, nCLK
CLK_SEL	CLK0	CLK1
PLL_SEL	BYPASS PLL	Enable PLL
nMR/OE	Master Reset/Output Hi Z	Enable Outputs
INV_CLK	Non-Inverted QC2, QC3	Inverted QC2, QC3

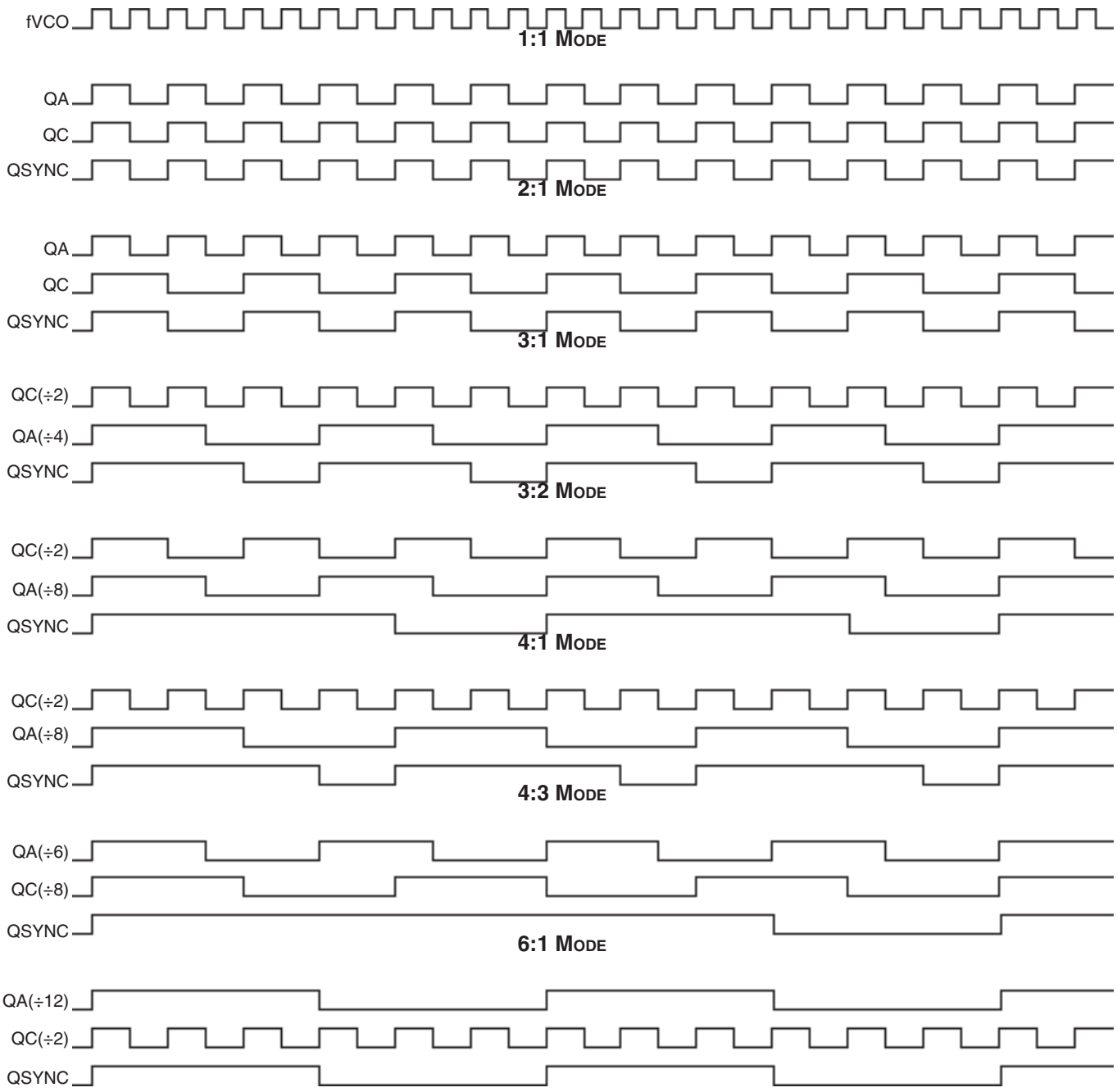


Figure 1. Timing Diagrams

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	42.3°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		2.935	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	All power pins			225	mA
I_{DDA}	Analog Supply Current				20	mA

NOTE: Special thermal handling may be required in some configurations.

Table 4B. DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		3.6	V
V_{IL}	Input Low Voltage				0.8	V
I_{IN}	Input Current				±120	µA
V_{OH}	Output High Voltage	I_{OH} = -20mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 20mA			0.5	V
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1, 2	CLK, nCLK	0.3		1	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2	CLK, nCLK	V_{DD} - 2V		V_{DD} - 0.6V	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2. For single ended applications, the maximum input voltage for CLK and nCLK is V_{DD} + 0.3V.

Table 5. Input Frequency Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	CLK0, CLK1, CLK, nCLK; NOTE 1				120	MHz
		FRZ_CLK				20	MHz

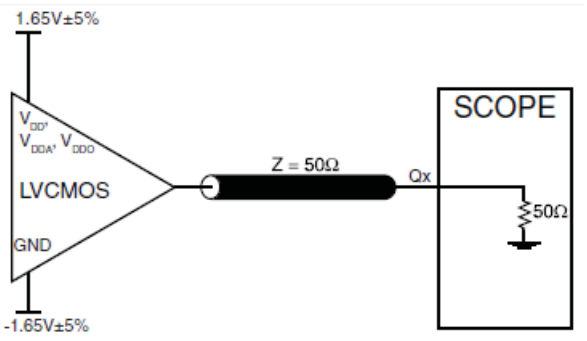
NOTE 1: Input frequency depends on the feedback divide ratio to ensure “clock * Feedback Divide” is in the VCO range of 200MHz to 480MHz.

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

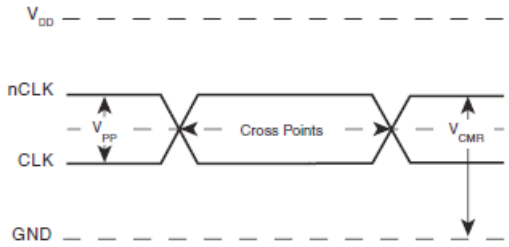
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Output Frequency		÷2			125	MHz
			÷4			120	MHz
			÷6			80	MHz
			÷8			60	MHz
t(Ø)	Static Phase Offset; NOTE 1	CLK0	QFB ÷8 In Frequency = 50MHz	-70	130	330	ps
		CLK1		-130	70	270	ps
		CLK, nCLK		-225	-25	175	ps
$t_{sk(o)}$	Output Skew; NOTE 2					550	ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 3, 4				±100		ps
f_{VCO}	PLL VCO Lock Range			200		480	MHz
t_{LOCK}	PLL Lock Time; NOTE 3					10	mS
t_R / t_F	Output Rise/Fall Time; NOTE 3		0.8V to 2V	0.15		1.2	ns
t_{PW}	Output Pulse Width			$t_{PERIOD}/2$ - 750	$t_{PERIOD}/2$ ± 500	$t_{PERIOD}/2$ + 750	ps
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 3			2		10	ns
t_{PLZ}, t_{PHZ}	Output Disable TIme; NOTE 3			2		8	ns

NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

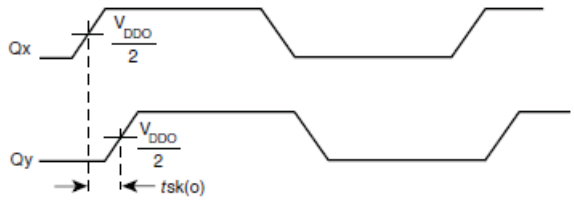
Parameter Measurement Information



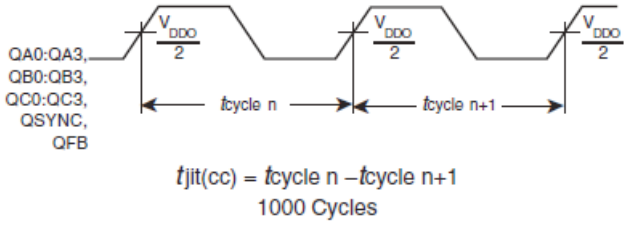
3.3V Output Load AC Test Circuit



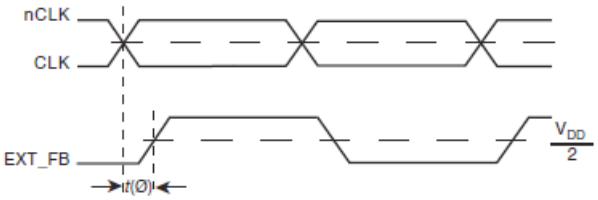
Differential Input Level



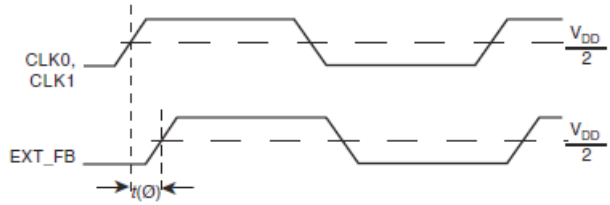
Output Skew



Cycle-to-Cycle Jitter

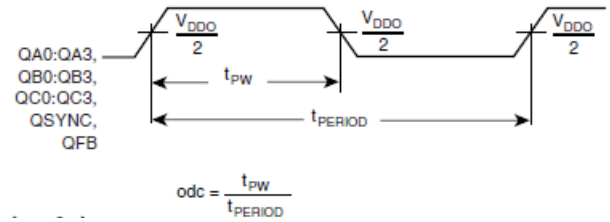


Static Phase Offset (Differential)



Static Phase Offset (LVCMOS)

Output Rise/Fall Time



t_{PW} & t_{Period}

Application Information

Using The Output Freeze Circuitry

Overview

To enable low power states within a system, each output of 87973 (Except QC0 and QFB) can be individually frozen (stopped in the logic "0" state) using a simple serial interface to a 12 bit shift register. A serial interface was chosen to eliminate the need for each output to have its own Output Enable pin, which would dramatically increase pin count and package cost. Common sources in a system that can be used to drive the 87973 serial interface are FPGA's and ASICs.

Protocol

The Serial interface consists of two pins, FRZ_Data (Freeze Data) and FRZ_CLK (Freeze Clock). Each of the outputs which can be frozen has its own freeze enable bit in the 12 bit shift register. The sequence is started by supplying a logic "0" start bit followed by 12NRZ freeze enable bits. The period of each FRZ_DATA bit equals the period of the FRZ_CLK signal. The FRZ_DATA serial transmission should be timed so the 87973 can sample each FRZ_DATA bit with the rising edge of the FRZ_CLK signal. To place an output in the freeze state, a logic "0" must be written to the respective freeze enable bit in the shift register. To unfreeze an output, a logic "1" must be written to the respective freeze enable bit. Outputs will not become enabled/disabled until all 12 data bits are shifted into the shift register. When all 12 data bits are shifted in the register, the next rising edge of FRZ_CLK will enable or disable the outputs. If the bit that is following the 12th bit in the register is a logic "0", it is used for the start bit of the next cycle; otherwise, the device will wait and won't start the next cycle until it sees a logic "0" bit. Freezing and unfreezing of the output clock is synchronous (see the timing diagram below). When going into a frozen state, the output clock will go LOW at the time it would normally go LOW, and the freeze logic will keep the output low until unfrozen. Likewise, when coming out of the frozen state, the output will go HIGH only when it would normally go HIGH. This logic, therefore, prevents runt pulses when going into and out of the frozen state.

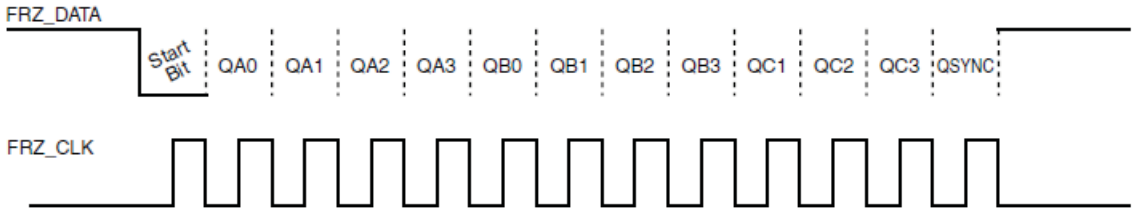


Figure 2A. Freeze Data Input Protocol

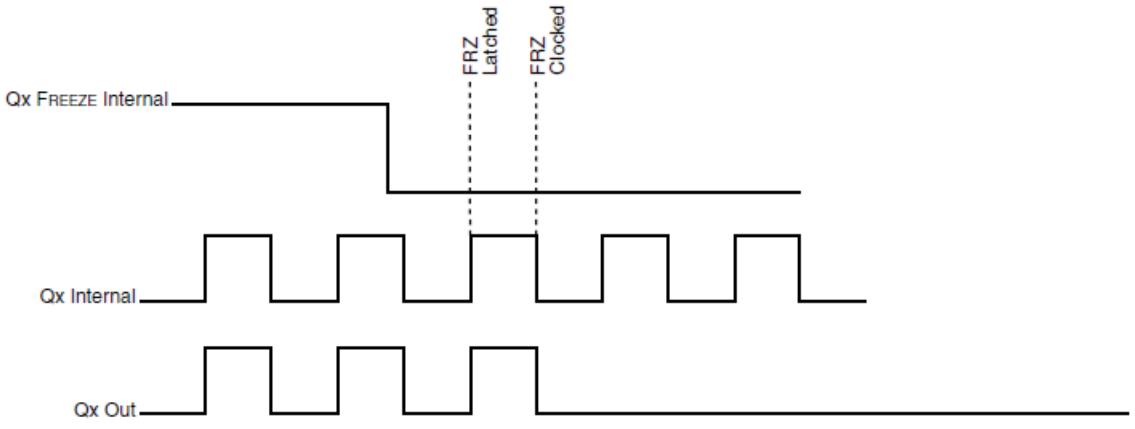


Figure 2B. Output Disable Timing

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 87973 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 3* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin. The 10Ω resistor can also be replaced by a ferrite bead.

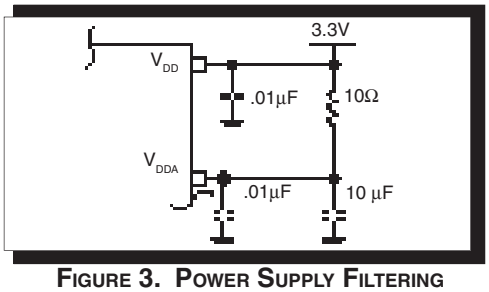


Figure 3. Power Supply Filtering

Wiring the Differential Input to Accept Single Ended Levels

Figure 4 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

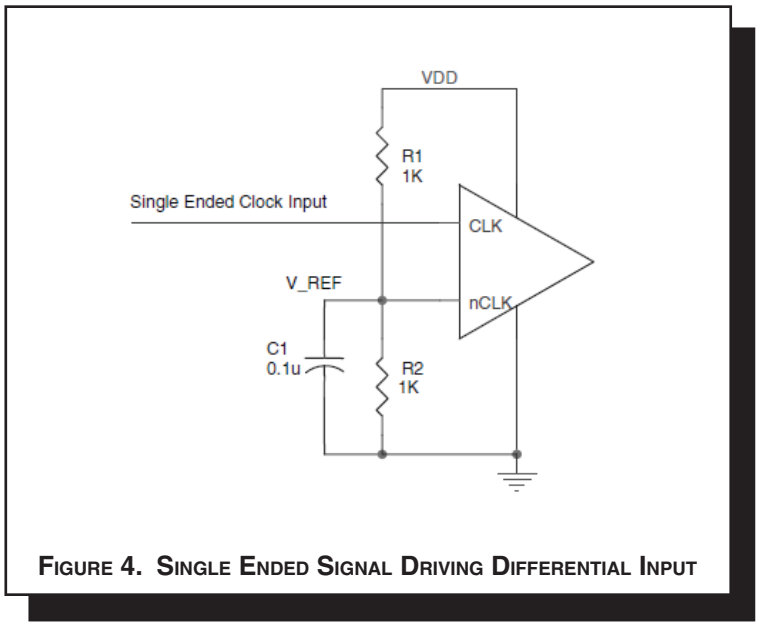


Figure 4. Single Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must mee t the V_{PP} and V_{CMR} input requirements. Figures 5A to 5D show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 5A,* the input termination applies for LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

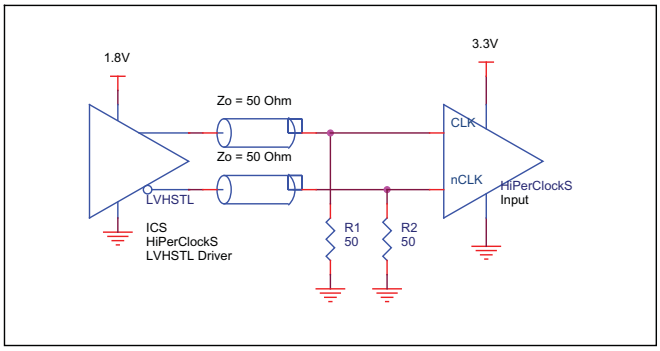


Figure 5A. CLK/nCLK Input Driven by LVHSTL Driver

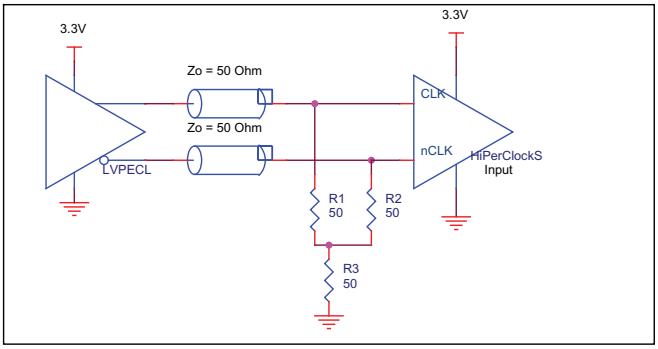


Figure 5B. CLK/nCLK Input Driven by 3.3V LVPECL Driver

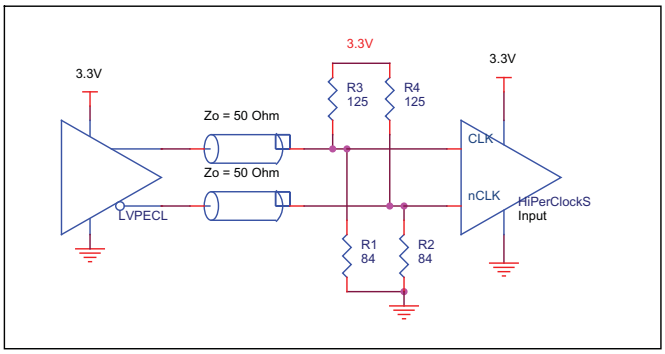


Figure 5C. CLK/nCLK Input Driven by 3.3V LVPECL Driver

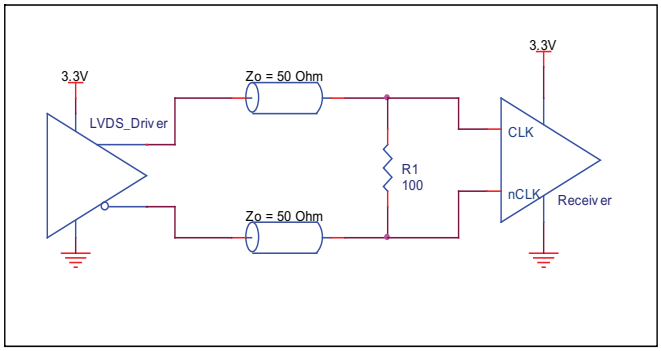


Figure 5D. CLK/nCLK Input Driven by 3.3V LVDS Driver

Recommendations for Unused Input and Output Pins

Inputs:

CLK Input:

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

CLK/nCLK Input:

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Output:

All unused LVCMOS output can be left floating. There should be no trace attached.

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	58.0°C/W	47.1°C/W	42.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	42.3°C/W	36.4°C/W	34.0°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for 87973 is: 8364

Package Outline - Y Suffix for 52 Lead LQFP

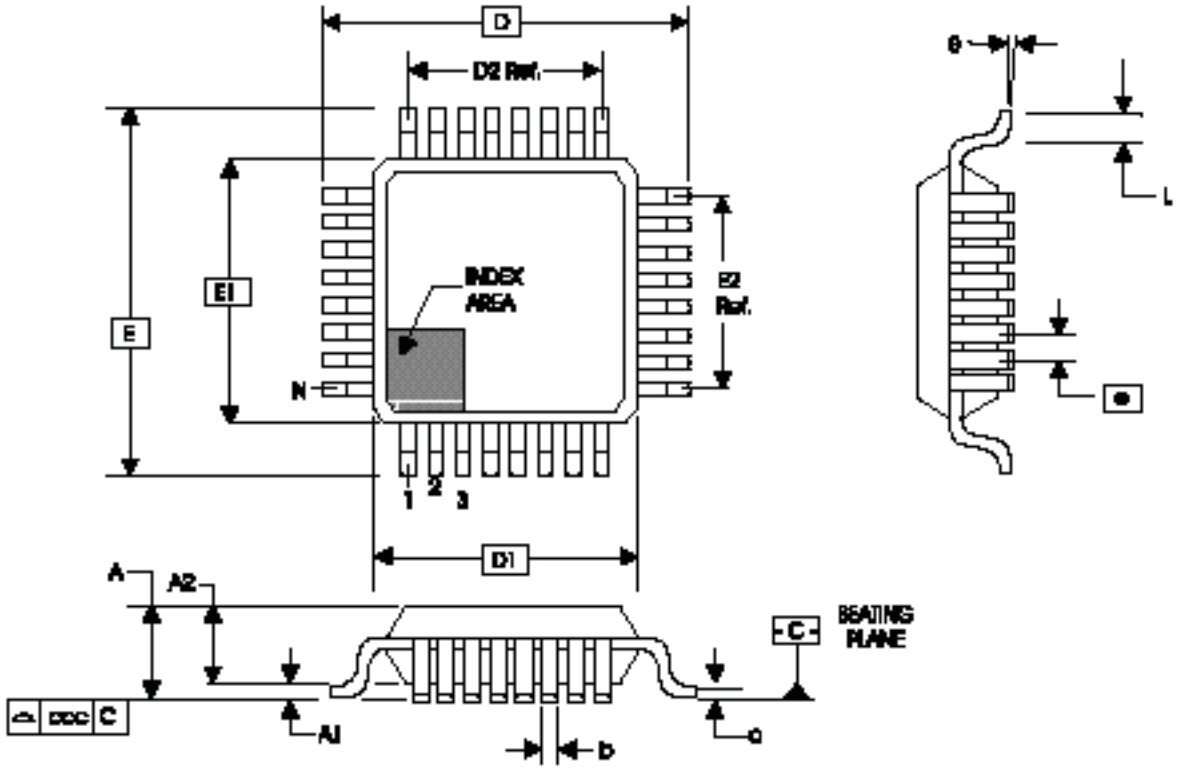


Table 8. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BCC		
	MINIMUM	NOMINAL	MAXIMUM
N	52		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
c	0.09	--	0.20
D	12.00 BASIC		
D1	10.00 BASIC		
E	12.00 BASIC		
E1	10.00 BASIC		
e	0.65 BASIC		
L	0.45	--	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87973DYILF	ICS87973DYILF	52 Lead “Lead-Free” LQFP	tray	-40°C to 85°C
87973DYILFT	ICS87973DYILF	52 Lead “Lead-Free” LQFP	tape & reel	-40°C to 85°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T1	4	Pin Description Table - added pins 20 and 21.	9/9/02
A		2	Block Diagram - added missing dividers to the Data Generator.	10/18/02
B	T4B	7	DC Characteristics table - updated VCMR values from GND + 1.5V min., V_{DD} max. to V_{DD} - 2V min., V_{DD} - 0.6V max.	10/23/02
B	T1 T8	4 12	Pin Description Table - corrected CLK Type to read Pullup from Pulldown. Revised Package Drawing. Corrected Package Dimensions table to correspond with the Package Drawing.	11/18/02
B		1 12	Added LVTTL to title. Corrected Package Outline to correspond with the Package Dimensions table.	12/10/02
C	T2 T4A 	5 7 11 12	Pin Characteristics - changed the C_{PD} limit from 25pF typical to 18pf max. Power Supply Table - changed the I_{DD} limit from 215mA max. to 225mA max. Application Information: Added sections, “Power Supply Filtering Techniques” and “Wiring the Differential Level...” Added “Differential Clock Input Interface” section.	3/21/03
C	T2	5 10	Pin Characteristics - changed C_{IN} from 4pF max. to 4pF typical. Corrected Freeze Data labeling on Figure 2A.	5/7/03
D	T4A	7	Power Supply Table - changed V_{DDA} minimum from 3.135V to 2.935V.	6/27/03
D	T1 T2	4 5	Pin Characteristics Table - added Pullup/Pulldown to pin 12, nCLK. Pin Characteristics Table - added to R_{OUT} 5Ω min. and 12Ω max.	7/9/03
D	T9	1 12 15	Features section - added lead-free bullet. Added *Recommendations for Unused Input and Output Pins.* Ordering Information Table - added lead-free part number, marking and note.	5/19/06
D	T9	 15 17	Updated datasheet’s header/footer with IDT from ICS. Removed ICS”prefix from Part/Order Number column. Added Contact Page.	8/15/10
D	T9	15	Ordering Information - removed leaded devices, quantity for tape & reel and LF suffix note. Updated DS header and footer.	12/7/15

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