MOSFET

Metal Oxide Semiconductor Field Effect Transistor

Bare Die

OptiMOS™3 Power MOS Transistor Chip
IPC014N03L3

Data Sheet

Rev. 2.5
Final

Industrial & Multimarket

1 Description

- N-channel enhancement mode
- For dynamic characterization refer to the datasheet of IPD135N03LG
- AQL 0.65 for visual inspection according to failure catalogue
- Electrostatic Discharge Sensitive Device according to MIL-STD 883C
- Die bond: soldered or glued
- Backside metallization: NiV system
- Frontside metallization: AlCu system
- Passivation: nitride + imide

Power MOS Transistor Chip

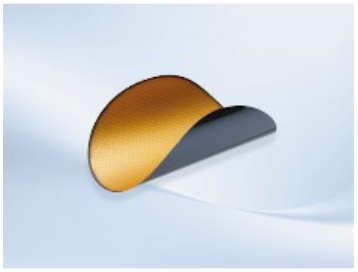
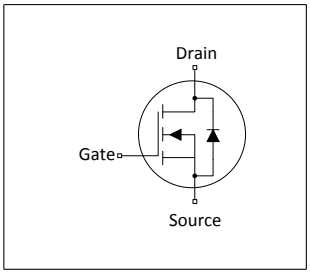


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{(BR)DSS}$	30	V
$R_{DS(on)}$	13.5[1)]	mΩ
Die size	1.64 x 0.845	mm^2
Thickness	175	µm



Type / Ordering Code	Package	Marking	Related Links
IPC014N03L3	Chip	not defined	-

2 Electrical Characteristics on Wafer Level

at T_j = 25°C, unless otherwise specified

Table 2

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	V_{GS}=0 V ,I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1	-	2.2	V	V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	2	µA	V_{GS}=0 V ,V_{DS}=30 V
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V ,V_{DS}=0 V
Drain-source on- resistance	$R_{DS(on)}$	-	10.3[2)]	50[3)]	mΩ	V_{GS}=10 V ,I_D=2.0 A
Reverse diode forward on-voltage	V_{SD}	-	0.86	1.1	V	V_{GS}=0 V ,I_F=1A

[1)] packaged in a PG-TO263-7 (see ref. product)
[2)] typical bare die $R_{DS(on)}$; V_{GS}=10 V, when used with 4x500µm Al-wedge double stitch bonding
[3)] limited by wafer test-equipment

3 Package Outlines

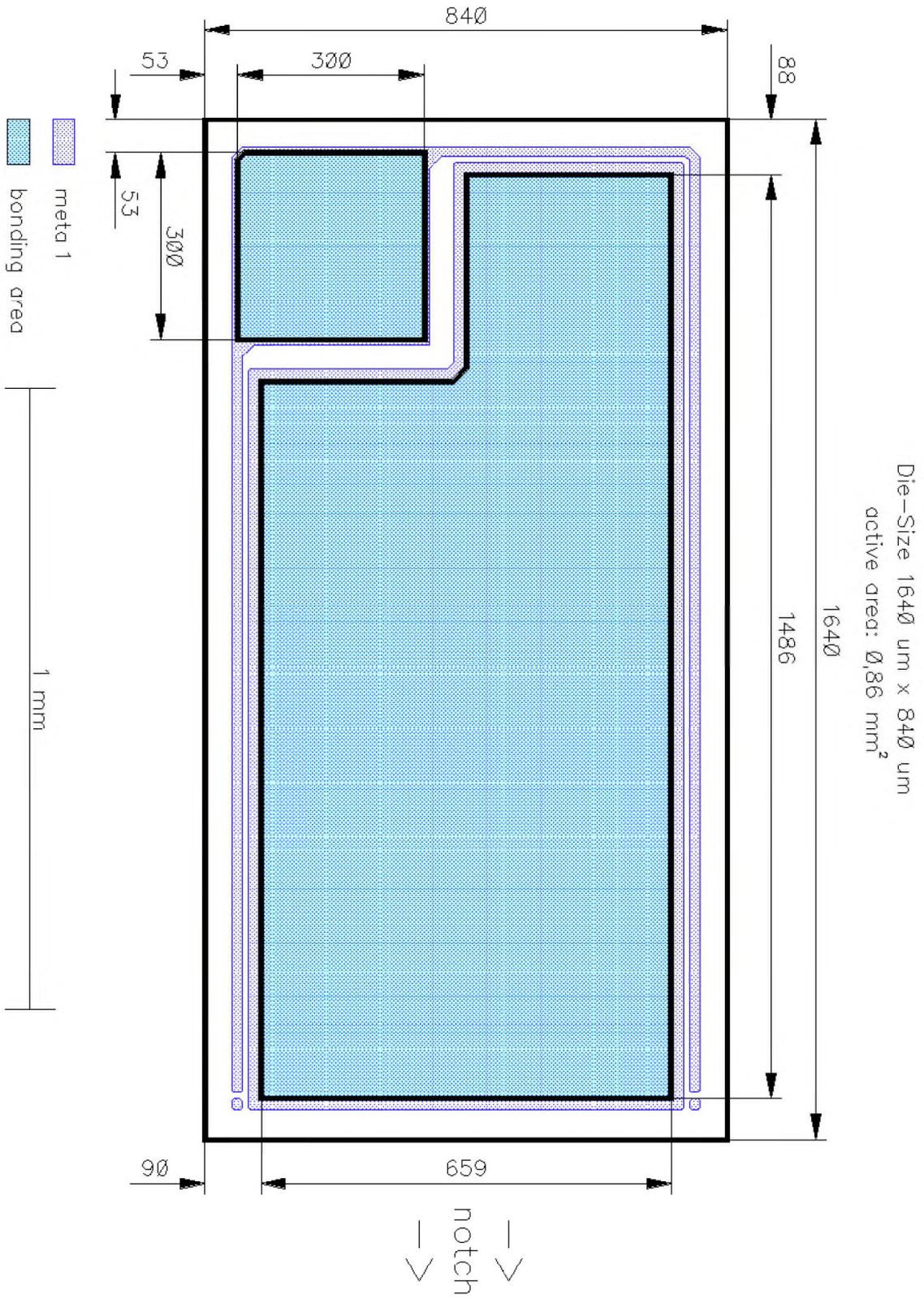


Figure 1 Outline Chip, dimensions in µm

Revision History

IPC014N03L3

Revision: 2014-10-03, Rev. 2.5

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.5	2014-10-03	Release Final Version

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