TE0320 Series User Manual

Xilinx Spartan-3A DSP Industrial-Grade FPGA Micromodule

Overview

The TE0320 is an industrial-grade FPGA micromodule integrating a leading-edge *Xilinx Spartan-3A DSP* FPGA, a USB 2.0 microcontroller, 32-bit wide 128 MByte DDR RAM, 4 MByte Flash memory for configuration and operation, and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/Os is provided via robust board-to-board (B2B) connectors. All this on a tiny footprint, **smaller than a credit card**, at the most competitive price. Hardware and software development environment as well as reference designs are available at: www.trenz-electronic.de.

Sample Applications

- Cryptographic hardware module
- Digital signal processing
- Embedded educational platform
- Embedded industrial OEM platform
- Embedded system design
- Emulation platforms
- FPGA graphics
- Image processing
- IP (intellectual property) cores
- Low-power design
- Parallel processing
- Rapid prototyping
- Reconfigurable computing
- System-on-Chip (SoC) development

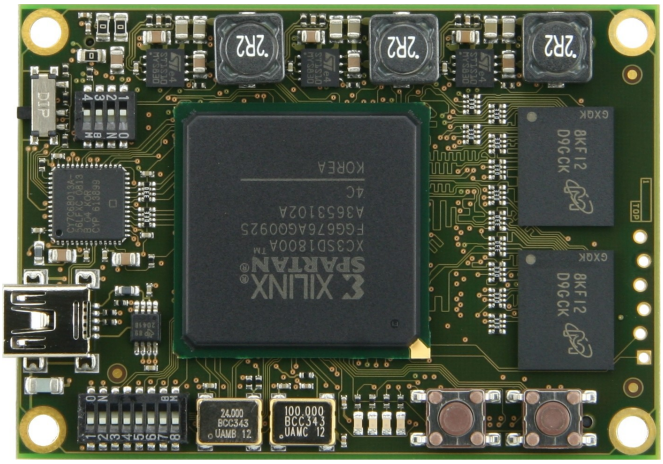

Figure 2: TE0320, top view.

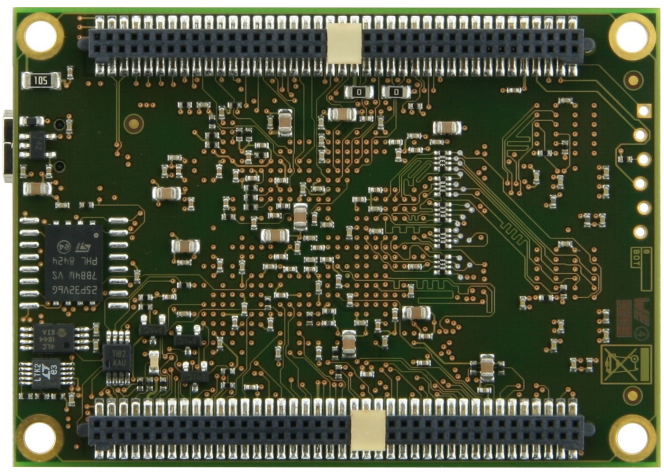

Figure 1: TE0320, bottom view.

Key Features

- Industrial-grade **Xilinx Spartan-3A DSP** FPGA module (1800 k gates or 3400 k gates)
- USB 2.0 (**Hi-Speed USB**) interface with a signalling bit rate of up to 480 Mbit/s
- 32-bit wide 1 Gbit **DDR SDRAM**
- FPGA configuration through:
  - B2B connector
  - JTAG port
  - SPI Flash memory
- Large **SPI Flash** memory (for configuration and operation) accessible through:
  - B2B connector (SPI direct)
  - FPGA
  - JTAG port (SPI indirect)
  - USB bus (Firmware Upgrade Tool)
- On-board 100 MHz oscillator for high performance
- On-board 24 MHz oscillator available to user
- 3 on-board high-power, high-efficiency, switch-mode DC-DC converters capable of 3 A each
- Power supply range: 4.0 - 7.0 V
- Power supply via USB or B2B (carrier board)
- 4 LEDs, 2 push buttons, 8 DIP switches.
- Plug-on module with 2 female 1.27 mm pitch header connectors
- 109 FPGA I/O pins (+ 10 dual-purpose pins) available on B2B connectors
- Evenly spread supply pins for good signal integrity
- Assembly options for cost or performance optimization available on request

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1 Block Diagram

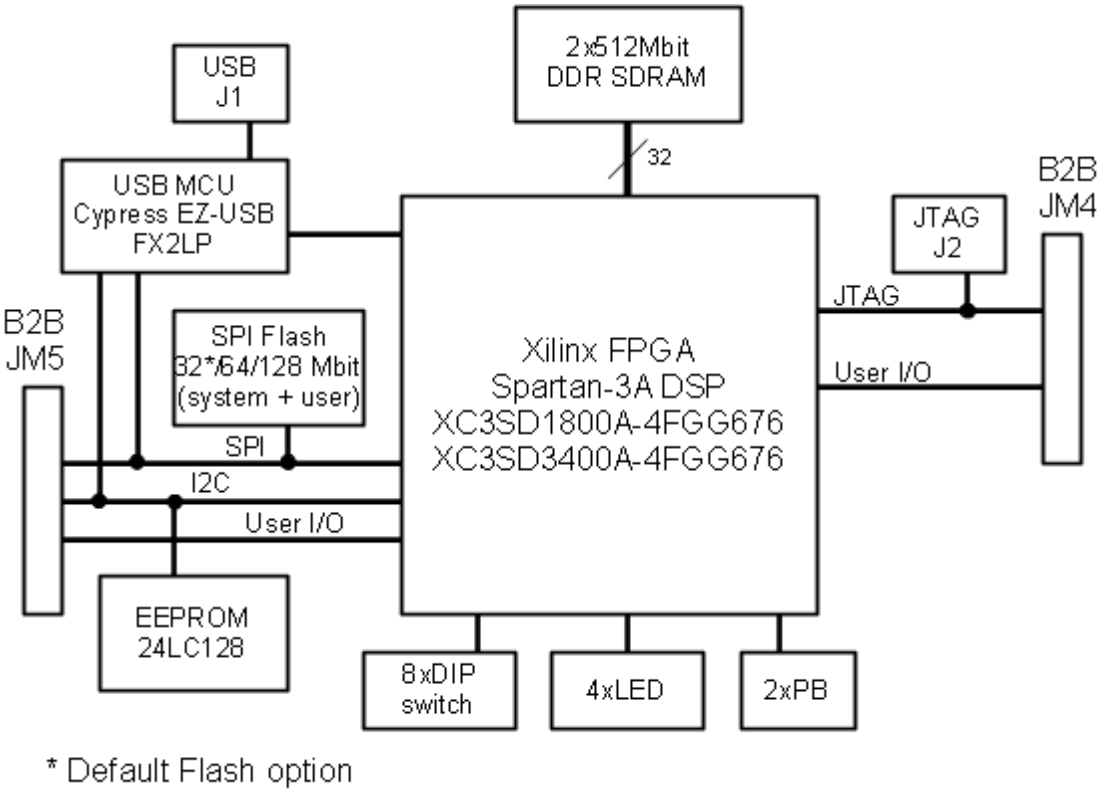


Figure 3: TE0320 block diagram

2 Module options

FPGA options

Module can be ordered with Spartan-3A DSP XC3SD1800A or XC3SD3400A chip.

Flash options

Module can be ordered with 32, 64 or 128 Mbit SPI Flash chip.

Temperature grade options

Module can be ordered in commercial or in extended (from -25 C° to +85 C°) temperature grade.

3 Specifications

- FPGA: Xilinx Spartan-3A DSP:
  - XC3SD1800A-4FGG676C, XC3SD1800A-4FGG676I or
  - XC3SD3400A-4FGG676C, XC3SD3400A-4FGG676I
- Cypress EZ-USB FX2LP™ USB microcontroller, high speed USB peripheral controller
  - CY7C68013A-56LTXC (commercial grade) or
  - CY7C68013A-56LTXI (industrial grade)
- Numonyx M25P32[1] / M25P64 / M25P128:
  low voltage, serial Flash memory with 75 MHz SPI bus interface
- 2 × 16-bit data-bus 512 Mbit DDR SDRAM (connected in parallel as a virtual 1 × 32-bit data-bus DDR SDRAM)
- Microchip Technology 24LC128I-ST
  128 kbit I2C CMOS serial EEPROM
- 3 × STMicroelectronics ST1S10:
  3 A, 900 kHz, monolithic synchronous step-down regulator
  3 A for each power rail: 1.2 V, 2.5 V, 3.3 V
- Texas Instruments TPS3705–33DGN
  processor supervisory circuits with power-fail and watchdog
- 100 MHz oscillator (system + user)
- 24 MHz oscillator (system + user)
- 2 × CviLux CBC1-80-2-M110-2P
  1.27 mm (50 mil = .050") pitch 80-pin double row socket (female) header board-to-board (B2B) connectors with key and pegs
- 109 FPGA IO Pins routed to the B2B connector
- 6-pin JTAG header
- 1 × USB mini-B receptacle (device)
- 1 × LED (system)
- 4 × LED (user)
- 2 × push button (user)
- 4 × DIP switches (system)
- 1 × slide switch (system)
- 8 × DIP switch (user)

1 Default module configuration contain 32 MBit Flash

4 Board Dimensions

TE0320 measures 68.0 × 48.0 mm.

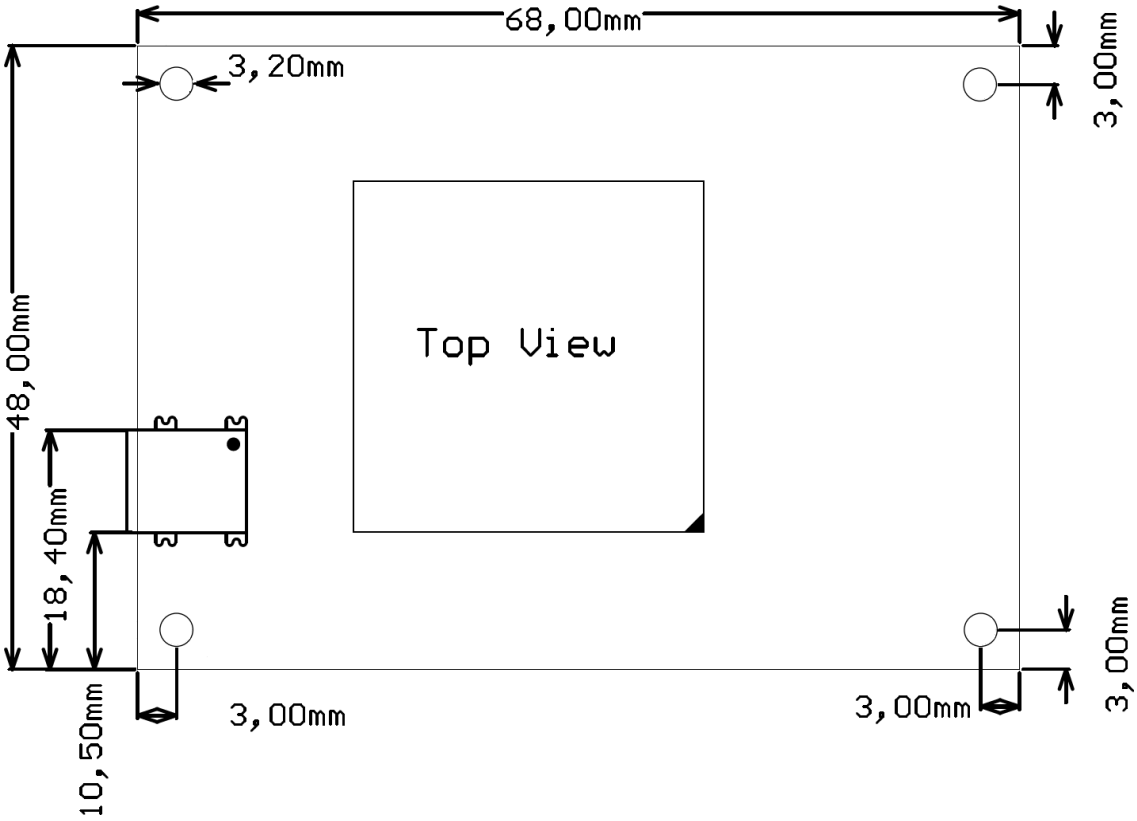


Figure 4: dimensional drawing.

TE0320 can reach a minimum vertical height of about 6 mm if push buttons and USB receptacle are not assembled.

Two mated standard TE0320 connectors have a nominal mated height of 6.0 mm. Processing conditions and solder paste thickness affects such height, resulting in an effective mating heights of 7.0 mm. Therefore the recommended stand-off (distance bolts) height is 7 mm.

TE0320 has 4 mounting holes, one in each corner. The module can be fixed by screwing M3 screws (ISO 262) into a carrier board through those mounting holes.

TE0320 weighs about 25 g.

5 Power Supply

5.1 Power Supply Range

The power supply range of TE0320 is 4.0 V to 7.0 V.

5.2 Power Supply Sources

TE0320 can be power supplied in two ways:

- through USB connector J1,
- through B2B connector JM5 (pins 1 to 4).

The power supply source is determined by assembly option. See Figure 5.

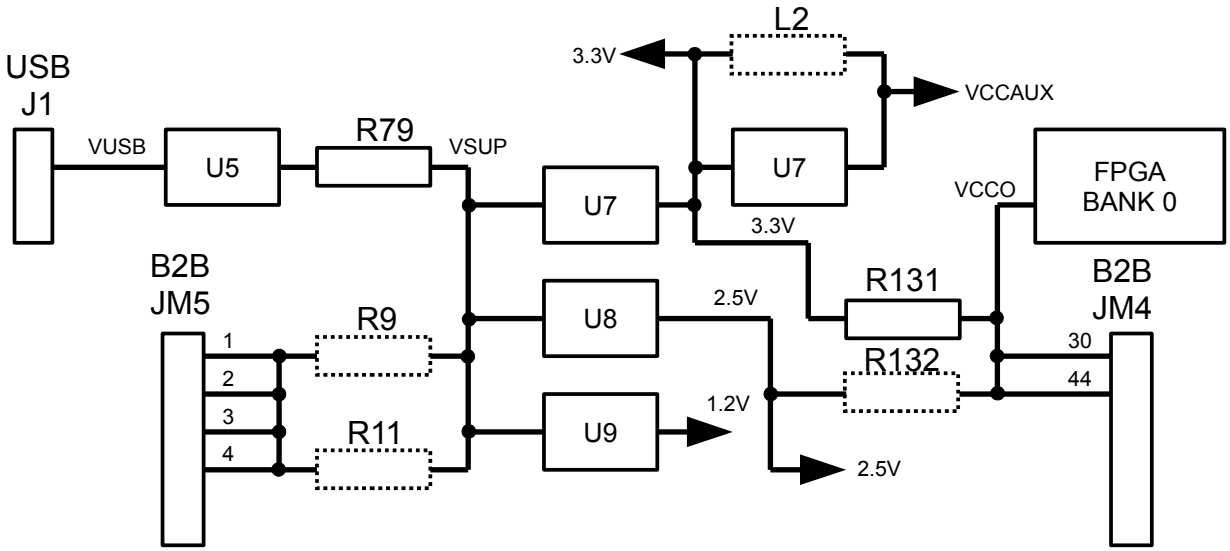


Figure 5: Power supply options diagram

If resistors R9 and R11 are populated and R12 is not populated, then TE0320 is power supplied through JM5 (B2B connector).

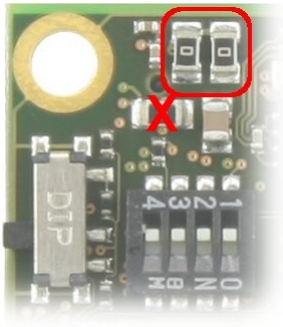


Figure 6: assembly combination for power supply through JM5.

If resistors R9 and R11 are not populated and R12 is populated, then TE0320 is power supplied through J1 (USB bus).

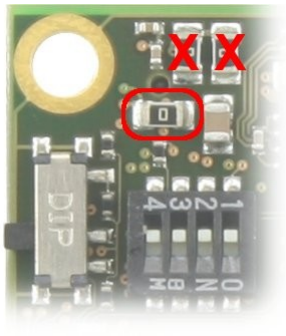


Figure 7: assembly combination for power supply through J1.

Any other assembly combination of R9, R11 and R12 is not allowed.

5.3 On-Board Power Rails

According to the Xilinx Spartan-3A DSP literature, there are the following power supply pin types:

- V_{CCAUX}: dedicated auxiliary power supply pins
- V_{CCINT}: dedicated internal core logic power supply pins
- V_{CCO}: supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards.

TE0320 has the following power rails on-board:

- Vsup

  It is the main internal power rail irrespective of the external power supply. It is supplied by either Vb2b or Vusb. It manages power distribution, conversion and supervision. It is routed also to connector JM5 as a user power supply output.
- Vb2b

  It is the main power rail when the module is supplied from B2B connector JM5.
- Vusb

  It is the main power rail when the module is supplied from USB mini-B connector J1. The maximum current than can be provided to J1 is determined by the USB power source.
- 3.3V

  It is converted from Vsup by a step-down DC/DC converter and can provide up to 3.0 A to the module and connectors JM4 and JM5.
- 2.5V

  It is converted from Vsup by a step-down DC/DC converter and can provide up to 3.0 A to the DDR SDRAM and connectors JM5.
- 1.2V

  It is converted from Vsup by a step-down DC/DC converter and can provide up to 3.0 A to the V_{CCINT} power supply pins and connectors JM5.
- VCCAUX

Here there are two assembly options:

(a) if inductor L2 is not populated and the low-noise low drop-out regulator U6 is populated, VCCAUX power rail is supplied with its nominal voltage of 2.5 V. This is the recommended option for noise-sensitive circuitry such as clocking and timing infrastructures.

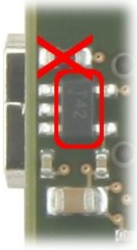


Figure 8: assembly option for VCCAUX = 2.5 V (bottom view).

(b) if the ferrite bead L2 is populated and U6 is not populated, the 3.3V power rail is simply filtered to generate VCCAUX power rail. This is the recommended option for cost-sensitive applications. In this case

(b.1) ensure the noise level on power rail VCCUAX is suitable to your application;

(b.2) avoid the connection of noise sources to power rail VCCUAX.

Figure 9: assembly option for VCCAUX = 3.3 V (bottom view).

Any other assembly combination of L2 and U6 is not allowed.

- VCCCIO0

VCCCIO0 supplies V_{CCO} to FPGA bank 0. The following assembly options are possible:

(a) if both resistors R131 and R132 are not populated, VCCCIO0 power can be supplied through pins 30 and 44 of B2B connector JM4.

Figure 10: assembly option for VCCAUX = off (bottom view).

Pins 30 and 44 of JM4 are power supply **inputs** in this case.

(b) if resistor R131 is not populated and R132 is populated, VCCCIO0 power rail is set to power rail 2.5V (nominal voltage = 2.5 V).

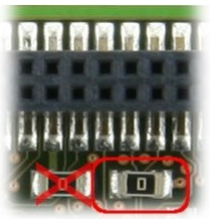


Figure 11: assembly option for VCCAUX = 2.5 V (bottom view).

Pins 30 and 44 of JM4 are power supply **outputs** in this case.

(c) if resistor R131 is populated and R132 is not populated, VCCCIO0 power rail is set to power rail 3.3V (nominal voltage = 3.3 V). This is the default.

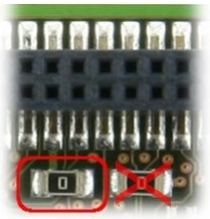


Figure 12: assembly option for VCCCIO0 = 3.3 V (bottom view).

Pins 30 and 44 of JM4 are power supply **outputs** in this case.

Assembly option where both R131 and R132 are populated is not allowed.

1.2 V, 2.5 V and 3.3 V voltage rails are provided by corresponding step-down regulator DC/DC converters, each one capable of providing up to 3 A of output current. These three regulators are synchronized to switch with 120° phase lag, to improve EMC, and to reduce input ripple. The synchronization circuit can be omitted in cost sensitive applications (please contact Trenz Electronic).

Power supply inputs and outputs are made available at B2B connectors JM4 and JM5 for user applications.

Each pin of B2B connectors JM4 and JM5 is capable of a maximum current of 1.0 A.

power-rail name	nominal voltage (V)	maximum current (A)	power source	system supply	user supply
Vb2b	4.0 to 7.0	4.0 (4 pin × 1.0 A/pin)	JM5	module	-
Vusb	5.0	0.5	J1	module	-
Vsup	4.0 to 7.0	< 0.5	Vusb	3 × DC/DC DC/DC sync power-fail	JM5 (≤1.0 A)
		< 4	Vb2b		
3.3V	3.3	3.0	Vsup ► DC/DC	module	JM4 (≤1.0 A) JM5 (≤1.0 A)
2.5V	2.5	3.0	Vsup ► DC/DC	DDR SDRAM	JM5 (≤1.0 A)
1.2V	1.2	3.0	Vsup ► DC/DC	VCCINT	JM5 (≤1.0 A)
VCCAUX	2.5	0.3	3.3V ► LDO	VCCAUX	JM4 (≤1.0 A)
	3.3	< 3.0	3.3V		
VCCCIO0	2.5	< 3.0	2.5V	VCCO (bank 0)	JM4 (≤1.0 A)
	3.3	< 3.0	3.3V		JM4 (≤1.0 A)
	1.10 to 3.60	2.0 (2 pin × 1.0 A/pin)	JM4 (30 + 44)		JM4 (30 / 44)

Table 1: On-board power rails summary.

5.4 Power Supervision

5.4.1 Power-on Reset

During power-on, the /RESET line is first asserted. Thereafter, the supply voltage supervisor monitors the power supply rail 3.3V and keeps the /RESET line active (low) as long as the rail remains below the threshold voltage (2.93 V). An internal timer delays the return of the /RESET line to the inactive state (high) to ensure proper system reset. The delay time of 200 ms starts after the rail has risen above the threshold voltage.

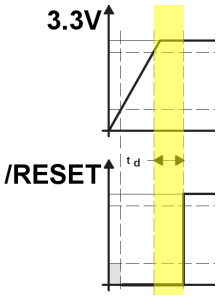


Figure 13: Power-on reset with fixed delay time of 200 ms.

After this delay, the /RESET line is reset high and the FPGA configuration can

start. When the rail voltage drops below the threshold voltage, the /RESET line becomes active (low) again.

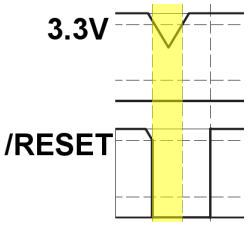


Figure 14: Reset assertion on power drop with fixed delay time of 200 ms.

5.4.2 Power Fail

TE0320 integrates a power-fail comparator which can be used for low-battery detection, power-fail warning, or for monitoring Vsup power rail.

An additional power-fail circuit can be used, to monitor the input voltage. At 4.4V, a power-fail signal (/PFO) is sent to the FPGA. Should you wish or need another threshold voltage, please contact Trenz Electronic.

6 Inputs and Outputs

6.1 Board-to-Board Connectors

The module has two B2B (board-to-board) connectors (JM4 and JM5) with the following features:

- gender: female
- overall number of contacts: 160
- contacts per connector: 80
- rows per connector: 2
- pitch: 1.27 mm = 50 mil = .050"

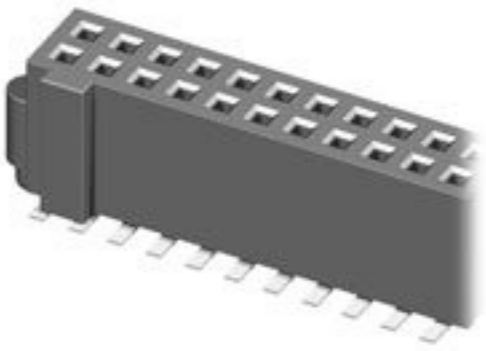


Figure 15: Board to board connector assembled on the TE0320.

Trenz Electronic recommends to mate the standard B2B connectors with the following ones:

- 2 x W+P 6110-080-00-10-PPTR
  1.27 mm (50 mil = .050") pitch 80-pin double row boxed plug (male) header board-to-board (B2B) connectors.

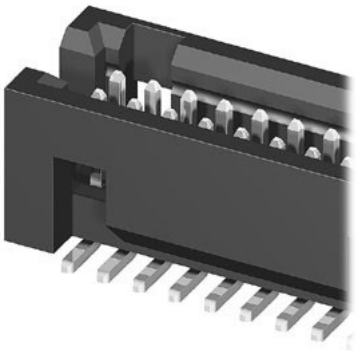


Figure 16: Close-up of the recommended mating B2B connector.

This connector couple offers the following two advantages:

- the module is protected against polarity inversion;
- the connection presents a mechanical resistance sufficient for most applications.

Ordering codes for connectors JM4 / JM5 and their mating connectors are given

in Table 2.

	gender	W+P	Trenz Electronic
B2B connector JM4 + JM5	female	6060-080-46-00-10-10-PPTR	23758
B2B mating connector	male	6110-080-00-10-PPTR	23749

Table 2: Ordering codes of recommended B2B connectors.

The mating height of connectors 6060-080-46-00-10-10-PPTR and 6110-080-00-10-PPTR is 6mm.

Connectors JM4 and JM5 can mate also with any 1.27 mm (50 mil = .050") pitch male header connectors with up to 2 × 40 pins. Figure 17.

Figure 17: sample matching header connector.

Connectors JM4 and JM5 and are placed on the bottom side of the module as shown in Figure 18.

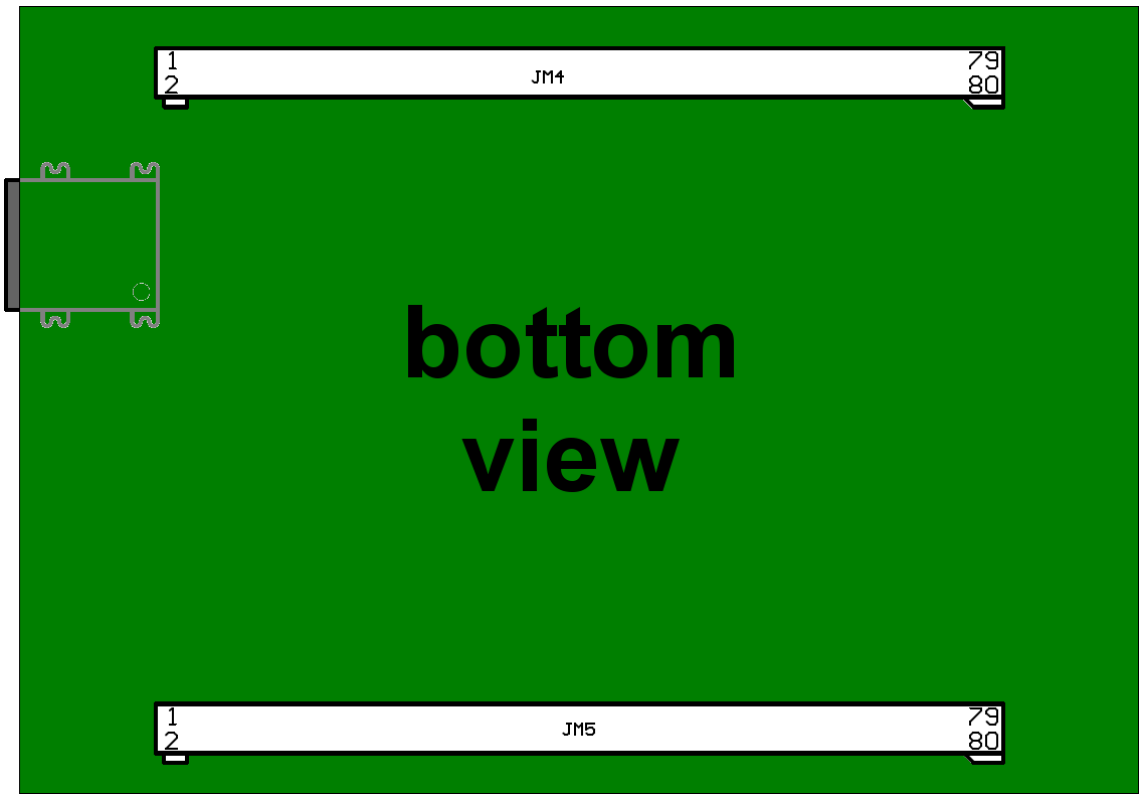


Figure 18: female header connectors JM4 and JM5 (bottom view).

6.2 USB Interface

USB communication can be performed in one of the following two ways:

- through a USB connector
- through USB lines at one B2B connector.

Only one connection type at one time is allowed.

6.2.1 USB Connector

TE0320 is provided with a USB mini-B receptacle (device) connector J1 on the top side.

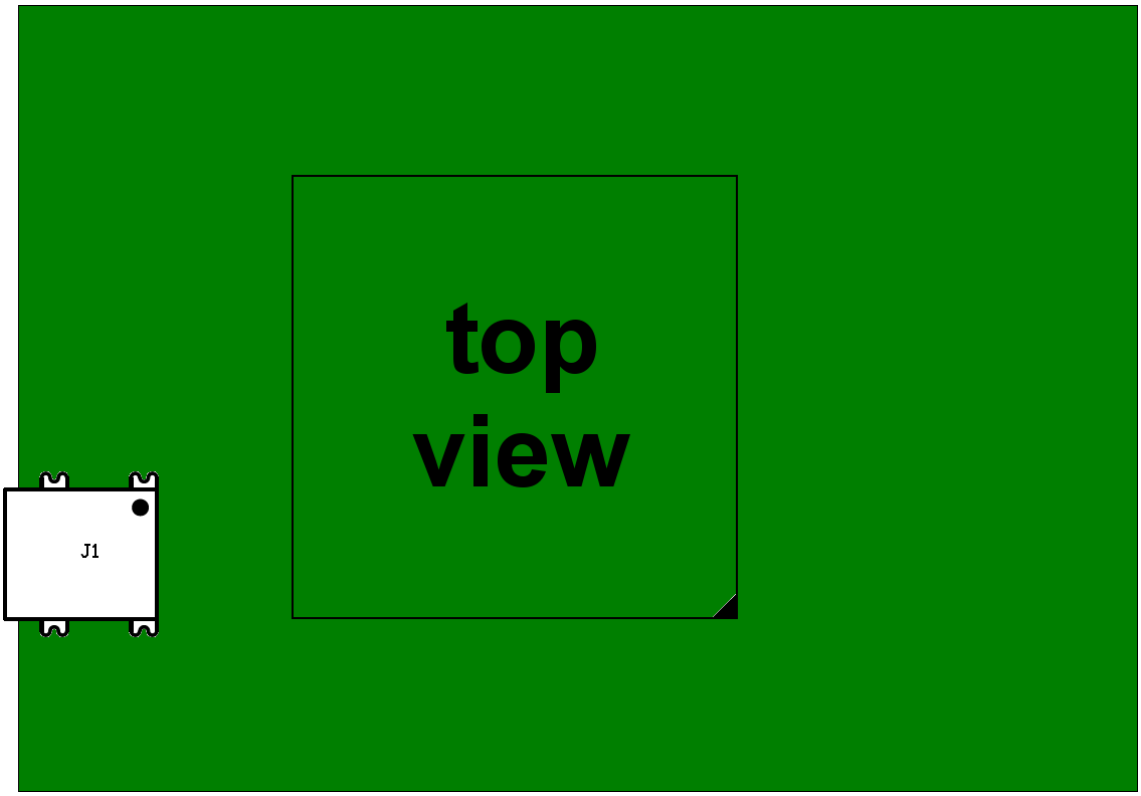


Figure 19: USB connector (top view).

Figure 20: USB mini-B receptacle (device) connector.

Figure 21 shows a sample USB connection between computer and TE0320 for both configuration and operation. The USB cable provides for

- Power supply.
- Configuration by means of the Firmware Upgrade Tool (FUT), recommended for field upgrades. Please use a dedicated JTAG Adapter during development.
- Data communication channel during operation.

Figure 21: sample USB connection (TE0320 side).

In order to minimize the stub on USB lines and improve communication quality, the connection to both USB pins of B2B connector JM4 can be interrupted by removing resistors R3 and R4.

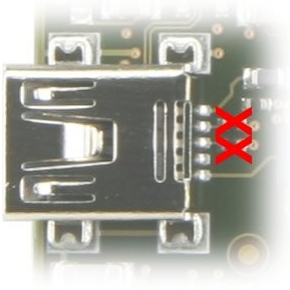


Figure 22: resistors R3 and R4 removed for lower stub on USB lines.

Should you require a module version without connector J1, please contact Trenz Electronic.

6.2.2 USB Pins

USB communication can be performed over 2 pins of B2B connector JM4 as

detailed in Table 3. Ensure resistors R3 and R4 are populated to connect USB B2B pins B2B_D_P and B2B_D_P to USB lines D_P and D_P respectively.

pin number	pin name	signal name	description
4	B2B_D_P	D_P	USB data + (D+)
6	B2B_D_N	D_N	USB data - (D-)

Table 3: USB pins at B2B connector JM4.

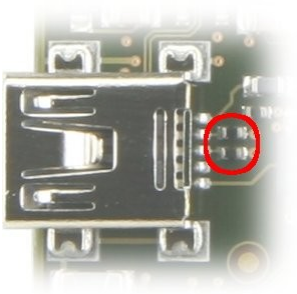


Figure 23: Resistors R3 and R4 required for USB communication over B2B connector JM4.

6.3 JTAG Interface

6.3.1 JTAG connector J2

JTAG signals are available on the gender-inverted standard 6-pin JTAG header connector J2 as shown in Figure 24.

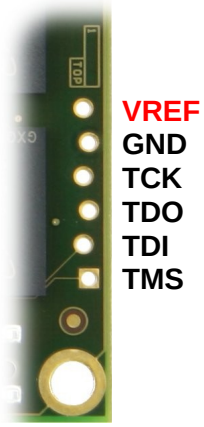


Figure 24: JTAG connector J2.

To connect your computer to JTAG connector J2 you typically need

- a JTAG cable with standard 6-pin JTAG female header;
- a 2.54 mm pitch 1 × 6 pin gender changer header.

Some examples of JTAG cable set are listed in Table 4.

JTAG cable	flying leads	software	gender changer
Xilinx Platform Cable USB	included	Xilinx iMPACT	1 × 6 pin
Digilent XUP USB-JTAG Programming Cable	XUP Fly Wire Assembly	Xilinx iMPACT	1 × 6 pin

Digilent JTAG-USB Full Speed Module	not needed	Digilent Adept 2.0	1 × 6 pin

Table 4: some examples of JTAG cable set.

Figure 25 shows a standard 6-pin JTAG female header, in this case flying leads, with a gender changer header.

Figure 26 shows how a JTAG cable, in this case a Xilinx Platform Cable USB with flying leads and gender changer, is connected to a TE0320.

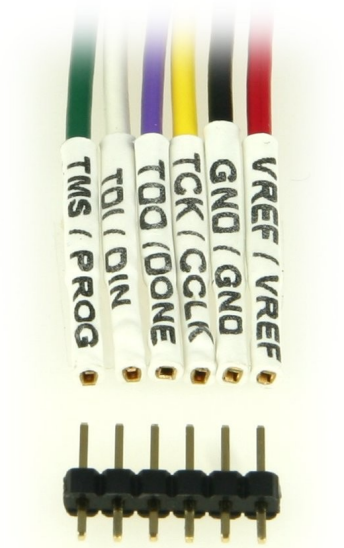


Figure 25: standard 6-pin JTAG female header with gender changer.

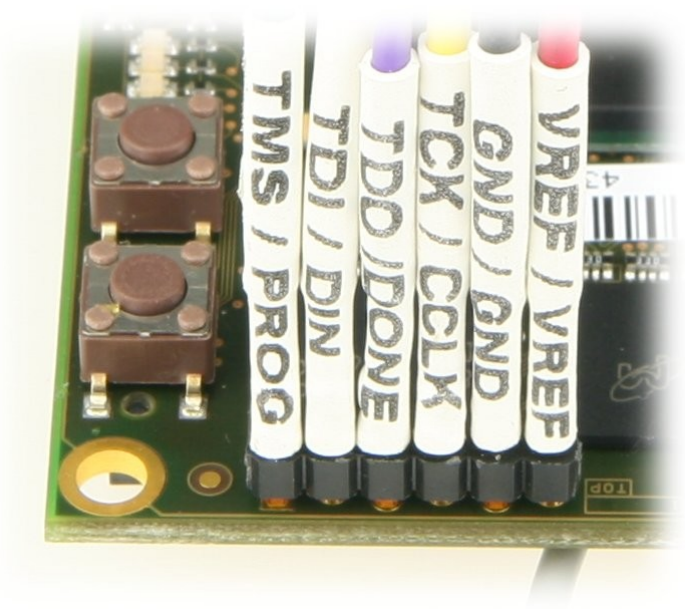


Figure 26: sample JTAG cable connection ((TE0320 side).

Figure 27 shows a recommended set-up for TE0320 configuration and operation. The USB cable provides for power supply and data communication channel. The JTAG is ideal for quick configuration and effective debugging.

Figure 27: recommended TE0320 set-up.

6.3.2 JTAG lines at B2B connector JM4

JTAG signal lines are also available at B2B connector JM4. See Table 40 for additional information on these signals.

6.4 I2C bus

TE0320 has a flexible I2C bus on-board as outlined in Figure 28.

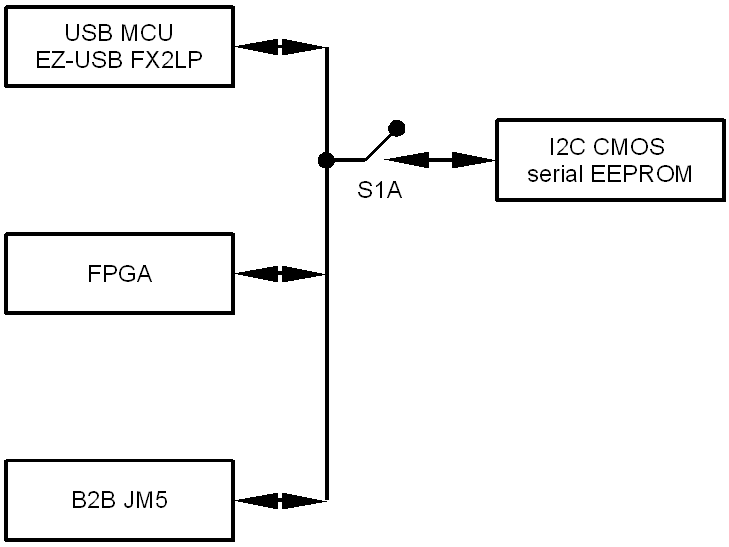


Figure 28: I2C bus topology.

The I2C signals on the TE0320 are listed and described in Table 5.

name	definition	description
SDA	serial data	This is a bidirectional pin used to transfer addresses and data into and out of a device.
SCL	serial clock	This signal is used to synchronize the data transfer to and from a device.

Table 5: I2C signals summary.

The I2C bus is typically used by the USB microcontroller to write USB firmware to the serial EEPROM. In this case,

- the I2C port of the FPGA must be set in slave mode (SCL pin as input),
- the device attached to the I2C port of B2B JM5 connector must be set to slave mode.

The USB microcontroller can operate just in I2C master mode (default operation). If the user wants to set another device attached to the I2C bus as master device, the USB microcontroller shall three-state (Z = high impedance) its SCL and SDA pins.

If the FPGA is set to I2C master mode, it can write to or read from serial EEPROM (always slave mode) and B2B connector JM5 (attached device set to slave mode).

If the device attached to the I2C port of B2B JM5 connector is set to master mode, it can write to or read from serial EEPROM (always slave mode) and FPGA I2C port (set to slave mode).

Possible I2C operation modes are summarized in Table 6.

core	EZ-USB FX2LP	FPGA (SDA = I/O)	B2B JM5	serial EEPROM
default	**master**	slave SCL = I	slave	slave
custom	inactive SCL = SDA = Z	**master** SCL = O	slave	slave
custom	inactive SCL = SDA = Z	slave SCL = I	**master**	slave

Table 6: I2C bus modes summary.

TE0320 reference design includes an HDL core managing the fast mode (400 kHz) I2C communication between the Xilinx MicroBlaze embedded soft-processor and the EZ-USB FX2LP USB microcontroller.

I2C pins on B2B connector JM5 cannot be used as GPIOs (general purpose I/Os),
as these bus signals are pulled up to 3.3V.

6.5 SPI bus

TE0320 has a flexible SPI bus on-board as outlined in Figure 29.

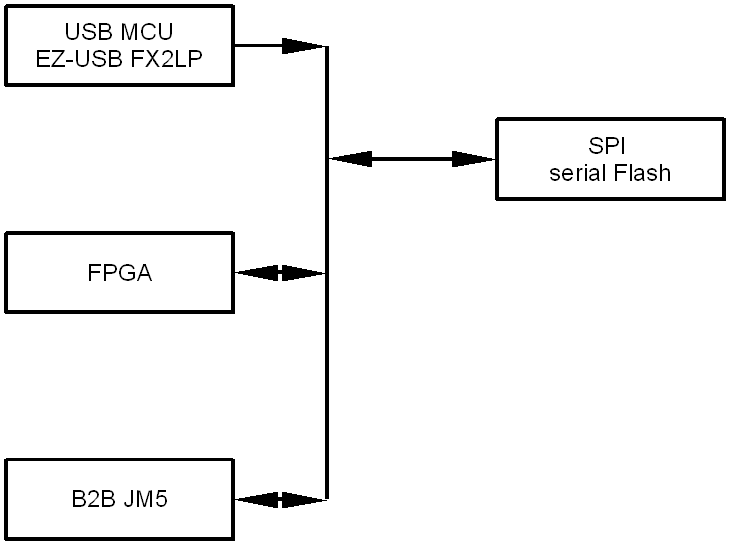


Figure 29: SPI bus topology.

SPI signals on the TE0320 are listed and described in Table 7.

name	definition	description
SPI_Q	serial data output	This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of SPI_/C.
SPI_D	serial data input	This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of SPI_/C
SPI_/C	serial clock	This input signal provides the timing of the serial interface. Instructions, addresses, or data present at SPI_D are latched on the rising edge of SPI_/C. Data on SPI_Q changes after the falling edge of SPI_/C.
SPI_/S	chip select	When this input signal is **high,** the device is **disabled** and SPI_Q is at high impedance (Z).
		When this input signal is **low**, the device is **enabled.**
		After power-up, a falling edge on SPI_/S is required prior to the start of any instruction to the Flash memory.

Table 7: SPI signals summary.

SPI signal pin-out of the TE0320 is summarized in Table 8.

name	FPGA ball	JM5 pin
SPI_Q	AF24	18
SPI_D	AB15	12
SPI_/C	AE24	22
SPI_/S	AA7	20

Table 8: SPI pin-out summary.

SPI pins on B2B connector JM5 cannot be used as GPIOs (general purpose I/Os).

The SPI bus can be used during configuration and operation in a plurality of ways as summarized respectively in Table 9 and Table 10. Any other usage of the SPI bus is neither supported nor recommended.

6.5.1 SPI bus for configuration

The SPI bus is used for configuration in two ways by default:

(d) EZ-USB ► Flash
the USB microcontroller (master) writes the PROM file (containing the FPGA configuration bitstream) to the SPI serial Flash memory (slave)

(e) FPGA ◄ Flash
the FPGA (master) configures itself in Master SPI mode from the SPI serial Flash memory (slave).

In case (a), the FPGA shall be turned off to release its shared SPI pins.

In case (b), the USB microcontroller shall three-state (Z = high impedance) its shared SPI pins.

description	usage	EZ-USB FX2LP	FPGA	B2B JM5	serial Flash
EZ-USB ► Flash	FUT API	**master**	off (S2 = FX2PON, FX2_PS_EN = 0)	deselected	slave
FPGA ◄ Flash	FUT API	inactive SPI_* = Z	**master** (SPI_/S = 1)	deselected	slave
B2B JM5 ► Flash	custom	inactive SPI_* = Z	off (S2 = FX2PON, FX2_PS_EN = 0)	**master** (SPI_/S = 0)	slave

Table 9: SPI bus modes for configuration.

The PROM file (containing the FPGA configuration bitstream) can be written to the SPI serial Flash memory (slave) also through the SPI pins of B2B connector JM5 (attached device set to master mode). In this case, the FPGA shall be turned off or three-stated to release its shared SPI pins and the USB microcontroller shall three-state (Z = high impedance) its shared SPI pins.

6.5.2 SPI bus for operation

A plurality of usage combinations of the SPI bus during operation is made available to the user as suggested in Table 10.

description	usage	EZ-USB FX2LP	FPGA	B2B JM5	serial Flash
EZ-USB ◄► Flash	custom	**master**	off (S2 = FX2PON, FX2_PS_EN = 0)	deselected	slave
FPGA ◄► Flash	custom	inactive SPI_* = Z	**master** (SPI_/S = 1)	deselected	slave
B2B JM5 ◄► Flash	custom	inactive SPI_* = Z	off (S2 = FX2PON, FX2_PS_EN = 0)	**master** (SPI_/S = 0)	slave
EZ-USB ◄► B2B JM5	custom	**master** SPI_/S = 1	off (S2 = FX2PON, FX2_PS_EN = 0)	slave	deselected
EZ-USB ◄► B2B JM5	custom	slave SPI_/C = Z	off (S2 = FX2PON, FX2_PS_EN = 0)	**master** (SPI_/S = 1)	deselected

Table 10: SPI bus modes for operation.

Other combinations of master and slave units are neither supported nor recommended.

6.6 LEDs

6.6.1 System LED D1

LED D1 is connected to the DONE pin. The DONE pin is powered by the VCCAUX supply.

The FPGA actively drives the DONE pin Low during configuration. Thus, LED D1 is unconditionally turned off during configuration.

To have LED D1 turned on or off after successful configuration, please see paragraph 11 Recommended Design Tools Settings.

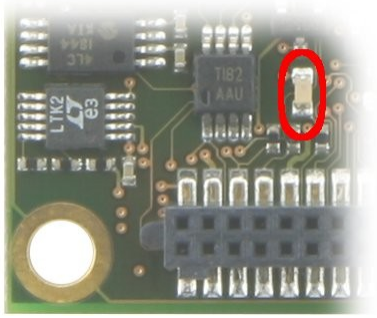


Figure 30: DONE LED D1 (bottom side).

6.6.2 User LEDs D[5:8]

TE0320 is provided with 4 user LEDs. A LED is lit when the corresponding signal listed in Table 11 is set high (logical 1).

LED	signal	FPGA ball	FPGA pin	bank
D5	UL1	R20	IO_L22N_1	1
D6	UL2	V23	IO_L21P_1	1
D7	UL3	R19	IO_L22P_1	1
D8	UL4	U24	IO_L23N_1 VREF_1	1

Table 11: user LEDs signal details..

6.7 Push-Buttons S[3:4]

TE0320 is provided with 2 user buttons. A signal listed in Table 12 is set low (logical 0) when a push button is pressed, and vice-versa.

switch	signal	FPGA ball	FPGA pin	bank	default input	input when pressed
S3	PB1	U23	IO_L23P_1	1	logical 1	logical 0
S4	PB2	R22	IO_L25N_1	1	logical 1	logical 0

Table 12: user push-buttons signal details.

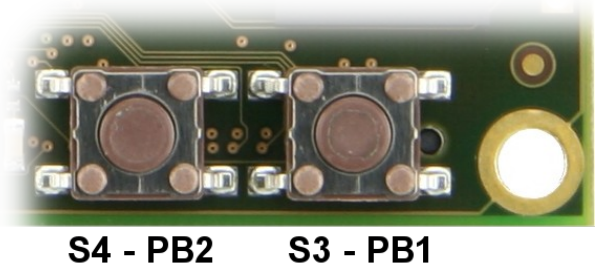


Figure 31: push buttons PB1 and PB2.

Warning! on some boards, PB1 and PB2 labels might be exchanged. Please take Figure 31 as reference.

6.8 Switches

TE0320 is provided with the following slide switches:

- S1: 4 x DIP slide switches (system)
- S2: 1 x slide switch (system)
- S5: 8 × DIP slide switches (user)

6.8.1 DIP Slide Switches S1[A:D]

TE0320 is provided with 4 system DIP slide switches as shown in Figure 32: S1A, S1B, S1C, S1D.

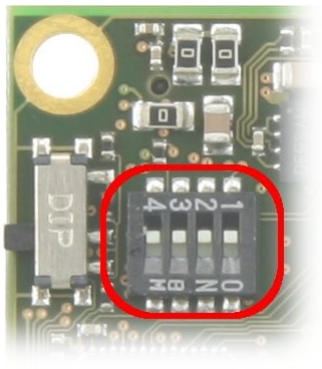


Figure 32: DIP slide switches S1[A:D].

Please note the 4 switch labels are on one side and the <ON> label is on the opposite side.

DIP slide switches S1[A:D] condition the value of some system signals as described in Table 13.

switch	S1 label	signal name	<OFF>	<ON>
S1A	1	EEPROM serial data	the USB microcontroller CANNOT read / write the serial EEPROM	the USB microcontroller can read / write the serial EEPROM
S1B	2	M2	mode pin M2 = 1	M2 = 0
S1C	3	M1	mode pin M1 = 1	M1 = 0
S1D	4	/MR (master reset)	module reset	module running

Table 13: S1X settings description.

DIP slide switches S1A is ON by default, to allow the USB microcontroller to read the serial EEPROM and enumerate as a custom/specific USB device. When DIP slide switches S1A is ON, the USB microcontroller can (re)write the serial EEPROM to, for example, store a (new) custom/specific firmware. When DIP slide switch is OFF, the USB microcontroller cannot read the serial EEPROM and enumerates as a generic USB device.

6.8.2 Slide Switch S2

TE0320 is provided with a slide switch S2.

Figure 33: Slide switch S2 (angle view).

Slide switch S2 conditions the value of signal PS_EN. Signal PS_EN enables (high) or disables (low) power rails 2.5V and 1.2V. According to the corresponding assembly option, power rail VCCCIO0 can depend or not on the 2.5V power rail. Power-rail 3.3V is not controlled by signal PS_EN and is unconditionally enabled. Table 14 summarizes all switching options implied by slide switch S2 under the standard assembly option.

power rail	S2= PON	S2 = FX2 PON FX2_PS_EN = 1	S2 = FX2 PON FX2_PS_EN = 0
2.5V	on	on	off
1.2V	on	on	off
VCCCIO0 (= 2.5V)	on	on	off
VCCCIO0 (= 3.3V)	on	on	on

Table 14: Slide switch S2 settings overview.

6.8.2.1 Slide Switch S2 = PON

When slide switch S2 is in the right position (PON = power rails unconditionally on), signal PS_EN is set to power rail 3.3V. Thus power rails 2.5V and 1.2V are unconditionally enabled.

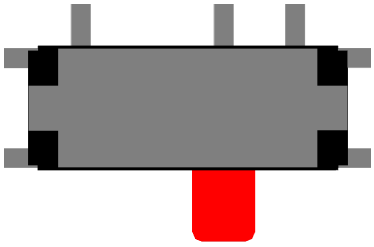


Figure 34: S2 on position PON.

6.8.2.2 Slide Switch S2 = FX2 PON

When slide switch S2 is in the left position (FX2 PON = power rails conditionally on depending on signal FX2_PS_EN), signal PS_EN is set to signal FX2_PS_EN driven by the EZ-USB FX2LP USB microcontroller under user control.

When the EZ-USB FX2LP USB microcontroller sets signal FX2_PS_EN (high), power rails 2.5V and 1.2V are enabled. This setting can be useful for dynamic

full power operation.

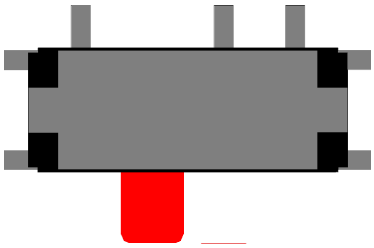


Figure 35: S2 on position FX2 PON (FX2_PS_EN = high).

When the EZ-USB FX2LP USB microcontroller resets signal FX2_PS_EN (low), the following components are switched off:

- FPGA core logic (1.2V)
- DDR SDRAM (2.5V)
- FPGA bank 3 (2.5V)
- VREF (2.5V)
- VCCCIO0 (2.5V) FPGA bank 0

This setting can be useful for dynamic **low power** operation.

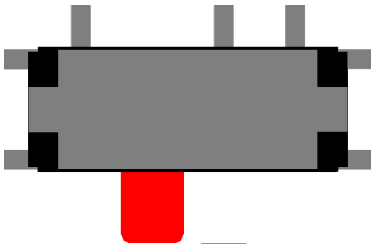


Figure 36: S2 on position FX2 PON (FX2_PS_EN = low).

6.8.2.3 Alternate Assembly Options for Slide Switch S2

Slide switch S2 can be replaced by one resistors in the following cases:

- cost sensitive applications
- applications where just one position of S2 is required
- application where switching of S2 is not allowed.

Assembly option when resistor R17 not populated and R19 populated is equivalent to slide switch S2 permanently set to PON.

Figure 37: assembly option: S2 = PON.

Assembly option when resistor R17 populated and R19 not populated is equivalent to slide switch S2 permanently set to FX2 PON.

Figure 38: Assembly option: S2 = FX2 PON.

Any other assembly options of R17 and R19 are not allowed.

6.8.3 DIP Slide Switches S5[A:H]

TE0320 is provided with 8 user DIP slide switches as shown in Figure 39: S5A to S5H.

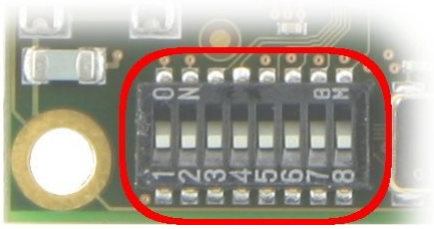


Figure 39: DIP slide switches S5[A:H].

Please note the 8 switch labels are on one side and the <ON> label is on the opposite side.

DIP slide switches S5[A:H] condition the value of some user signals as described in Table 15.

switch	S5 label	signal name	FPGA ball	FPGA pin	FPGA bank
S5A	1	US1	F24	IO_L54N_1	1
S5B	2	US2	E24	IO_L56P_1	1
S5C	3	US3	E26	IO_L60P_1	1
S5D	4	US4	D24	IO_L61N_1	1
S5E	5	US5	D26	IO_L60N_1	1
S5F	6	US6	D25	IO_L61P_1	1
S5G	7	US7	C26	IO_L63P_1 A22	1
S5H	8	US8	C25	IO_L63N_1 A23	1

Table 15: S1X settings description.

A signal listed in Table 15 is set low (logical 0) when a slide switch is set to <ON>, and vice-versa.

6.9 Voltage Reference VREF0

The user can freely set voltage VREF0 through pin 37 of B2B connector JM4. VREF0 is the reference voltage for setting the input switching threshold for certain I/O standards of FPGA bank 0. For more information on reference voltages, please consult Xilinx DS610: Spartan-3A DSP FPGA Family: Complete Data Sheet.

Recommended operating voltage for VREF0 is 0.75 to 1.5 V

Absolute maximum voltage range for VREF0 is -0.5 to VCCCIO+0.5 V.

7 Timing

7.1 Main Clock Oscillator

The module has a main SMD clock oscillator providing a clock source for the FPGA as detailed in Table 3.

signal	FPGA pin	FPGA ball	FPGA bank
MAINCLK	IO_L27N_2 GCLK1	AA14	2

Table 16: Main clock signal details.

Standard frequency is 100 MHz. Should you wish or need another main clock oscillator frequency, please contact Trenz Electronic. The lower the main clock frequency, the lower the module power consumption. Moreover, as the main clock is preferably used as DDR SDRAM clock, a lower clock frequency makes easier for the development tools to meet the timing requirements (particularly for DDR SDRAM).

7.2 24 MHz Clock Oscillator

The module has a 24 MHz SMD clock oscillator providing a clock source for both the EZ-USB FX2LP USB microcontroller (XTALIN) and the FPGA as detailed in Table 17.

signal	FPGA pin	FPGA ball	FPGA bank
24MHZ1	IO_L28N_2 GCLK3	AE14	2

Table 17: 24 MHz clock signal details.

7.3 Interface Clock (IFCLK)

The IFCLK line synchronizes the communication between the EZ-USB FX2LP USB microcontroller and the FPGA as detailed in Table 18.

signal	FPGA pin	FPGA ball	FPGA bank
IFCLK	IO_L31N_1 TRDY1 RHCLK3	P25	1

Table 18: Interface clock signal details.

7.4 Digital Clock Manager (DCM)

The DCMs of the FPGA can be used to synthesize arbitrary clock frequencies from any on-board clock network, differential clock input pair or single-ended clock input. For further reference, please read Xilinx DS485:Digital Clock Manager (DCM) Module and the DCM chapter in Xilinx UG331: Spartan-3 Generation FPGA User Guide.

7.5 Watchdog

TE0320 has a watchdog timer that is periodically triggered by a positive or negative transition of the watchdog input (WDI) signal. When the supervising system fails to retrigger the watchdog circuit within the time-out interval (min 1.1

s, typ 1.6 s, max 2.3 s), the watchdog output becomes active and asserts the master reset (/MR) signal. This event also reinitializes the watchdog timer.

If resistors R135 and R165 are not populated, the watchdog is disabled.

If resistors R135 and R165 are populated, the watchdog can be enabled. In this case there are still two options.

- To enable the watchdog after module power-up, drive the WDI signal to generate a transition (no matter if positive or negative).
- To keep the watchdog disabled, set the WDI FPGA signal output to high-impedance. One way to reach this goal is to leave FPGA pin V24 (FPGA signal IO_L19P_1) undeclared in the user constraints file (UCF) and set the Xilinx Project Navigator options as follows:
project properties > configuration options > unused IOB pins > float.

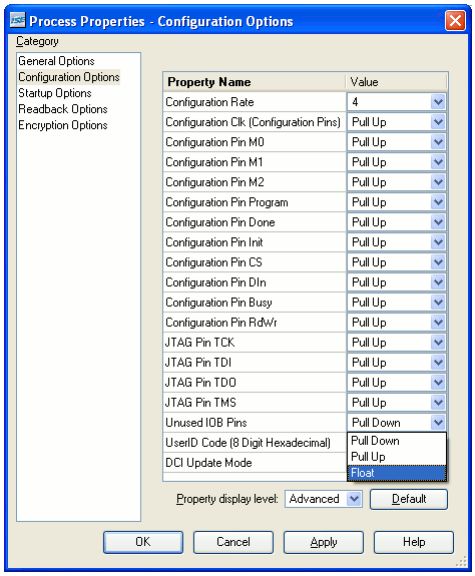


Figure 40: configuration option in Xilinx ISE Project Navigator.

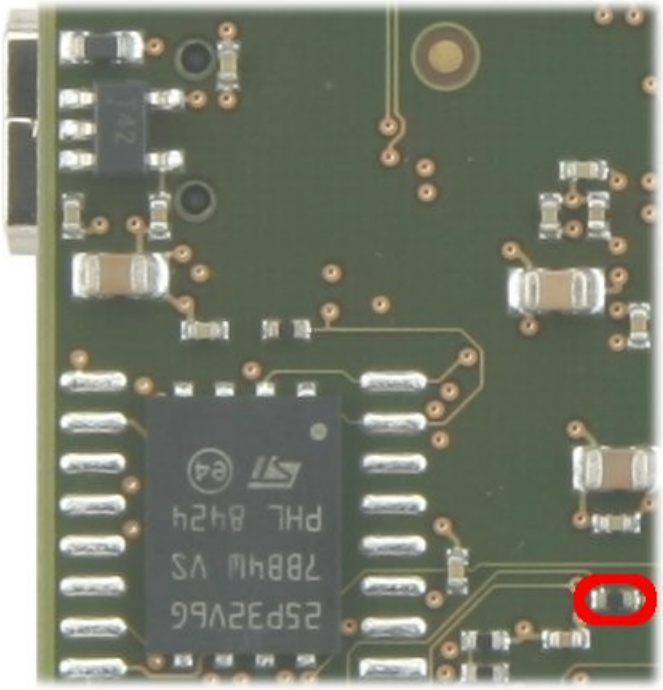


Figure 41: R135 (bottom side).

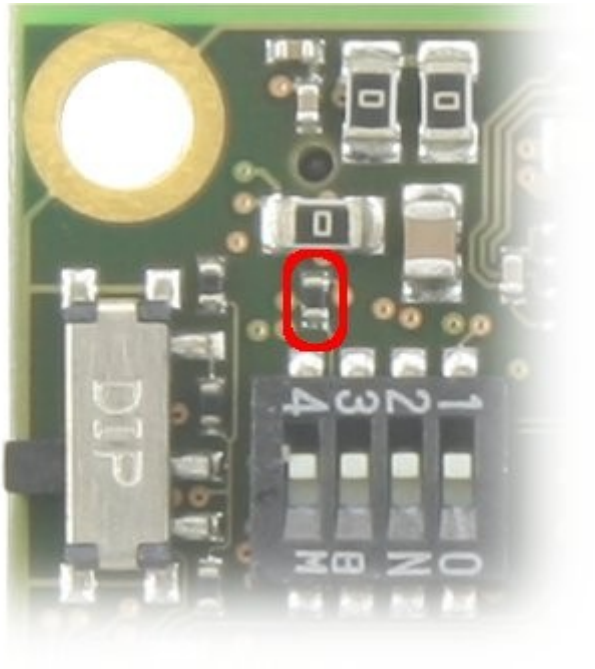


Figure 42: R136 (top side).

Any other combination of resistors R135 and R136 is not supported.

8 Memories

The TE0300 has three on-board memories:

- DDR SDRAM
- SPI Flash
- serial EEPROM

8.1 DDR SDRAM

TE0320 modules have two 512Mb DDR SDRAM components each with a 16-bit data-bus connected in parallel to FPGA bank 3 as a virtual 512Mb DDR SDRAM component with a 32-bit data-bus. Memory available in industrial and commercial temperature grade.

8.2 SPI Flash

TE0320 has an STMicroelectronics M25P32/64/128 (32/64/128-Mbit), low voltage, serial Flash memory with 75 MHz SPI bus interface for configuration and operating storage accessible through USB or SPI. Default module configuration contain 32 Mbit Flash chip M25P32, others available by request.

8.3 Serial EEPROM

TE0300 modules have a Micron Technology 24LC128 128 kbit I2C CMOS Serial EEPROM for EZ-USB FX2 firmware, vendor ID and device ID storage accessible through the EZ-USB FX2 microcontroller.

9 System Requirements

9.1 Power Supply Requirements

TE0320 can be power supplied by one of the following power sources:

- USB bus, 5 V;
- JM5[1:4], 4 V to 7 V power supply (5 V recommended).

System current consumption is design dependent.

USB buses able to supply only 100 mA are not supported.

See paragraph 5.2 Power Supply Sources for additional information on this topic.

9.2 Hardware Design Requirements

PUDC_B (pull-up during configuration, active Low) pin in TE0320 modules is hard-wired high, determining user-I/O pins to float before and during configuration. Turning off pull-up resistors in hot-swap or hot-insertion applications, disables potential current paths to the I/O power rail. However, external pull-up or pull-down resistors may be required on each individual I/O pin depending on the specific application.

9.3 USB Requirements

Recommended USB bus classes are 1.1 and 2.0.

TE0320 can be connected to a USB bus through connector either J1 or JM4[4, 6].

SPI serial Flash memory can be written through the Firmware Upgrade Tool and the API.

Data communication over USB can be implemented through the API.

9.4 JTAG Requirements

TE0320 can be configured and debugged over JTAG through connector either J2 or JM4[74, 76, 78, 80].

See paragraph 6.3 JTAG Interface for additional information on this topic.

9.4.1 Software Requirements

Software requirements depend on the intended design goal.

design goal	ISE WebPACK	EDK
HDL design	•	
MicroBlaze design	•	•
reference design	•	•

Table 19: software requirements chart.

EDK: Xilinx Embedded Development Kit = XPS + SDK;

XPS = Xilinx Platform Studio (for hardware engineers);

SDK: Xilinx Software Development Kit (for software engineers).

Xilinx ISE WebPACK is a **free** development environment featuring

- Xilinx ISE Foundation (device limited)
- Xilinx ISE Simulator (ISim)
- Xilinx PlanAhead

TE0320 reference design requires Xilinx EDK.

Please visit the official Xilinx ISE Design Suite page for latest information about Xilinx design tools.

9.5 Operating System Support

Xilinx ISE Design Suite is supported on both 32-bit and 64 bit versions of both Microsoft Windows and GNU/Linux operating systems. Please consult the Xilinx ISE Design Suite Product Table and Xilinx ISE Design Suite Software Matrix on the official Xilinx ISE Design Suite page for latest information about Xilinx ISE Design Suite operating system support.

TE0320 software package includes EZ-USB FX2LP USB microcontroller device drivers for the 32 bit version of Microsoft Windows operating system.

TE0320 software package includes the Firmware Upgrade Tool for the 32 bit version of Microsoft Windows operating system.

10 Configuration

The Xilinx Spartan-3A DSP FPGA on the TE0320 can be configured in the following ways:

- B2B connector
  - JTAG
  - Slave Parallel (SelectMAP)
  - Slave Parallel
- JTAG port
- SPI Flash memory

For further information on Xilinx Spartan-3A DSP configuration modes, please consult the documentation listed in chapter 17 Related Materials and References.

The SPI Flash memory can be programmed in the following ways:

- B2B connector (SPI direct)
- FPGA
- JTAG (SPI indirect)
- USB bus (Firmware Upgrade Tool)

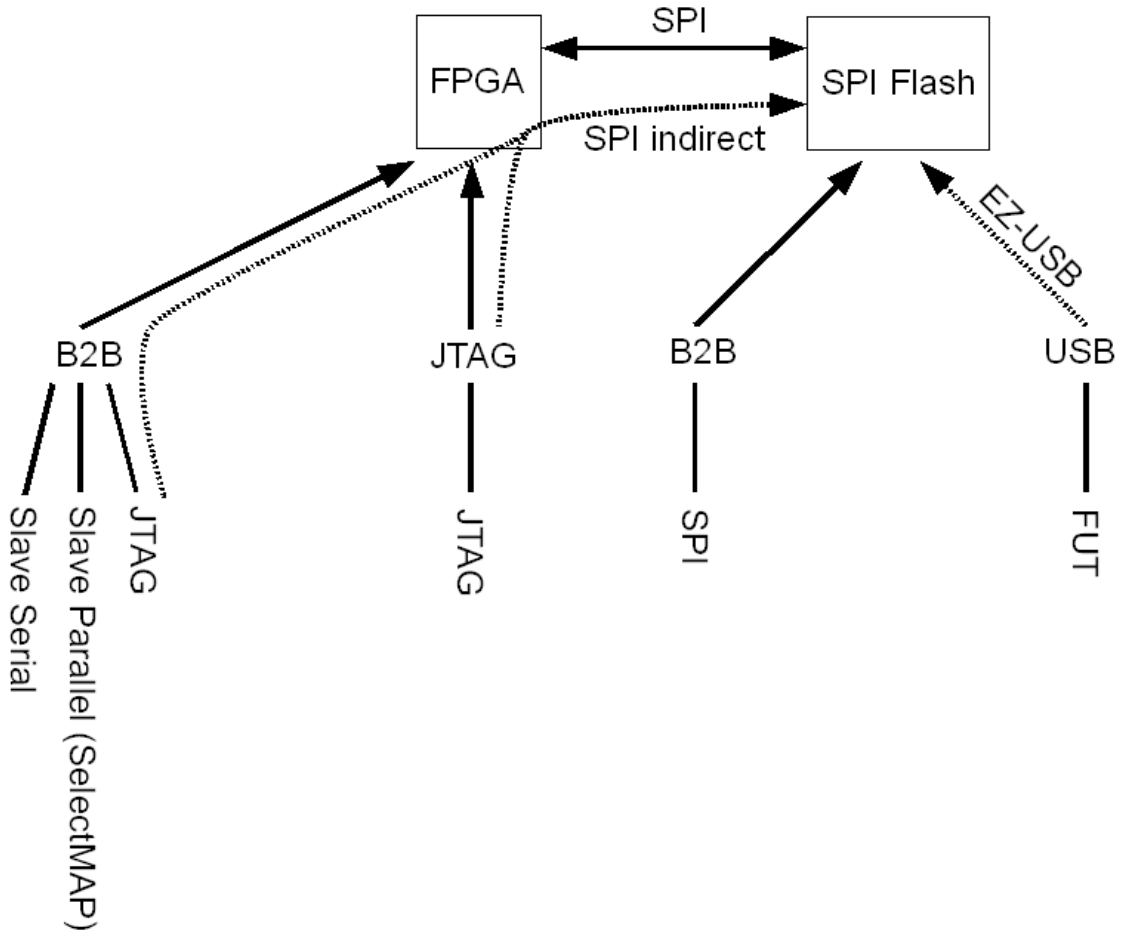


Figure 43: configuration modes overview.

10.1 Mode Select Pins M[2:0]

The mode select pins M[2:0] define the configuration mode that the FPGA uses to load its bitstream. Table 20 shows the configuration modes supported by TE0320. The logic level applied to the mode pins is sampled on the rising edge of INIT_B, immediately after the FPGA completes initializing its internal configuration memory. See Xilinx UG332: Spartan-3 Generation Configuration User Guide for additional information on these signals.

configuration mode	M2	M1	M0
master SPI	0	0	1
JTAG	1	0	1
slave parallel (SelectMAP)	1	1	0
slave serial	1	1	1

Table 20: mode pin settings supported by TE0320.

Xilinx Spartan-3 generation FPGAs have a dedicated four-wire IEEE 1149.1/1532 JTAG port that is always available any time the FPGA is powered and regardless of the mode pin settings. However, when the FPGA mode pins are set for JTAG mode (M[2:0] = <1:0:1>), the FPGA waits to be configured via the JTAG port after a power-on event or after PROG_B is pulsed Low. Selecting the JTAG mode simply disables the other configuration modes. No other pins are required as part of the configuration interface.

M0-M2 have Pull ups in FPGA.

If S1B S1C is off, then signals from B2B should be left float. If S1B C1C is on, then mode can be set from B2B.

Stop condition: Never set Mx from B2B directly to one,

Table 21 shows some options about setting mode pin M2 high or low.

M2 value	M2 @ S1B	M2 @ JM5
0	0N	any
0	any	0
1	OFF	floating
1	OFF	1

Table 21: mode pin M2 settings.

Table 22 shows some options about setting mode pin M1 high or low.

M1 value	M1 @ S1C	M1 @ JM5
0	0N	any
0	any	0
1	OFF	floating
1	OFF	1

Table 22: mode pin M1 settings.

Table 23 shows some options about setting mode pin M0 high or low.

M0 value	M0 @ JM5
0	0
1	floating
1	1

Table 23: mode pin M0 settings.

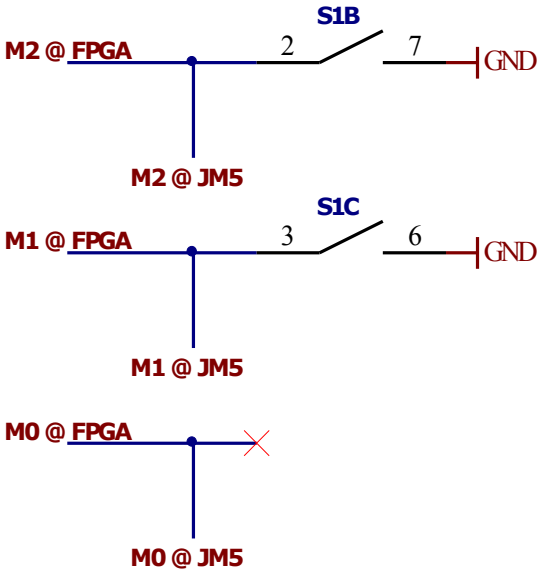


Figure 44: configuration modes schematic

10.2 Configuration via USB bus

To configure a TE0320 module via USB bus, there are different procedures to follow according to module status and purpose of use. For instance, a full quality control test already performed at Trenz Electronic laboratory premises requires all the following steps to be performed:

(a) generic USB device driver installation

(b) USB microcontroller large EEPROM programming

(c) specific USB device driver installation

(d) FWU file generation

(e) Firmware Upgrade Tool utilization.

step	first development cycle	following development cycles	EEPROM recovery	quality control (lab test)
(a)			•	•
(b)			•	•
(c)	•			•
(d)	•	•		•
(e)	•	•		•

Table 24: configuration steps via USB bus according to module status and purpose of use.

10.2.1 generic USB device driver installation

TE0320 users are normally not required to perform this step.

This step has to be performed when a Trenz Electronic module with EZ-USB technology is connected to a computer on which the Cypress generic USB device driver is not yet installed.

Disconnect the TE0320 from the USB bus or leave it unconnected if it already is.

Ensure that DIP switch S1 is set as follows:

- S1A = OFF

  this disconnect the serial data line between the USB microcontroller and the large EEPROM; in so doing, the USB microcontroller enumerates as a Cypress generic USB device
- S1B and S1C = do not care

  configuration mode is irrelevant for this step
- S1D = OFF

  master reset disabled

switch	S1 label	signal name	status
S1A	1	EEPROM serial data	OFF
S1B	2	M2	X
S1C	3	M1	X
S1D	4	/MR (master reset)	OFF

Table 25: S1 Settings for installing generic USB device driver.

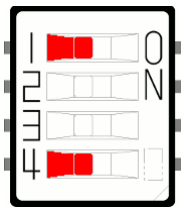
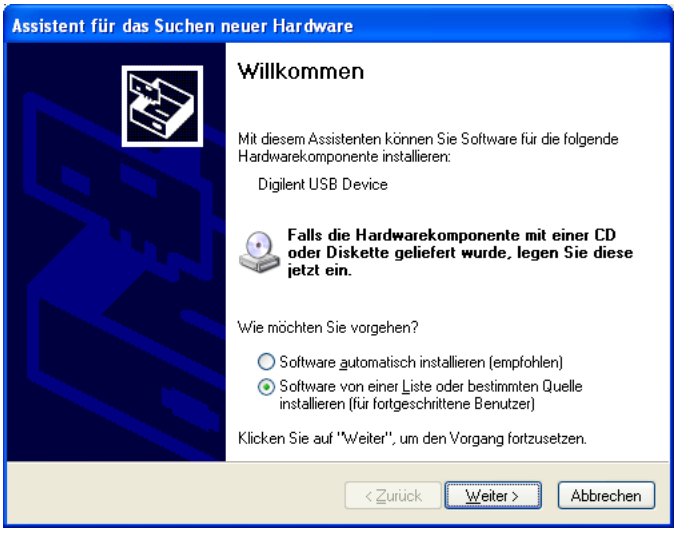
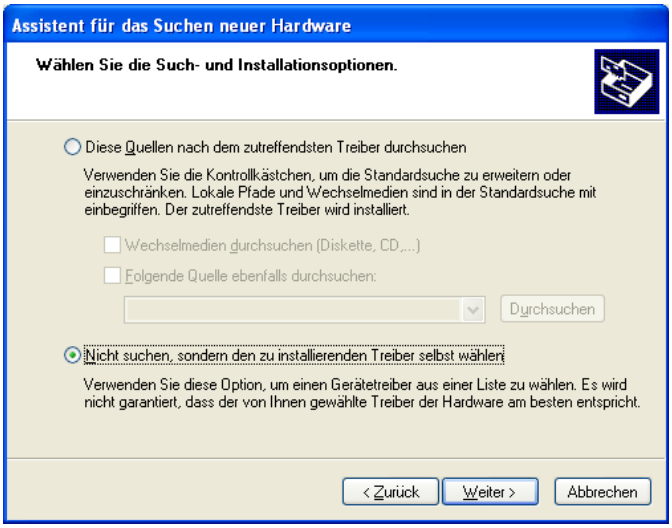


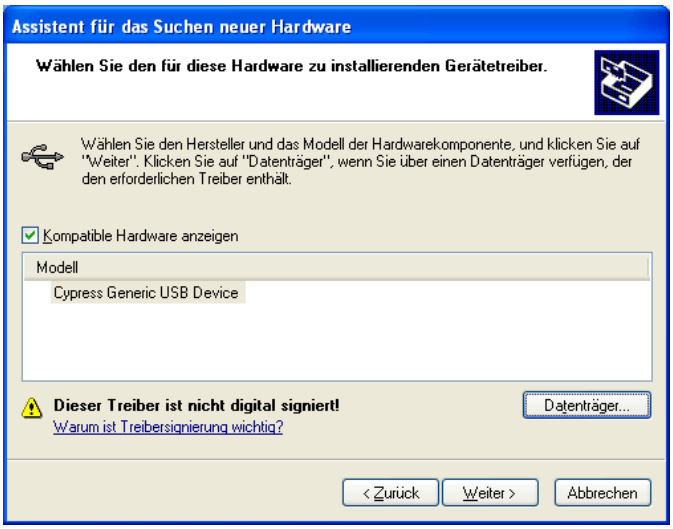
Figure 45: S1 Settings for installing generic USB device driver.

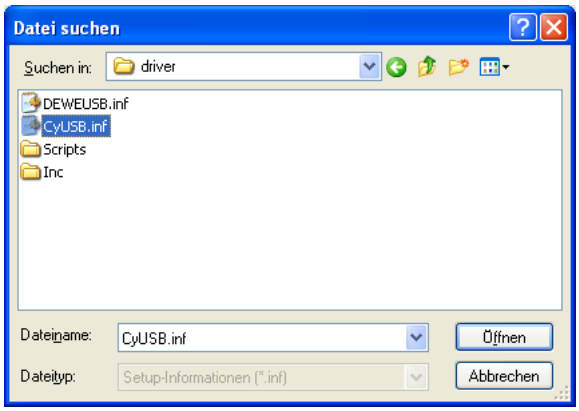
Connect the TE0320 to a USB port on your computer using a USB cable.

Follow the “Found New Hardware” wizard to install the driver, if necessary, as shown in the following example. You need to look for the *step1_factory/CyUSB.inf* device driver information file in the TE0320 software package.

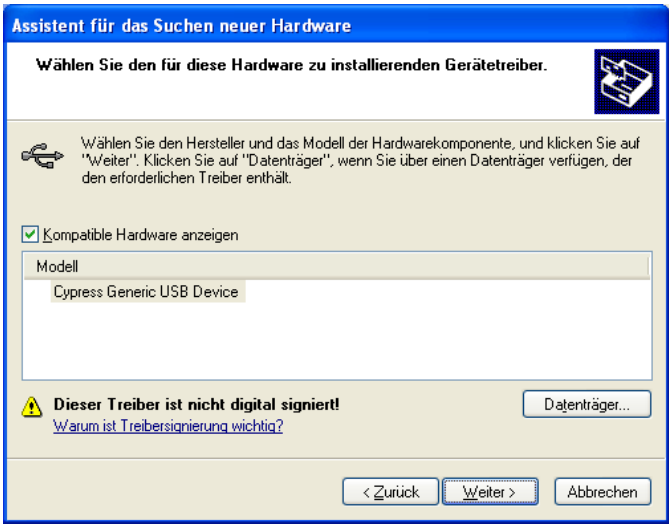

Assistent für das Suchen neuer Hardware
Willkommen
Mit diesem Assistenten können Sie Software für die folgende Hardwarekomponente installieren:
Digilent USB Device
Falls die Hardwarekomponente mit einer CD oder Diskette geliefert wurde, legen Sie diese jetzt ein.
Wie möchten Sie vorgehen?
Software automatisch installieren (empfohlen)
Software von einer Liste oder bestimmten Quelle installieren (für fortgeschrittene Benutzer)
Klicken Sie auf "Weiter", um den Vorgang fortzusetzen.
< Zurück
Weiter >
Abbrechen

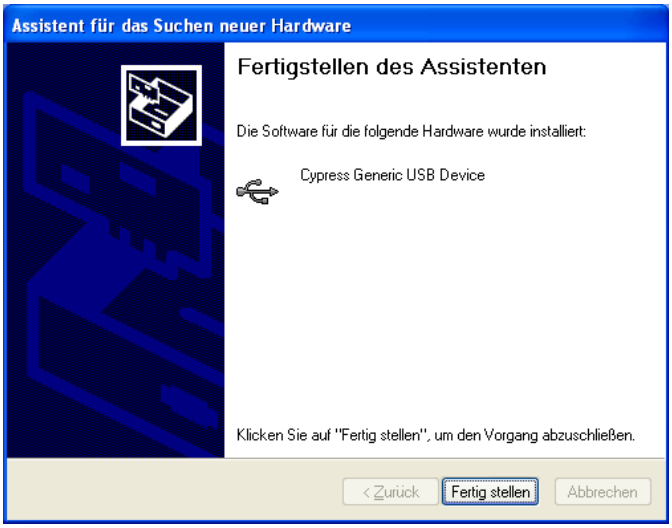

Assistent für das Suchen neuer Hardware
Wählen Sie die Such- und Installationsoptionen.
Diese Quellen nach dem zutreffendsten Treiber durchsuchen
Verwenden Sie die Kontrollkästchen, um die Standardsuche zu erweitern oder einzuschränken. Lokale Pfade und Wechselmedien sind in der Standardsuche mit einbegriffen. Der zutreffendste Treiber wird installiert.
Wechselmedien durchsuchen (Diskette, CD,...)
Folgende Quelle ebenfalls durchsuchen:
Durchsuchen
Nicht suchen, sondern den zu installierenden Treiber selbst wählen
Verwenden Sie diese Option, um einen Gerätetreiber aus einer Liste zu wählen. Es wird nicht garantiert, dass der von Ihnen gewählte Treiber der Hardware am besten entspricht.
< Zurück
Weiter >
Abbrechen


Assistent für das Suchen neuer Hardware
Wählen Sie den für diese Hardware zu installierenden Gerätetreiber.
Wählen Sie den Hersteller und das Modell der Hardwarekomponente, und klicken Sie auf "Weiter". Klicken Sie auf "Datenträger", wenn Sie über einen Datenträger verfügen, der den erforderlichen Treiber enthält.
Kompatible Hardware anzeigen
Modell
Cypress Generic USB Device
Dieser Treiber ist nicht digital signiert!
Warum ist Treibersignierung wichtig?
Datenträger...
< Zurück
Weiter >
Abbrechen


Datei suchen
Suchen in:
driver
DEWEUSB.inf
CyUSB.inf
Scripts
Inc
Dateiname:
CyUSB.inf
Öffnen
Dateityp:
Setup-Informationen (*.inf)
Abbrechen


Installation von Datenträger
Legen Sie den Installationsdatenträger des Herstellers ein und stellen Sie sicher, dass weiter unten das richtige Laufwerk ausgewählt ist.
OK
Abbrechen
Dateien des Herstellers kopieren von:
E:\TE0320\1st_program\driver
Durchsuchen...


Assistent für das Suchen neuer Hardware
Wählen Sie den für diese Hardware zu installierenden Gerätetreiber.
Wählen Sie den Hersteller und das Modell der Hardwarekomponente, und klicken Sie auf "Weiter". Klicken Sie auf "Datenträger", wenn Sie über einen Datenträger verfügen, der den erforderlichen Treiber enthält.
Kompatible Hardware anzeigen
Modell
Cypress Generic USB Device
Dieser Treiber ist nicht digital signiert!
Warum ist Treibersignierung wichtig?
Datenträger...
< Zurück
Weiter >
Abbrechen



After successful installation of the generic device driver, TE0320 should be identified as “Cypress Generic USB Device” and the Device Manager panel should look like Figure 46.

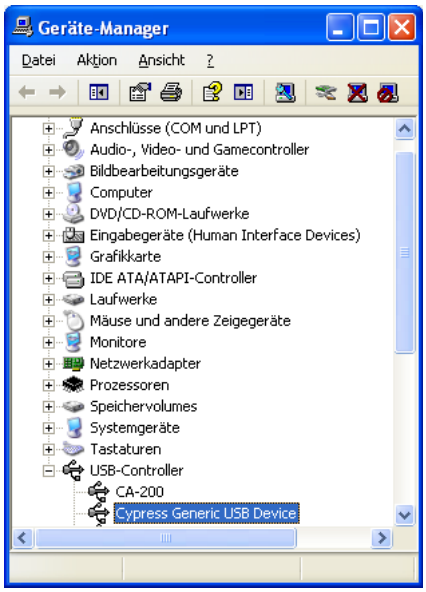


Figure 46: Device manager after successful installation of the generic device driver.

Now the EZ-USB microcontroller can be controlled from a computer by the Cypress USB Console.

10.2.2 USB microcontroller large EEPROM programming

TE0320 users are not normally required to perform this step.

Disconnect the TE0320 from the USB bus or leave it unconnected if it already is.

Ensure that DIP switch S1 is set as follows:

- S1A = OFF

  this disconnect the serial data line between the USB microcontroller and the large EEPROM; in so doing, the USB microcontroller enumerates as a

Cypress generic USB device

- S1B and S1C = do not care

  configuration mode is irrelevant for this step
- S1D = OFF

  master reset disabled

switch	S1 label	signal name	status
S1A	1	EEPROM serial data	OFF
S1B	2	M2	X
S1C	3	M1	X
S1D	4	/MR (master reset)	OFF

Table 26: S1 settings for forcing the EZ-USB FX2LP USB microcontroller to enumerate as a generic USB device driver.

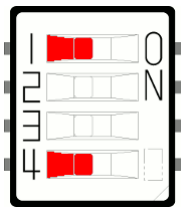


Figure 47: S1 settings for forcing the EZ-USB FX2LP USB microcontroller to enumerate as a generic USB device driver.

Connect the TE0320 to a USB port on your computer using a USB cable.

The USB microcontroller should now enumerate as a Cypress generic USB device.

Toggle S1A to ON; this will

- Connect the serial data line between the USB microcontroller and the large EEPROM;
- Allow the EZ-USB FX2LP USB microcontroller to program the large EEPROM;
- Prevent the EZ-USB FX2LP USB microcontroller to enumerate again for any content of the large EEPROM.

switch	S1 label	signal name	status
S1A	1	EEPROM serial data	ON
S1B	2	M2	X
S1C	3	M1	X
S1D	4	/MR (master reset)	OFF

Table 27: S1 settings for programming EZ-USB FX2LP USB microcontroller large EEPROM.

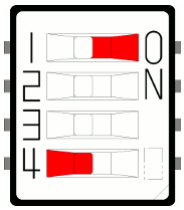
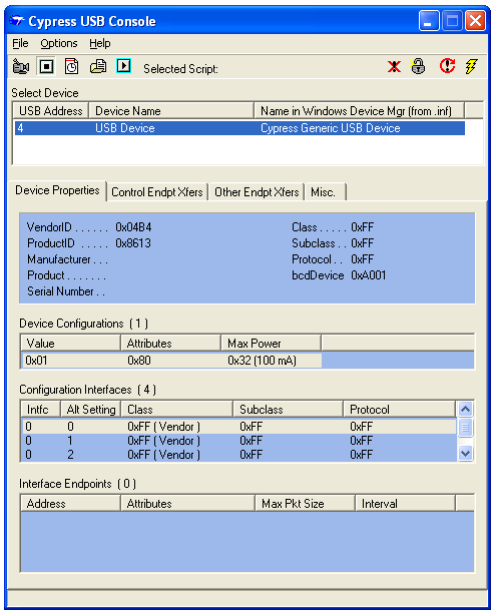
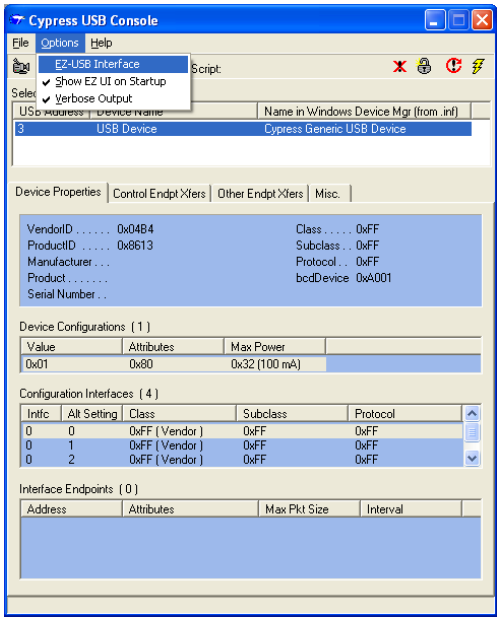


Figure 48: S1 settings for programming EZ-USB FX2LP USB microcontroller large EEPROM.

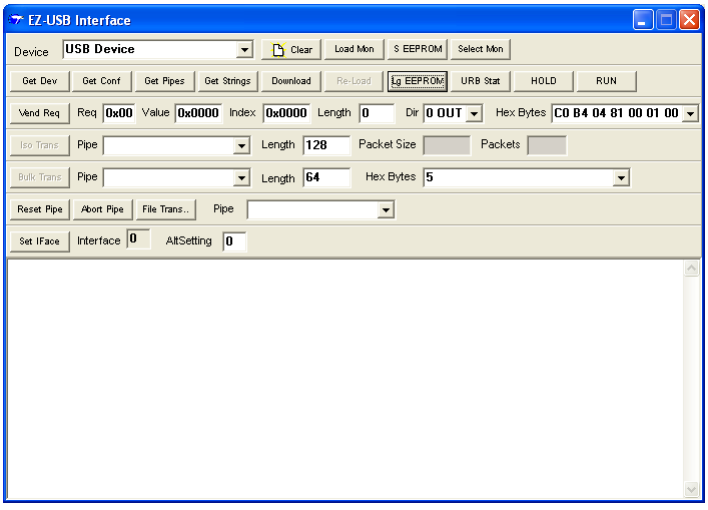


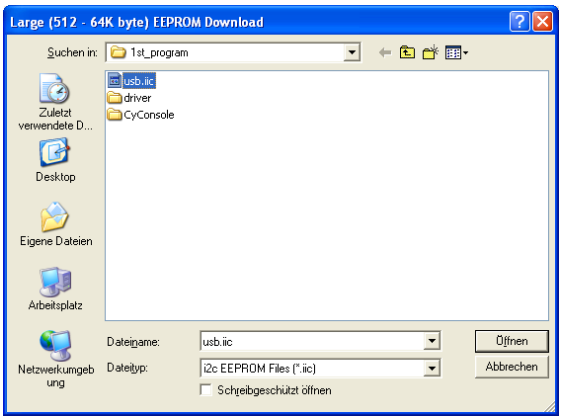
Run Cypress USB Console application from the TE0320 software package: *1st_program\CyConsole\CyConsole.exe*. The device must have the status “Cypress Generic USB Device” in the *select device* display. This indicates that the Cypress USB Console recognizes the EZ-USB microcontroller.



Click Options from the top menu of the CyConsole window and then choose the EZ-USB Interface.

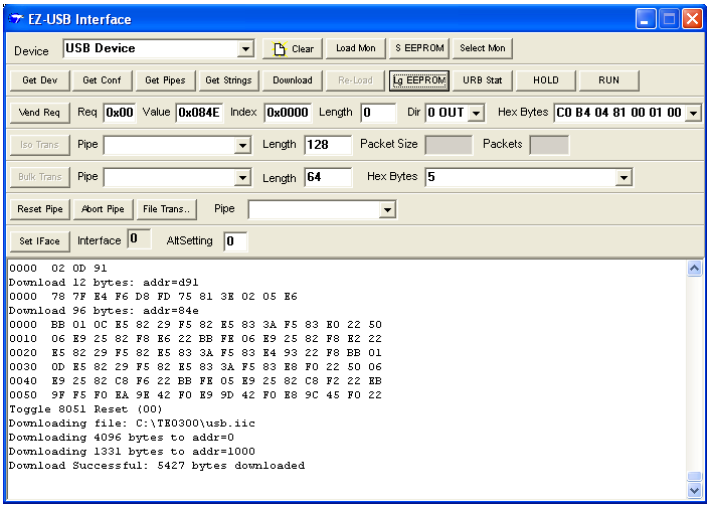
A new application window opens: EZ-USB Interface. “S EEPROM” button refers to the small EEPROM (256 bytes) whereas the “Lg EEPROM” one refers to the large EEPROM (64 kbit). Press the “Lg_EEPROM” button.





Select the *step2_factory/USB.iic* file in the TE0320 software package and press the “Open” button to start writing to EEPROM.

The display window shows the process of IIC file being programmed into the EEPROM and displays “Downloaded Successful” when completed.



10.2.3 specific USB device driver installation

TE0320 users are normally required to perform this step when a Trenz Electronic module with DEWESoft technology is connected to a computer on which the DEWESoft specific USB device driver is not yet installed.

Disconnect the TE0320 from the USB bus or leave it unconnected if it already is.

Ensure that DIP switch S1 is set as follows:

- S1A = ON

  this connect the serial data line between the USB microcontroller and the large EEPROM; in so doing, the USB microcontroller is able to read the large EEPROM and enumerate as a DEWESoft specific USB device
- S1B and S1C = do not care

  configuration mode is irrelevant for this step
- S1D = OFF

  master reset disabled

switch	S1 label	signal name	status
S1A	1	EEPROM serial data	ON
S1B	2	M2	X
S1C	3	M1	X
S1D	4	/MR (master reset)	OFF

Table 28: S1 settings for installing specific USB device driver.

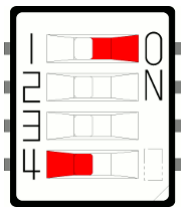
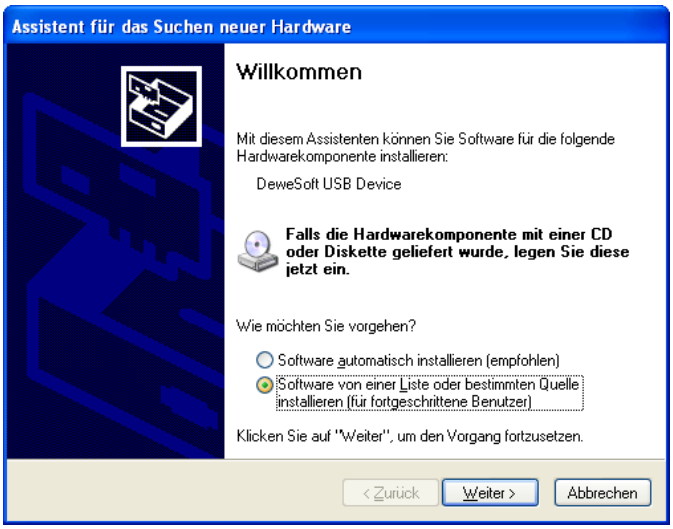
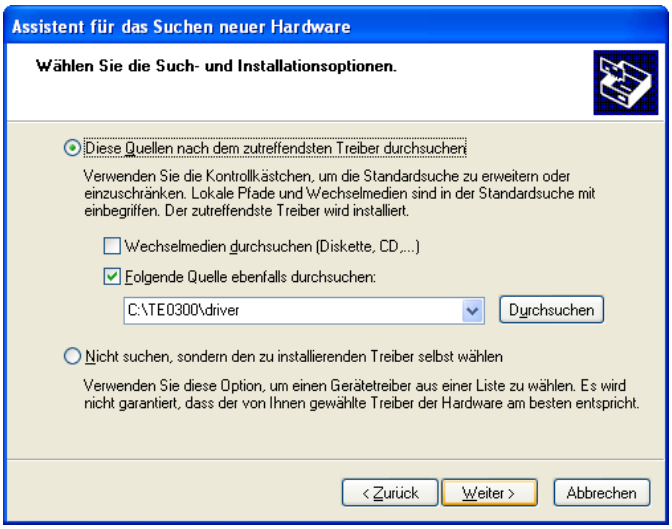


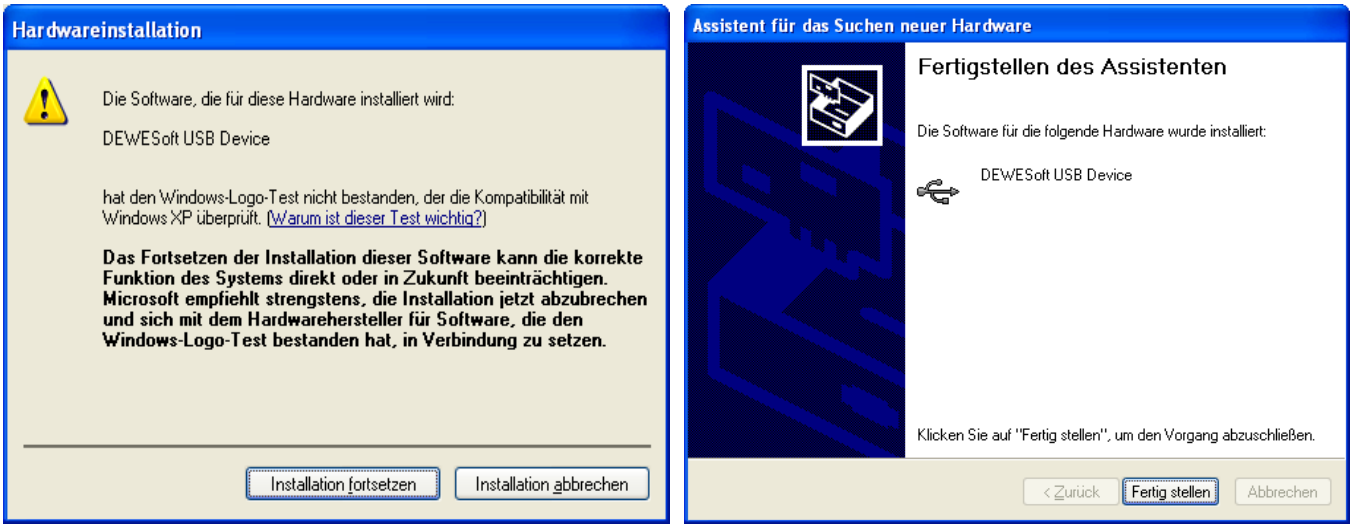
Figure 49: S1 settings for installing pecific USB device driver.

Connect the TE0320 to a USB port on your computer using a USB cable.

Follow the “Found New Hardware” wizard to install the driver, if necessary, as shown in the following example. You need to look for the *step3_user/DEWESOFT.inf* device driver information file in the TE0320 software package.







After successful installation of the specific device driver, TE0320 should be identified as “DEWESoft USB Device” and the Device Manager panel should look like Figure 50.

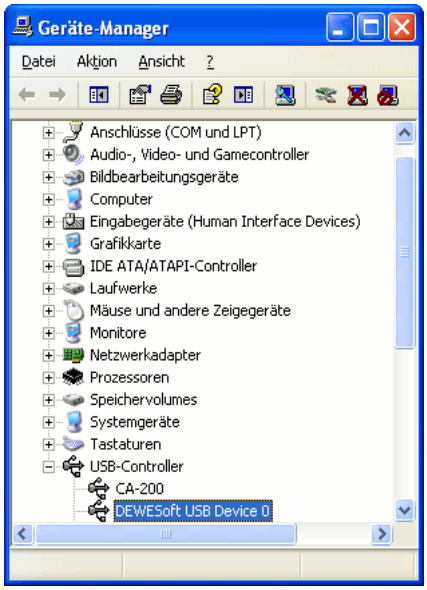


Figure 50: device manager after successful installation of the specific device driver.

Now the EZ-USB FX2LP USB microcontroller can be controlled from a computer by the DEWESoft API.

10.2.4 FWU file generation

In order to generate the FWU file you shall

(a) generate a bit-stream file from your Xilinx EDK design;

(b) generate a PROM file from the bit-stream file;

(c) generate a FWU file from the PROM file.

10.2.4.1 bit-stream file from your Xilinx EDK design

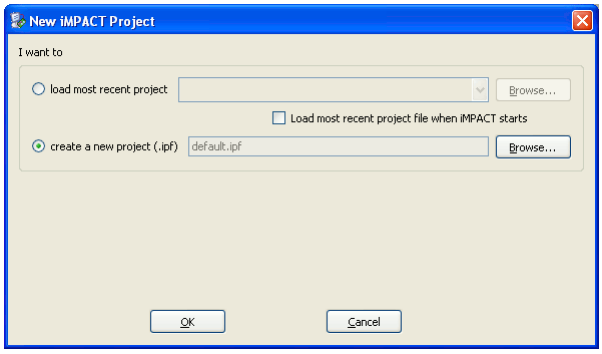
In order to generate a `.bit` bit-stream file from your Xilinx EDK design, you shall

- open your `./system.xmp` project file with Xilinx EDK;
- select ***project / clean all generated files*** (optional);
- select ***hardware / generate bitstream***.

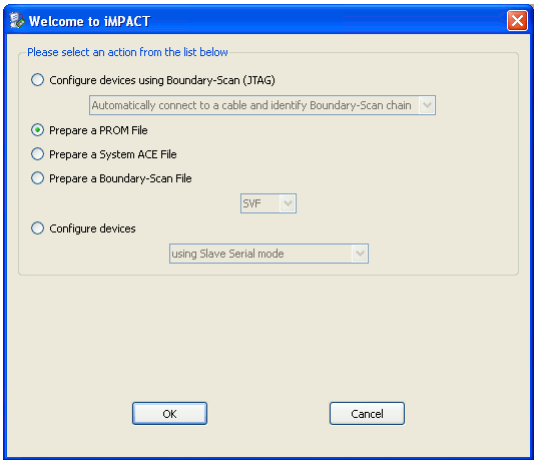
This will generate the bit-stream file `download.bit` in the `./implementation/` folder of your "`.`" project folder.

10.2.4.2 PROM file from the bit-stream file

In order to generate a `.bin` PROM file from the bit-stream file `download.bit`, start Xilinx iMPACT. The following example shows the case of Xilinx iMPACT 11.3.

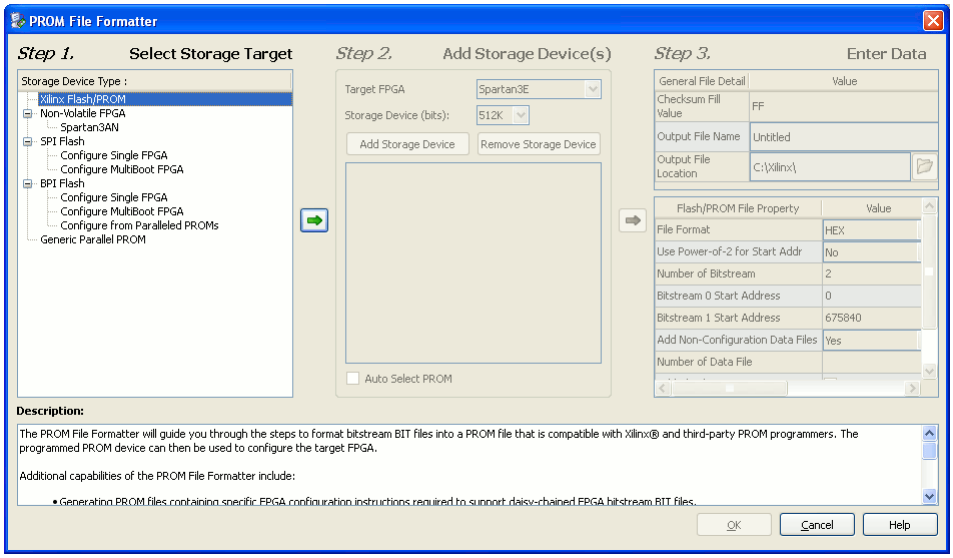


Select ***file / new project***.
Choose ***create a new project***.
Press ***OK***.

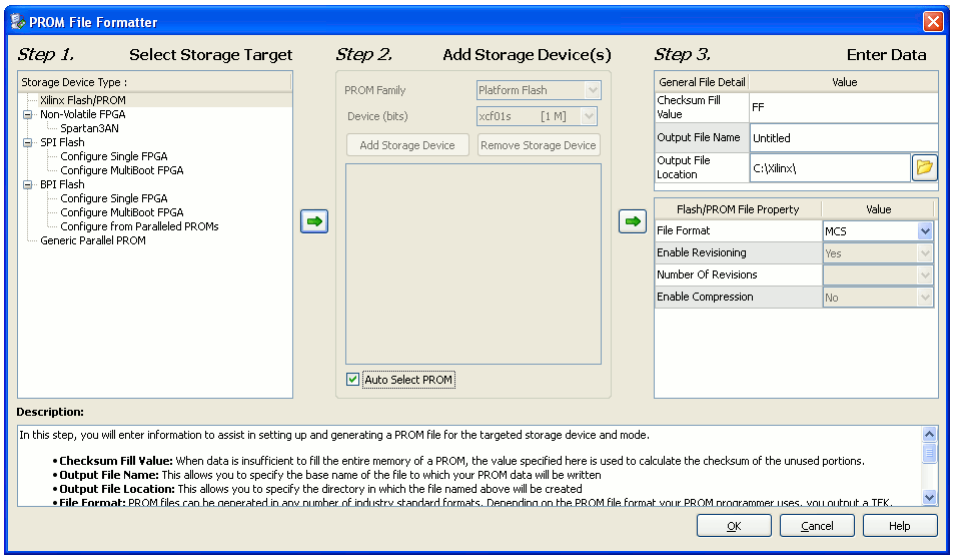


Select ***prepare a PROM file***.
Press ***OK***.

Select ***step 1. storage target / Xilinx Flash/PROM*** of the left panel and press the left green arrow.

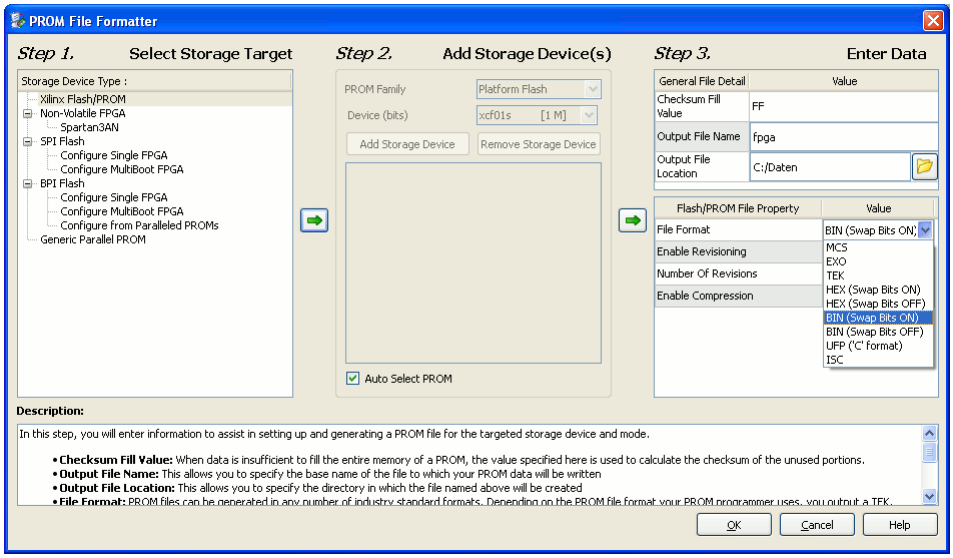


Select ***step 2. add storage device(s) / auto select PROM*** of the middle panel and press the right green arrow.



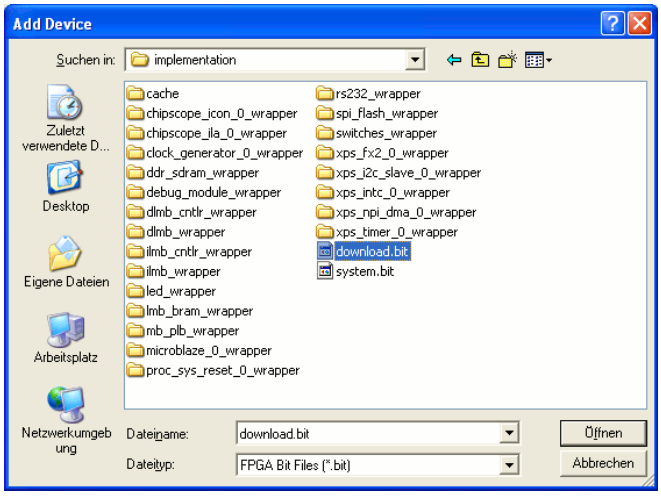
In ***step 3. enter data*** of the right panel

- type ***fpga*** in the `output file name` input field;
- choose a suitable path for the `output file location` input field;
- select ***BIN (swap bits ON)*** from the drop-down menu `file format` in the `flash/PROM file property` sub-panel;
- press the ***OK*** button in the bottom left corner of the current window.

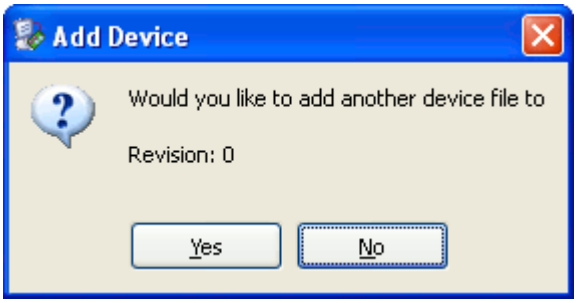


Any other name than ***fpga*** for the `output file name` input field is not allowed.

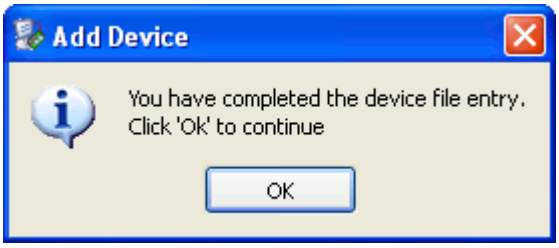
Just acknowledge the pup-up message.



Browse to the `./implementation/` folder of your "`.`" project folder and select the bit-stream file `download.bit`.
Press the ***open*** button in the bottom left corner of the current window.

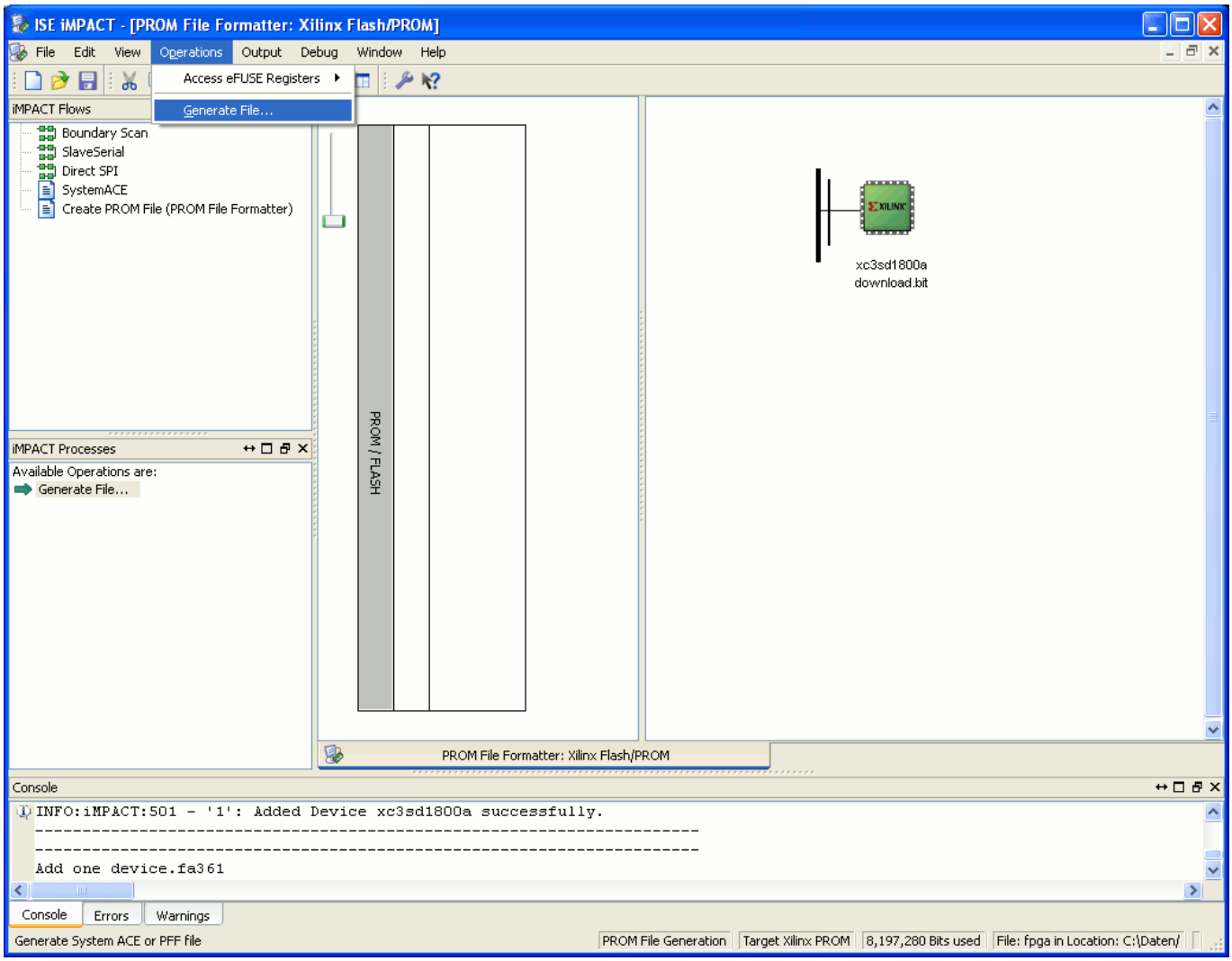


Your design likely consist of just one device file. So deny the request by pressing the ***NO*** button.

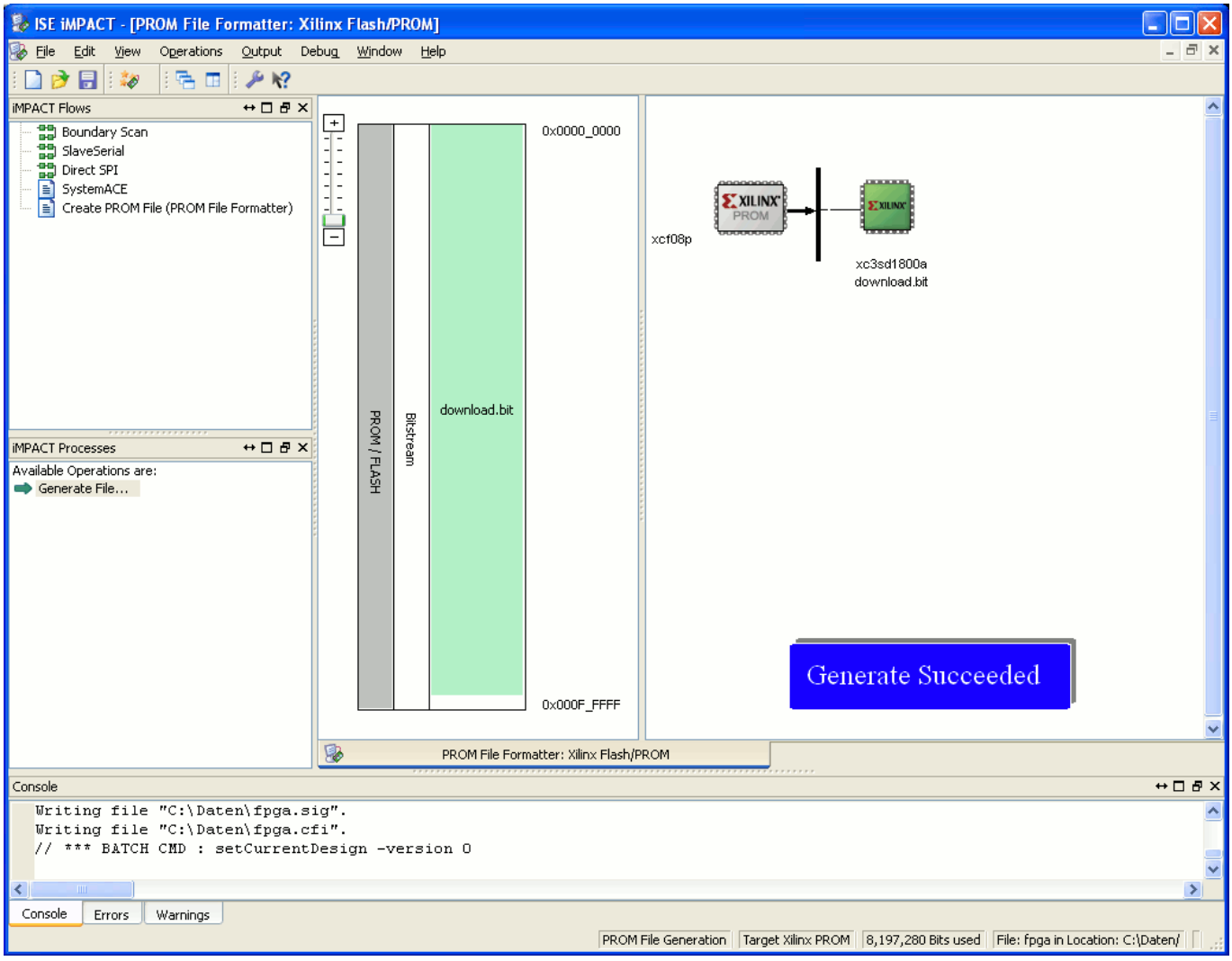


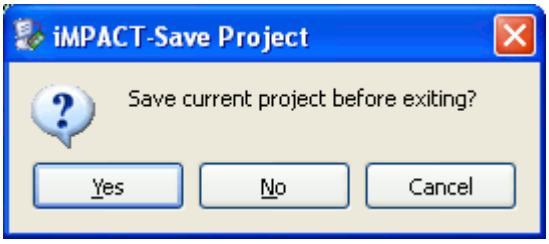
Just acknowledge the pup-up message.

Select ***operations / generate file...*** or double click ***generate file...*** from the `iMPACT processes` panel.



You should see the following message in the main panel: `generate succeeded.`





You might now want to save your Xilinx iMPACT project settings for future use.

In the folder corresponding to the path you chose as the `output file location`, you should find the `fpga.bin` PROM file.

10.2.4.3 FWU file from the PROM file

Once you have got your `fpga.bin` PROM file, you can proceed and generate your FWU (= FirmWare Upgrade) file. The FWU file is a ZIP archive containing 3 files:

- `Bootload.ini` – TE0320 booting settings (see paragraph 10.2.4.3.1 Bootload.ini file)
- `fpga.bin` – FPGA configuration PROM file

- `usb.bin` – EZ-USB FX2LP USB microcontroller firmware

To create your FWU file, you shall

- replace the existing `step4_user\fpga.bin` with the latest `fpga.bin` (once per design)
- zip the 3 files
- rename the `zip` file extension to `fwu`
- upload the file as explained in paragraph 10.2.5 Firmware Upgrade Tool utilization.

Warning! file and path names are given and must not be changed!

10.2.4.3.1 Bootload.ini file

The `step4_user\Bootload.ini` file defines some module start-up options. Version 1.0 of Bootload.ini has the following structure:

- `[Info]` – information section (do not edit this section)
  - `Version` – Bootload.ini file format version
  - `DeviceType` – 3 stands for current device type
- [Settings]: settings section
  - `FPGABitSwap` – see Xilinx UG332: Spartan-3 Generation Configuration User Guide, chapter SelectMAP Data Ordering (default = 1 = do bit swapping)
  - `FPGAPowerON` – value of FX2_PS_EN after SPI Flash memory programming (see paragraph 6.8.2 Slide Switch S2) (default = 1 = power on after upgrade)

10.2.4.3.2 usb.bin file

The `step4_user\usb.bin` file contains the firmware to be written in the large EEPROM of the EZ-USB FX2LP USB microcontroller and loaded at module start-up to implement the DEWESoft instruction set.

10.2.5 Firmware Upgrade Tool utilization

10.2.5.1 Switch Settings

For the Firmware Upgrade Tool to operate correctly, switch S1 and S2 shall be set properly.

10.2.5.2 DIP Switch S1

Ensure that DIP switch S1 is set to

- USB microcontroller large EEPROM enabled (S1A set to ON)
- configuration mode set to Master SPI (S1B and S1C set to ON)

- master reset disabled (S1D set to OFF)

S1	S1 label	signal	status
S1A	1	EEPROM serial data	ON
S1B	2	M2	ON
S1C	3	M1	ON
S1D	4	/MR (master reset)	OFF

Table 29: S1 settings for configuration via USB bus.

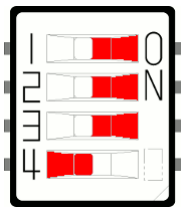


Figure 51: S1 settings for configuration via USB bus.

10.2.5.3 Slide Switch S2

Ensure that slide switch S2 is set to FX2 PON.

switch	signal	status
S2	PON / FX2 PON	FX2PON

Table 30: S2 settings for SPI Flash programming via USB bus.

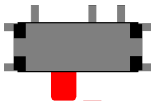


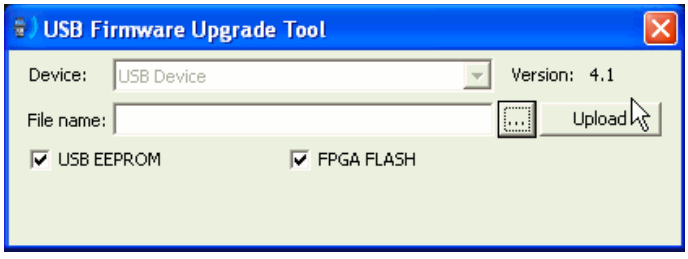
Figure 22: S2 settings for SPI Flash programming via USB bus (FX2 PON).

This will

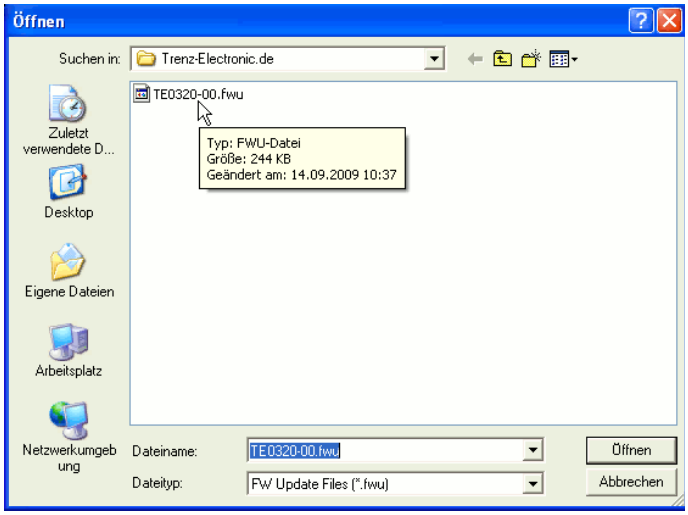
- allow the EZ-USB FX2LP USB microcontroller to power off the FPGA,
- release the SPI lines driven by the FPGA and made them available to the EZ-USB FX2LP USB microcontroller
- allow the EZ-USB FX2LP USB microcontroller to program the SPI Flash memory.

10.2.5.4 FUT upgrade procedure

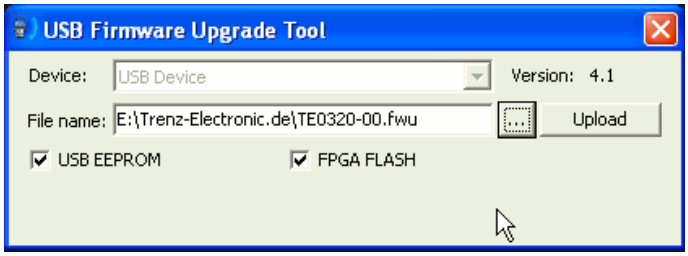
Open `USB Firmware Upgrade Tool` (double click `step5_user\USBFirmwareUpgradeTool.exe`).



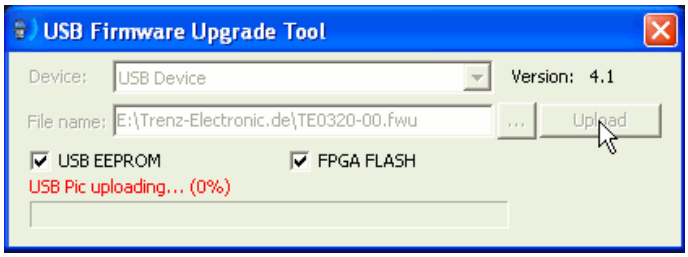
Press the "`...`" button corresponding to the `File name`:



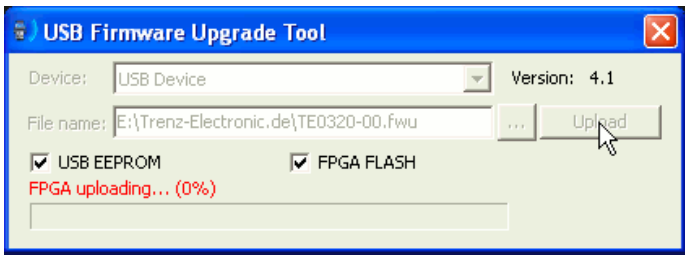
Select a suitable `.fwu` firmware upload file.
Press the ***open*** button.



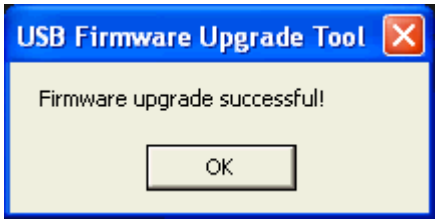
Check the ***USB EEPROM*** box if you want the `usb.bin` file compressed into the `.fwu` file to be written into the large EEPROM of the EZ-USB FX2LP USB microcontroller.
Check the ***FPGA FLASH*** box if you want the fpga`.bin` file compressed into the `.fwu` file to be written into the SPI Flash memory.
Press the ***upload*** button.



The tool will first attempt to write the large EEPROM, if the corresponding box has been selected.



The tool will then attempt to write the SPI Flash memory, if the corresponding box has been selected.



When the progress bar reaches 100%, the following pop-up message notifies the successful completion of the USB upgrade procedure.

If the `FPGAPowerON` bit in the `Bootload.ini` file was set to ***1***, the FPGA will try to configure from SPI Flash memory straight after successful completion of the FUT utilization.

If the `FPGAPowerON` bit in the `Bootload.ini` file was set to ***0***, the FPGA keep powered off.

10.3 Configuration Using Indirect SPI Configuration Mode

Similar to the traditional configuration memories, SPI serial Flash memories must be loaded with the configuration data. SPI serial Flash memories have a single interface for programming, but there are multiple methods to deliver the data to this interface. This section discusses the hardware setup, the PROM file generation flow and the software flow for ISP (indirect in-system programming) of a Trenz Electronic TE0320 SPI serial Flash configuration PROM through the JTAG interface of a Xilinx Spartan-3A DSP FPGA using Xilinx iMPACT 11.5.

To write the SPI Flash memory, perform the following steps:

(a) disable the master reset S1D (do not care about all other switches at write time);

(b) connect the Xilinx platform cable to JTAG connector J2 as described in paragraph 6.3.1 JTAG connector J2;

(c) generate or locate the FPGA bit-stream file you want to store on the memory;

(d) prepare an SPI PROM file using the ISE iMPACT graphical software from the FPGA bit-stream file;

(e) use the ISE iMPACT graphical software to in-system program the SPI PROM.

In order to have the module to configure from its SPI Flash memory next time it is (re)booted, ensure one of following DIP switch settings:

switch	S1A (EEPROM serial data)	S1B (M2)	S1C (M1)	S1D (/MR master reset)	S2 (PS_EN)
state	0 = ON	0 = ON	0 = ON	1 = OFF	X = do note care
state	1 = OFF	0 = ON	0 = ON	1 = OFF	FX2 PON

Table 31: S1 settings for booting from SPI Flash memory.

For your convenience, a reference video is available on the TrenzElectronic's Channel at YouTube.

For further reference, please read Xilinx XAPP974: Indirect Programming of SPI Serial Flash PROMs with Spartan-3A FPGAs.

11 Recommended Design Tools Settings

11.1 DONE LED

When the configuration process successfully completes, the FPGA either actively drives the DONE pin High (*DriveDone*) or allows the DONE pin to float High using either an internal or external pull-up resistor, controlled by the *DonePin* bitstream generator option. To have DONE LED D1 lit after successful FPGA configuration, DriveDone and DonePin bitstream generator options for the DONE pin have to be set to have DONE actively driving its line (see Figure 52 and Table 32).

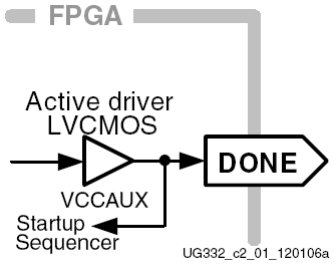


Figure 52: DriveDone and DonePin set to have DONE actively driving its line.

DriveDone defines whether the DONE pin is an active driver or an open-drain output.

DonePin defines whether or not the DONE pin has an internal pull-up resistor.

bitstream generator (BitGen) option	Setting
DriveDone	Yes
DonePin	Pullnone

Table 32: DriveDone and DonePin settings for having DONE actively driving its line.

See Xilinx UG332: Spartan-3 Generation Configuration User Guide (paragraph "DONE Pin") for additional information on these signals.

This options are set graphically in Xilinx ISE Software Project Navigator by selecting the following:

- Generate Programming File > Process Properties > Startup Options > Drive Done Pin High > check the box
- Generate Programming File > Process Properties > Configuration Options > Configuration Pin Done > float

Xilinx ISE Project Navigator option	setting
Drive Done Pin High	√ (checked)
Configuration Pin Done	Float

Table 33: Xilinx ISE Project Navigator settings for having DONE actively driving its line.

Consult *ISE Help* about the Process Properties of the Generate Programming File process in the Processes pane for additional information on these properties.

11.2 Unused IOB Pins

All signals entering and exiting a Xilinx Spartan-3 generation FPGA must pass through the I/O resources, known as I/O blocks or IOBs. Users can specify the configuration for any unused IOB pins. This is the serial data outputs for all JTAG instruction and data registers.

This options are set graphically in Xilinx ISE Software Project Navigator by selecting the following:

- Generate Programming File > Process Properties > Configuration Options > Unused IOB Pins

Select an option from the drop-down list.

(a) Pull Down
Default. All unused I/O pins and input-only pins have a pull-down resistor to GND.

(b) Pull Up
All unused I/O pins and input-only pins have a pull-up resistor to the VCCO_# supply for its associated I/O bank.

(c) Float (also: Pullnone)
All unused I/O pins and input-only pins are left floating (Hi-Z, high-impedance, three-state). Use external pull-up or pulldown resistors or logic to apply a valid signal level.

11.3 CCLK Frequency

In SPI Flash mode, the FPGA's internal oscillator generates the configuration clock frequency. The FPGA provides this clock on its CCLK output pin, driving the PROM's Slave Clock input pin. The FPGA begins configuring using its lowest frequency setting. If so specified in the configuration bitstream, the FPGA increases the CCLK frequency to the specified setting for the remainder of the configuration process. The maximum frequency is specified using the ConfigRate bitstream generator option. The maximum frequency supported by the FPGA configuration logic depends on the timing for the SPI Flash device. For TE0320 SPI Flash PROM, use ConfigRate = 12 or lower.

This options are set graphically in Xilinx ISE Software Project Navigator by selecting the following:

- Generate Programming File > Process Properties > Configuration Options > Configuration Rate > 12 (or lower)

12 Reference Design Summaries (ISE 11.5)

12.1 Reference Design Summary for Xilinx Spartan-3A DSP 1800

```
--------------------------------------------------------------------------

platgen -p xc3sd1800afg676-4 -lang vhdl -lp x:/xxx/projects_EDK/  system.mhs
Release 11.5 - platgen Xilinx EDK 11.5 Build EDK_LS5.70 (nt)
Copyright (c) 1995-2009 Xilinx, Inc.  All rights reserved.

--------------------------------------------------------------------------

Command Line: platgen -p xc3sd1800afg676-4 -lang vhdl -lp

Running post-placement packing...

Design Summary:
Number of errors:      0
Number of warnings: 1272
Logic Utilization:
  Number of Slice Flip Flops:         6,442 out of  33,280   19%
  Number of 4 input LUTs:             8,291 out of  33,280   24%
Logic Distribution:
  Number of occupied Slices:          7,304 out of  16,640   43%
    Number of Slices containing only related logic:   7,304 out of   7,304 100%
    Number of Slices containing unrelated logic:          0 out of   7,304   0%
      *See NOTES below for an explanation of the effects of unrelated logic.
  Total Number of 4 input LUTs:       8,663 out of  33,280   26%
    Number used as logic:             6,213
    Number used as a route-thru:        372
    Number used for Dual Port RAMs:   1,892
      (Two LUTs used per Dual Port RAM)
    Number used as Shift registers:     186

  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

  Number of bonded IOBs:                119 out of     519   22%
    IOB Flip Flops:                      39
    IOB Master Pads:                      2
    IOB Slave Pads:                       2
  Number of ODDR2s used:                 44
    Number of DDR_ALIGNMENT = NONE       44
    Number of DDR_ALIGNMENT = C0          0
    Number of DDR_ALIGNMENT = C1          0
  Number of BUFGMUXs:                     5 out of      24   20%
  Number of DCMs:                         1 out of       8   12%
  Number of BSCANs:                       1 out of       1  100%
  Number of DSP48As:                      3 out of      84    3%
  Number of RAMB16BWERs:                 30 out of      84   35%
  Number of BSCAN_SPARTAN3As:             1 out of       1  100%

  Number of RPM macros:            1
Average Fanout of Non-Clock Nets:                3.56

--------------------------------------------------------------------------
```

```
Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)
Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.260 Volts)


Device speed data version:  "PRODUCTION 1.33 2010-02-13".



Design Summary Report:

 Number of External IOBs                          119 out of 519    22%

   Number of External Input IOBs                  30

      Number of External Input IBUFs              30
        Number of LOCed External Input IBUFs      30 out of 30    100%


   Number of External Output IOBs                 43

      Number of External Output DIFFMs             2
        Number of LOCed External Output DIFFMs     2 out of 2     100%

      Number of External Output DIFFSs             2
        Number of LOCed External Output DIFFSs     2 out of 2     100%

      Number of External Output IOBs              39
        Number of LOCed External Output IOBs      39 out of 39    100%


   Number of External Bidir IOBs                  46

      Number of External Bidir IOBs               46
        Number of LOCed External Bidir IOBs       46 out of 46    100%


   Number of BSCANs                             1 out of 1     100%
   Number of BUFGMUXs                           5 out of 24     20%
   Number of DCMs                               1 out of 8      12%
   Number of DSP48As                            3 out of 84      3%
   Number of RAMB16BWERs                       30 out of 84     35%
   Number of Slices                          7304 out of 16640  43%
      Number of SLICEMs                      1156 out of 8320   13%

   Number of LOCed Slices                      125 out of 7304    1%
      Number of LOCed SLICEMs                   83 out of 1156    7%



Overall effort level (-ol):   High
Router effort level (-rl):    High

--------------------------------------------------------------------------------
```

12.2 Reference Design Summary for Xilinx Spartan-3A DSP 3400

```
--------------------------------------------------------------------------

platgen -p xc3sd3400afg676-4 -lang vhdl -lp x:/xxx/projects_EDK/  system.mhs
Release 11.5 - platgen Xilinx EDK 11.5 Build EDK_LS5.70 (nt)
Copyright (c) 1995-2009 Xilinx, Inc.  All rights reserved.

--------------------------------------------------------------------------

Command Line: platgen -p xc3sd3400afg676-4 -lang vhdl -lp

Running post-placement packing...

Design Summary:
Number of errors:      0
Number of warnings: 1272
Logic Utilization:
  Number of Slice Flip Flops:         6,442 out of  47,744   13%
  Number of 4 input LUTs:             8,290 out of  47,744   17%
Logic Distribution:
  Number of occupied Slices:          7,889 out of  23,872   33%
    Number of Slices containing only related logic:   7,889 out of   7,889 100%
    Number of Slices containing unrelated logic:          0 out of   7,889   0%
      *See NOTES below for an explanation of the effects of unrelated logic.
  Total Number of 4 input LUTs:       8,662 out of  47,744   18%
    Number used as logic:             6,212
    Number used as a route-thru:        372
    Number used for Dual Port RAMs:   1,892
      (Two LUTs used per Dual Port RAM)
    Number used as Shift registers:     186

  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

  Number of bonded IOBs:                119 out of     469   25%
    IOB Flip Flops:                      39
    IOB Master Pads:                      2
    IOB Slave Pads:                       2
  Number of ODDR2s used:                 44
    Number of DDR_ALIGNMENT = NONE       44
    Number of DDR_ALIGNMENT = C0          0
    Number of DDR_ALIGNMENT = C1          0
  Number of BUFGMUXs:                     5 out of      24   20%
  Number of DCMs:                         1 out of       8   12%
  Number of BSCANs:                       1 out of       1  100%
  Number of DSP48As:                      3 out of     126    2%
  Number of RAMB16BWERs:                 30 out of     126   23%
  Number of BSCAN_SPARTAN3As:             1 out of       1  100%

  Number of RPM macros:           1
Average Fanout of Non-Clock Nets:               3.56

--------------------------------------------------------------------------
```

```
Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)
Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.260 Volts)


Device speed data version:  "PRODUCTION 1.33 2010-02-13".



Design Summary Report:

 Number of External IOBs                          119 out of 469    25%

   Number of External Input IOBs                  30

      Number of External Input IBUFs              30
        Number of LOCed External Input IBUFs      30 out of 30    100%


   Number of External Output IOBs                 43

      Number of External Output DIFFMs             2
        Number of LOCed External Output DIFFMs     2 out of 2     100%

      Number of External Output DIFFSs             2
        Number of LOCed External Output DIFFSs     2 out of 2     100%

      Number of External Output IOBs              39
        Number of LOCed External Output IOBs      39 out of 39    100%


   Number of External Bidir IOBs                  46

      Number of External Bidir IOBs               46
        Number of LOCed External Bidir IOBs       46 out of 46    100%


   Number of BSCANs                             1 out of 1     100%
   Number of BUFGMUXs                           5 out of 24     20%
   Number of DCMs                               1 out of 8      12%
   Number of DSP48As                            3 out of 126     2%
   Number of RAMB16BWERs                       30 out of 126    23%
   Number of Slices                          7889 out of 23872  33%
      Number of SLICEMs                      1156 out of 11936   9%

   Number of LOCed Slices                     125 out of 7889    1%
      Number of LOCed SLICEMs                  83 out of 1156    7%



Overall effort level (-ol):   High
Router effort level (-rl):    High

--------------------------------------------------------------------------------
```

13 Verification

The quickest way to test most module functions is to execute the sample DMA test available in the `TE0320_API_Example\Release` folder of the TE0320 software package. Hereunder is reported a sample trace of a successful execution.

```
TE0320 DLL Example 1.0
        1 - Get number of modules
        2 - Connect module No 0
        3 - Connect module No 1
        4 - Disconnect
        5 - Get FX2 status
        6 - Get FX2 version
        7 - Get FPGA firmware version
        8 - Get FX2 FIFO Status
        9 - Reset FX2 FIFO Status
        w - Write high speed data (FPGA RX)
        r - Read high speed data (FPGA TX)
        0 - Exit
1
```

```
1
```

```
TE0320 DLL Example 1.0
        1 - Get number of modules
        2 - Connect module No 0
        3 - Connect module No 1
        4 - Disconnect
        5 - Get FX2 status
        6 - Get FX2 version
        7 - Get FPGA firmware version
        8 - Get FX2 FIFO Status
        9 - Reset FX2 FIFO Status
        w - Write high speed data (FPGA RX)
        r - Read high speed data (FPGA TX)
        0 - Exit
2
```

```
TE0320 DLL Example 1.0
        1 - Get number of modules
        2 - Connect module No 0
        3 - Connect module No 1
        4 - Disconnect
        5 - Get FX2 status
        6 - Get FX2 version
        7 - Get FPGA firmware version
        8 - Get FX2 FIFO Status
        9 - Reset FX2 FIFO Status
        w - Write high speed data (FPGA RX)
        r - Read high speed data (FPGA TX)
        0 - Exit
5
```

```
fifo_error: 0
current_mode: 1
flash_busy: 0
fpga_prog.: 170
booting: 1
```

```
TE0320 DLL Example 1.0
        1 - Get number of modules
        2 - Connect module No 0
        3 - Connect module No 1
        4 - Disconnect
        5 - Get FX2 status
        6 - Get FX2 version
        7 - Get FPGA firmware version
        8 - Get FX2 FIFO Status
        9 - Reset FX2 FIFO Status
        w - Write high speed data (FPGA RX)
        r - Read high speed data (FPGA TX)
        0 - Exit
```

```
6
```

```
Major version: 1
Minor version: 7
Device hi: 1
Device lo: 1
```

```
TE0320 DLL Example 1.0
        1 - Get number of modules
        2 - Connect module No 0
        3 - Connect module No 1
        4 - Disconnect
        5 - Get FX2 status
        6 - Get FX2 version
        7 - Get FPGA firmware version
        8 - Get FX2 FIFO Status
        9 - Reset FX2 FIFO Status
        w - Write high speed data (FPGA RX)
        r - Read high speed data (FPGA TX)
        0 - Exit
7
```

```
INT# : 1
Major version: 7
Minor version: 1
Release version: 2
Build version: 24
```

```
TE0320 DLL Example 1.0
        1 - Get number of modules
        2 - Connect module No 0
        3 - Connect module No 1
        4 - Disconnect
        5 - Get FX2 status
        6 - Get FX2 version
        7 - Get FPGA firmware version
        8 - Get FX2 FIFO Status
        9 - Reset FX2 FIFO Status
        w - Write high speed data (FPGA RX)
        r - Read high speed data (FPGA TX)
        0 - Exit
8
```

```
EP2 FIFO CS: 0x04
EP4 FIFO CS: 0x04
EP6 FIFO CS: 0x04
EP8 FIFO CS: 0x04
EP2 FIFO BCH: 0x00
EP4 FIFO BCH: 0x00
EP6 FIFO BCH: 0x00
EP8 FIFO BCH: 0x00
```

```
TE0320 DLL Example 1.0
        1 - Get number of modules
        2 - Connect module No 0
        3 - Connect module No 1
        4 - Disconnect
        5 - Get FX2 status
        6 - Get FX2 version
        7 - Get FPGA firmware version
        8 - Get FX2 FIFO Status
        9 - Reset FX2 FIFO Status
        w - Write high speed data (FPGA RX)
        r - Read high speed data (FPGA TX)
        0 - Exit
```

```
9
```

```
Resetting all FIFOs

TE0320 DLL Example 1.0
        1 - Get number of modules
        2 - Connect module No 0
        3 - Connect module No 1
        4 - Disconnect
        5 - Get FX2 status
        6 - Get FX2 version
        7 - Get FPGA firmware version
        8 - Get FX2 FIFO Status
        9 - Reset FX2 FIFO Status
        w - Write high speed data (FPGA RX)
        r - Read high speed data (FPGA TX)
        0 - Exit
w
Resetting all FIFOs
host->memory data verification PASSED!
Transferred 120000 kB in 4.048 s = 28.953 MB/s

TE0320 DLL Example 1.0
        1 - Get number of modules
        2 - Connect module No 0
        3 - Connect module No 1
        4 - Disconnect
        5 - Get FX2 status
        6 - Get FX2 version
        7 - Get FPGA firmware version
        8 - Get FX2 FIFO Status
        9 - Reset FX2 FIFO Status
        w - Write high speed data (FPGA RX)
        r - Read high speed data (FPGA TX)
        0 - Exit
r
Resetting all FIFOs

memory->host data verification PASSED!!!
Transferred 120000 kB in 3.268 s = 35.861 MB/s

TE0320 DLL Example 1.0
        1 - Get number of modules
        2 - Connect module No 0
        3 - Connect module No 1
        4 - Disconnect
        5 - Get FX2 status
        6 - Get FX2 version
        7 - Get FPGA firmware version
        8 - Get FX2 FIFO Status
        9 - Reset FX2 FIFO Status
        w - Write high speed data (FPGA RX)
        r - Read high speed data (FPGA TX)
        0 - Exit
0
Drücken Sie eine beliebige Taste . . .
```

14 High Resolution Pictures

(a) Figure 53: TE0320 high resolution top view.

(b) Figure 54: TE0320 high resolution bottom view.

(c) Figure 55: TE0320 angle view.

14.1 Top View

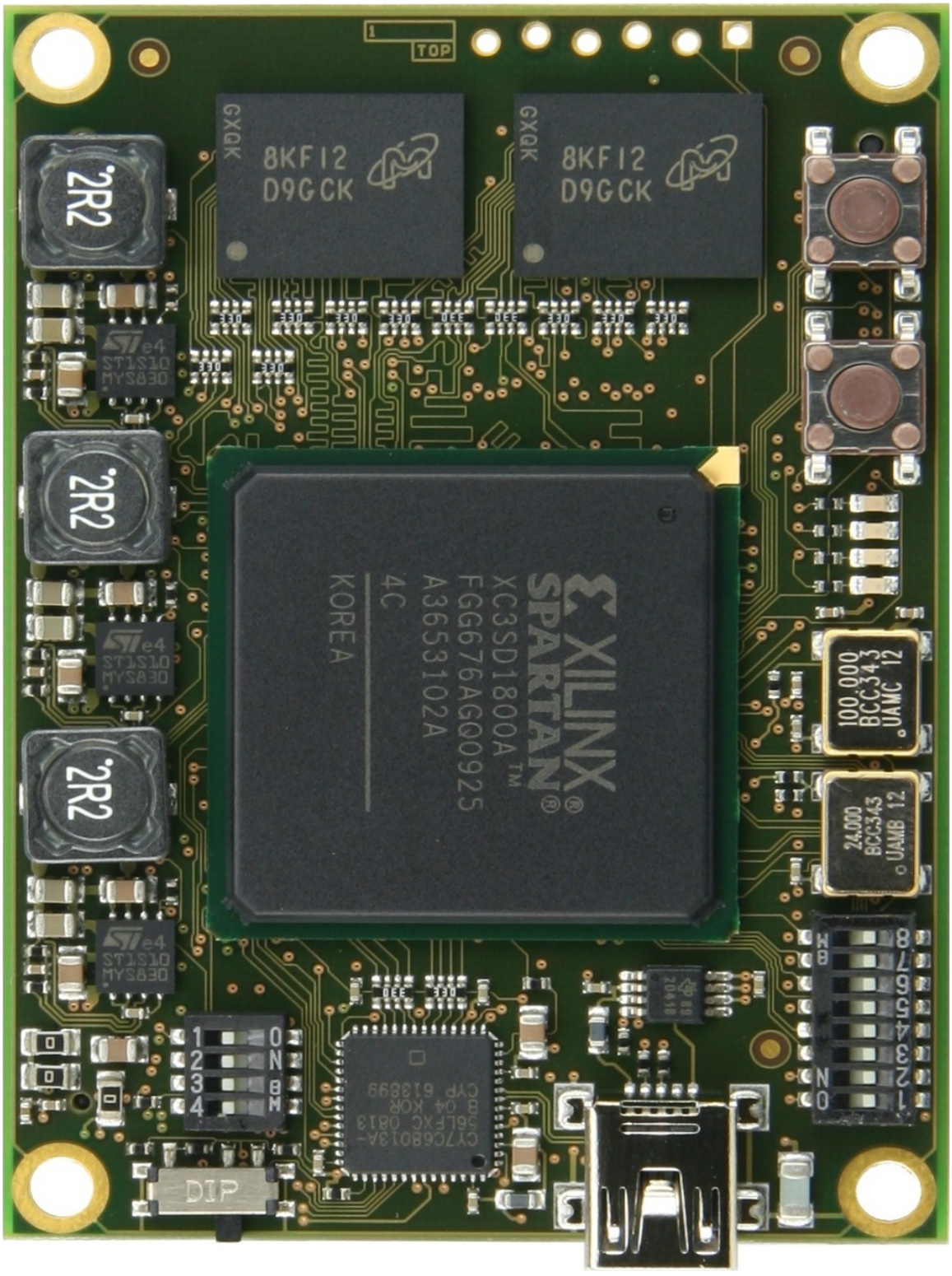


Figure 53: TE0320 high resolution top view.

14.2 Bottom View

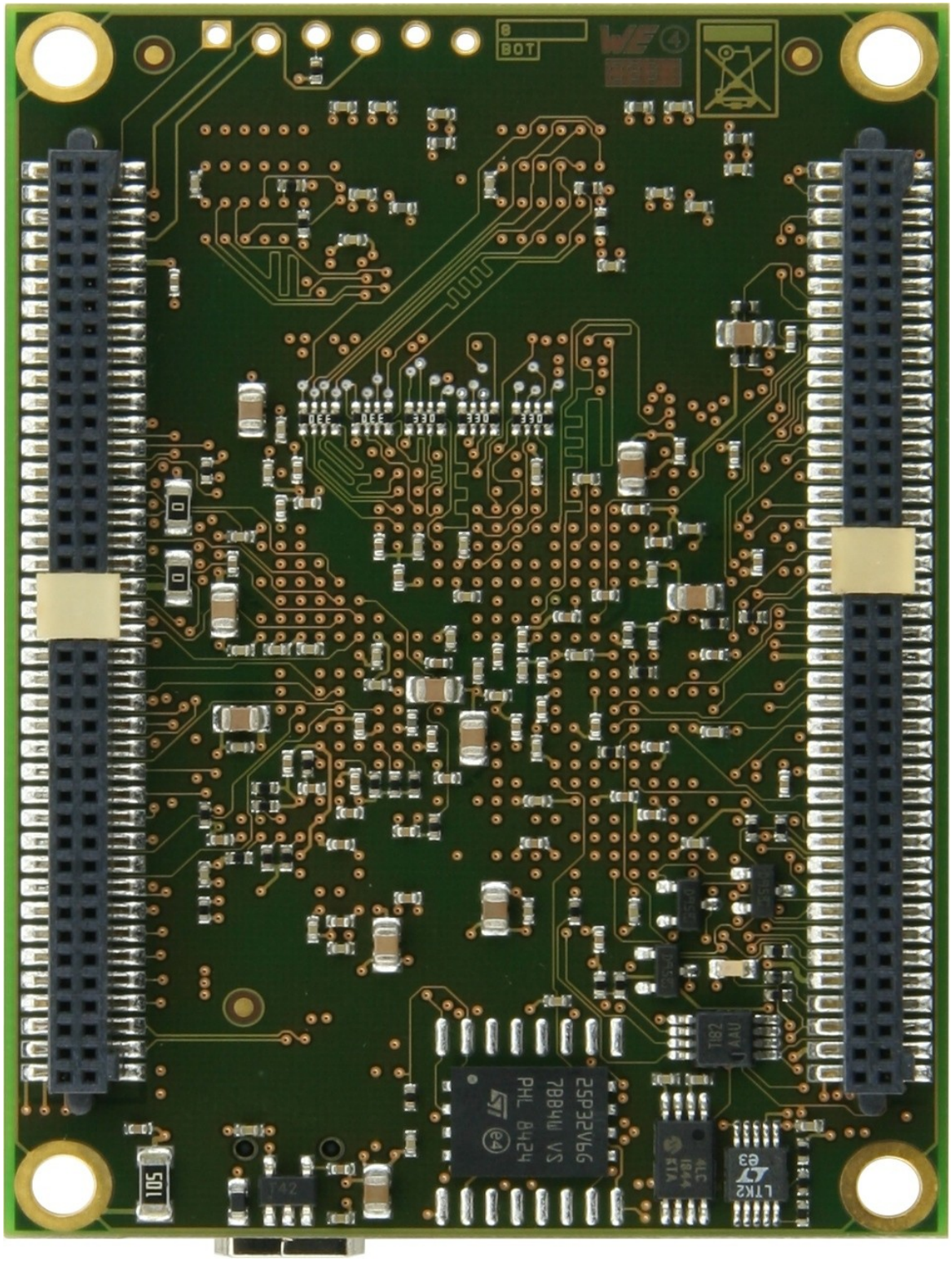


Figure 54: TE0320 high resolution bottom view.

14.3 Angle View

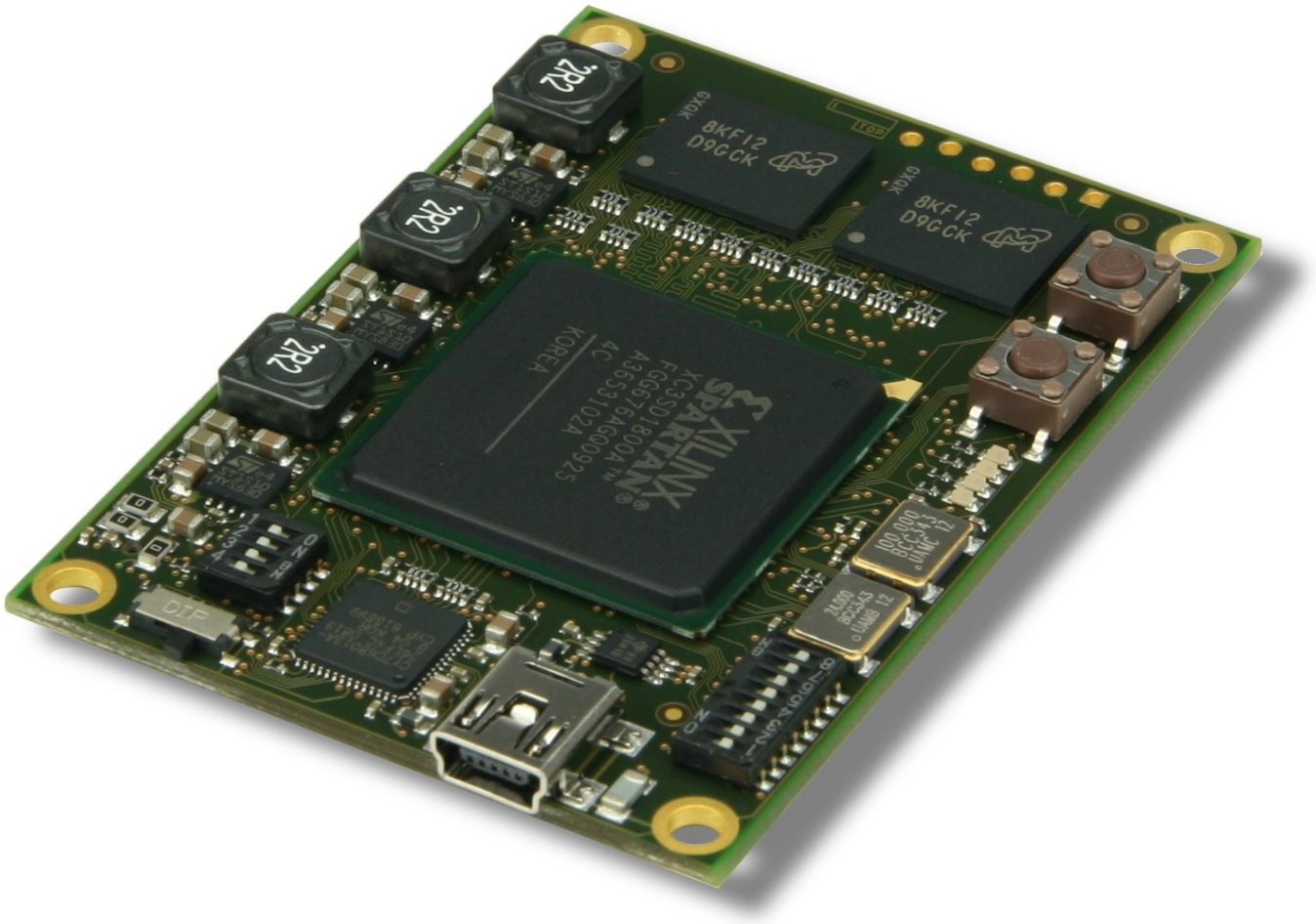


Figure 55: TE0320 angle view.

15 Ordering Information

Boards with other configurations or equipped with industrial temperature grade parts are available on request.

15.1 Product Identification System

Trenz Electronic TE0320 series modules have the following ordering numbers:

TE0320	-	XX	-	Y ... Y
module series		PCB revision		assembly option

15.2 Assembly Options Overview

module	FPGA device	power supply source	VcccIO0	mnemonics
TE0320-00-EV01	XC3SD1800A-4FGG676C	USB	3.3 V	evaluation
TE0320-00-EV02	XC3SD1800A-4FGG676C	B2B	3.3 V	evaluation
TE0320-00-EV02B	XC3SD3400A-4FGG676C	B2B	3.3 V	evaluation, big

Table 34: assembly options overview.

To determine the FPGA device, you just read the code on the package under the "Xilinx Spartan" label.

To determine the power supply source, please see paragraph 5.2 Power Supply Sources.

To determine the VcccIO0 voltage, please see paragraph 5.3 On-Board Power Rails.

To determine PCB revision and assembly variant from FPGA, TE0320 have dedicated user signals, which can be read by user core.

Board revision coded in 4 bits REV[3:0]

Signal name	FPGA pin
REV0	C21
REV1	D21
REV2	E21
REV3	C20

Table 35: Board revision pins

To define low (zero) level REV pin connected to ground rail, to define high (one) level REV pin left float (open). These pins should be configured with "pullup" option in user design.

See Table 12 for current list of board revisions.

REV3	REV2	REV1	REV0	Board revision
1	1	1	1	Revision 00

Table 36: Board revisions

Module assembly variant encoded using VAR[5:0] pins.

Signal name	FPGA pin
VAR0	F17
VAR1	K16
VAR2	J16
VAR3	E17
VAR4	D20
VAR5	A20

Table 37: Assembly variants pins

To define low (zero) level VAR pin connected to ground rail through zero resistor, to define high (one) level VAR pin left float (open). These pins should be configured with "pullup" option in user design.

Available module assembly variants listed in Table 38.

VAR5	VAR4	VAR3	VAR2	VAR1	VAR0	Variant
1	1	1	1	1	1	EV01
1	1	1	1	1	0	EV02

Table 38: Module assembly variants

15.3 Availability

For the latest product details and available options, please visit

www.trenz-electronic.de

To order or obtain information, e.g. on pricing or delivery, please visit:

shop.trenz-electronic.de

16 Product Support

Trenz Electronic provides support via its site at

www.trenz-electronic.de ► support

This web site is used as a means to make files and information easily available to customers. It contains the following information:

- product support
  - data sheets
  - errata
  - application notes
  - sample programs
  - design resources
  - user's guides
  - hardware support documents
  - latest software releases
  - archived software
- general technical support
  - Frequently Asked Questions (FAQ)
  - technical support requests
- business of Trenz Electronic
  - product selector
  - ordering guides
  - latest press releases
  - listing of events
  - listings of business partners
- video archive
  - TrenzElectronic's Channel at YouTube

17 Related Materials and References

The following documents provide supplementary information useful with this user manual.

17.1 Data Sheets

- Xilinx DS485: Digital Clock Manager (DCM) Module Data Sheet
  This is the data sheet for the Digital Clock Manager (DCM) Module core.
  www.xilinx.com/support/documentation/ip_documentation/dcm_module.pdf
- Xilinx DS610: Spartan-3A DSP FPGA Family: Complete Data Sheet
  The Spartan®-3A DSP family of Field-Programmable Gate Arrays (FPGAs) solves the design challenges in most high-volume, cost-sensitive, high-performance DSP applications.
  www.xilinx.com/support/documentation/data_sheets/ds610.pdf

17.2 User Guides

- Xilinx UG331: Spartan-3 Generation FPGA User Guide
  Functional description of the Spartan®-3 generation FPGA architecture and how to use it. Includes the Spartan-3A, Spartan-3AN, Spartan-3A DSP, Spartan-3E, and Spartan-3 platforms.
  www.xilinx.com/support/documentation/user_guides/ug331.pdf
- Xilinx UG332: Spartan-3 Generation Configuration User Guide
  Describes the configuration features of the Spartan®-3 Generation FPGAs. Includes the Spartan-3A, Spartan-3AN, Spartan-3A DSP, Spartan-3E, and Spartan-3 FPGA families.
  www.xilinx.com/support/documentation/user_guides/ug332.pdf
- EZ-USB® Technical Reference Manual (TRM)
  www.cypress.com/?rID=14667

17.3 Tutorials

- (Xilinx) ISE (10.1) In-Depth Tutorial
  Chapter 7: iMPACT Tutorial
  www.xilinx.com/direct/ise10_tutorials/ise10tut.pdf
- Xilinx UG695: ISE In-Depth Tutorial
  Chapter 7: iMPACT Tutorial
  http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/ise11tut.pdf

17.4 Application Notes

- Xilinx XAPP104: A Quick JTAG ISP Checklist
  Most Xilinx CPLDs, PROMs, and FPGAs have an IEEE Standard 1149.1 (JTAG) port. Xilinx devices with a JTAG port are in-system programmable (ISP) through the JTAG port. The ISP feature is beneficial for fast prototype development. This application note describes a short list of considerations needed to get the best performance from your ISP designs.
  www.xilinx.com/support/documentation/application_notes/xapp104.pdf
- Xilinx XAPP974: Indirect Programming of SPI Serial Flash PROMs with Spartan-3A FPGAs

This application note describes how to indirectly program an SPI Serial Flash PROM through the JTAG interface of a Spartan®-3A FPGA using iMPACT 9.1.01i. The hardware setup, software flows for file generation, and programming are also covered.
www.xilinx.com/support/documentation/application_notes/xapp974.pdf

- ISP Standards & Specifications
  Brief descriptions of In-system Programmability (ISP) standards and specifications
  www.xilinx.com/products/design_resources/config_sol/isp_standards_specs.htm

18 B2B Connectors Pin Descriptions

This section describes how the various pins on B2B connectors JM4 and JM5 connect with TE0320 on-board components. In this chapter, most of naming conventions and colour coding scheme are taken from the official Xilinx Spartan-3A DSP documentation.

18.1 Pin Labelling

The pin label is abbreviated but descriptive for each pin. All I/O pins begin with IO. If a pin can be used as a differential signal, the name includes an _Lxxy_b suffix, where

- L indicates that the pin is part of a differential pair
- xx is a two-digit integer, unique for each bank, that identifies a differential pin-pair
- y is the signal polarity and is replaced by P for the positive signal or N for the negative. These two pins form one differential pin-pair
- b is an integer, 0 through 2 for TE0320, indicating the associated I/O bank.

Dual- or multi-purpose pins have a name composed of the signal names referring to each possible pin function (e. g. IO_L52P_2 / D0 / DIN / MISO). _B is used as the active-Low designator, as in CSI_B.

A differential clock input requires two global clock inputs. The P and N inputs follow the same configuration as for standard inputs on those pins. The clock inputs that get paired together are consecutive pins in clock number, an even clock number and the next higher odd value. For example, GCLK0 and GCLK1 are a differential pair.

18.2 Pin Types

Most pins of B2B connectors JM4 and JM5 are general-purpose, user-defined I/O pins (GPIOs). There are, however, up to 9 different functional types of pins on the TE0320, as outlined in Table 39. In pin-out tables 40 and 41, the individual pins are colour-coded according to pin type as in Table 39.

type colour code	description
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. See Xilinx UG332: Spartan-3 Generation Configuration User Guide for additional information on these signals.
VREF	VREF0 provides a reference voltage input for certain I/O standards. See paragraph 6.9 Voltage Reference VREF0 for additional information on this signal.
CLK	Either a user-I/O pin or an input to a specific clock buffer driver. Packages have 16 global clock inputs that optionally clock the entire device. See the Using Global Clock Resources chapter in UG331: Spartan-3 Generation FPGA User Guide for additional information on these signals.
CONFIG	Dedicated configuration pin, two per device. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See Xilinx UG332: Spartan-3 Generation Configuration User Guide for additional information on these signals.
PWRMGMT	Control and status pins for the power-saving Suspend mode. SUSPEND is a dedicated pin and is powered by VCCAUX. AWAKE is a Dual-Purpose pin. Unless Suspend mode is enabled in the application, AWAKE is available as a user-I/O pin.
JTAG	Dedicated JTAG pin - 4 per device. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX.

GND	Dedicated ground pin. All must be connected.
TE	Trenz Electronic specific pin type. See the description of each pin in the user manual for additional information on the corresponding signals.

Table 39: types of pins on TE0320.

18.3 B2B Connectors Pin-Out

18.3.1 JM4 Pin-Out

supply	bank	type	FPGA pin	FPGA ball	JM4 singal	JM4	pin	JM4 singal	FPGA ball	FPGA pin	type	bank	supply
3.3 V	-	out	-	-	3.3V	1	2	GND	-	-	GND	GND	GND
VcccIO0	0	I/O	IO_L20P_0	F15	JM4-IO01	3	4	B2B_D_P	-	-	I/O	-	USB
VcccIO0	0	I/O	IO_L21N_0	C16	JM4-IO02	5	6	B2B_D_N	-	-	I/O	-	USB
GND	GND	GND	-	-	GND	7	8	JM4-IO34	K12	IO_L39N_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L21P_0	D17	JM4-IO03	9	10	JM4-IO35	J12	IO_L39P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L22N_0	C15	JM4-IO04	11	12	JM4-IO36	D8	IO_L40N_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L22P_0	D16	JM4-IO05	13	14	JM4-IO37	C8	IO_L40P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L23N_0	A15	JM4-IO06	15	16	GND	-	-	GND	GND	GND
VcccIO0	0	I/O	IO_L23P_0	B15	JM4-IO07	17	18	JM4-IO38	C6	IO_L41N_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L24N_0	F14	JM4-IO08	19	20	JM4-IO39	B6	IO_L41P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L24P_0	E14	JM4-IO09	21	22	JM4-IO40	C7	IO_L42N_0	I/O	0	VcccIO0
GND	GND	GND	-	-	GND	23	24	JM4-IO41	B7	IO_L42P_0	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L25N_0 GCLK5	J14	JM4-IO10	25	26	JM4-IO42	K11	IO_L43N_0	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L25P_0 GCLK4	K14	JM4-IO11	27	28	JM4-IO43	J11	IO_L43P_0	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L26N_0 GCLK7	A14	JM4-IO12	29	30	VcccIO0	-	-	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L26P_0 GCLK6	B14	JM4-IO13	31	32	JM4-IO44	D6	IO_L44N_0	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L27N_0 GCLK9	G13	JM4-IO14	33	34	JM4-IO45	C5	IO_L44P_0	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L27P_0 GCLK8	F13	JM4-IO15	35	36	JM4-IO46	B4	IO_L45N_0	I/O	0	VcccIO0
VREF	0	in	-	-	VREF0	37	38	JM4-IO47	A4	IO_L45P_0	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L28N_0 GCLK11	C13	JM4-IO16	39	40	JM4-IO48	H10	IO_L46N_0	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L28P_0 GCLK10	B13	JM4-IO17	41	42	JM4-IO49	G10	IO_L46P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L29N_0	B12	JM4-IO18	43	44	VcccIO0	-	-	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L29P_0	A12	JM4-IO19	45	46	JM4-IO50	H9	IO_L47N_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L30N_0	C12	JM4-IO20	47	48	JM4-IO51	G9	IO_L47P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L30P_0	D13	JM4-IO21	49	50	JM4-IO52	E7	IO_L48N_0	I/O	0	VcccIO0
GND	GND	GND	-	-	GND	51	52	JM4-IO53	F7	IO_L48P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L33N_0	B10	JM4-IO22	53	54	JM4-IO54	B3	IO_L51N_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L33P_0	A10	JM4-IO23	55	56	JM4-IO55	A3	IO_L51P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L34N_0	D10	JM4-IO24	57	58	GND	-	-	GND	GND	GND
VcccIO0	0	I/O	IO_L34P_0	C10	JM4-IO25	59	60	JM4-IO56	C23	IO_L06N_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L35N_0	H12	JM4-IO26	61	62	JM4-IO57	D23	IO_L06P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L35P_0	G12	JM4-IO27	63	64	JM4-IO58	A22	IO_L07N_0	I/O	0	VcccIO0
GND	GND	GND	-	-	GND	65	66	JM4-IO59	B23	IO_L07P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L36N_0	B9	JM4-IO28	67	68	JM4-IO60	G17	IO_L08N_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L36P_0	A9	JM4-IO29	69	70	JM4-IO61	H17	IO_L08P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L37N_0	D9	JM4-IO30	71	72	VccAux	-	-	out	VccAux	VccAux
VcccIO0	0	I/O	IO_L37P_0	E10	JM4-IO31	73	74	TDI	G7	TDI	JTAG	VccAux	VccAux
VcccIO0	0	I/O	IO_L38N_0	B8	JM4-IO32	75	76	TDO	E23	TDO	JTAG	VccAux	VccAux
VcccIO0	0	I/O	IO_L38P_0	A8	JM4-IO33	77	78	TCK	D4	TCK	JTAG	VccAux	VccAux
GND	GND	GND	-	-	GND	79	80	TMS	A25	TMS	JTAG	VccAux	VccAux

Table 40: pin-out of B2B connector JM4.

18.3.2 JM5 Pin-Out

supply	bank	type	FPGA pin	FPGA ball	JM5 singal	JM5	pin	JM5 singal	FPGA ball	FPGA pin	type	bank	supply
TE	-	in	-	-	Vb2b	1	2	Vb2b	-	-	in	-	TE
TE	-	in	-	-	Vb2b	3	4	Vb2b	-	-	in	-	TE
3.3V	1	I/O (I2C)	IO_L13P_1	Y22	SCL	5	6	/MR	-	-	in	-	3.3V
3.3V	1	I/O (I2C)	IO_L13N_1	Y23	SDA	7	8	/RESET	A2	PROG_B	in CONFIG	2	VccAux 3.3V
GND	GND	GND	-	-	GND	9	10	DONE	AB21	DONE	out CONFIG	VccAux	VccAux
3.3V	2	I/O DUAL	IO_L22N_2 DOUT	AE15	DOUT	11	12	SPI_D	AB15	IO_L30N_2 MOSI/CSI_B	SPI in DUAL	2	3.3V
3.3V	2	I/O DUAL	IO_L01N_2 M0	AD4	M0	13	14	INIT_B	AA15	IO_L34P_2 INIT_B	I/O DUAL	2	3.3V
3.3V	2	I/O DUAL	IO_L01P_2 M1	AC4	M1	15	16	Vsup	-	-	out	-	TE
3.3V	2	I/O DUAL	IO_L02P_2 M2	Y7	M2	17	18	SPI_Q	AF24	IO_L52P_2 D0/DIN/MISO	SPI out DUAL	2	3.3V
3.3V	2	I/O DUAL	IO_L07P_2 RDWR_B	Y12	RDWR _B	19	20	SPI_/S	AA7	IO_L02N_2 CSO_B	SPI out DUAL	2	3.3V
VccAux	VccAux	in CONFIG	PROG_B	A2	B2B _PROGB	21	22	SPI_/C	AE24	IO_L52N_2 CCLK	SPI out DUAL	2	3.3V
3.3 V	-	out	-	-	3.3V	23	24	D4	AE12	IO_L24N_2 D4	I/O DUAL	2	3.3V
3.3V	2	I/O PWRMGMT	IO_L22P_2 AWAKE	AD15	AWAKE	25	26	D5	AF12	IO_L24P_2 D5	I/O DUAL	2	3.3V
VccAux	VccAux	in PWRMGMT	SUSPEND	V20	SUSPEND	27	28	D6	AF10	IO_L22N_2 D6	I/O DUAL	2	3.3V
3.3V	2	I/O DUAL	IO_L36N_2 D1	AE18	D1	29	30	GND	-	-	GND	GND	GND
3.3V	2	I/O DUAL	IO_L36P_2 D2	AF18	D2	31	32	D7	AE10	IO_L22P_2 D7	I/O DUAL	2	3.3V
3.3V	2	I/O DUAL	IO_L34N_2 D3	Y15	D3	33	34	J5-IO20	AA18	IO_L47N_2	I/O	2	3.3V
3.3V	2	I/O GCLK	IO_L27P_2 GCLK0	Y14	J5-IO01	35	36	J5-IO21	AB18	IO_L47P_2	I/O	2	3.3V
GND	GND	GND	-	-	GND	37	38	J5-IO22	AE23	IO_L48N_2	I/O	2	3.3V
3.3V	2	I/O GCLK	IO_L28P_2 GCLK2	AF14	J5-IO02	39	40	J5-IO23	AF23	IO_L48P_2	I/O	2	3.3V
3.3V	2	I/O	IO_L29N_2	AC14	J5-IO03	41	42	J5-IO24	AE25	IO_L51P_2	I/O	2	3.3V
3.3V	2	I/O	IO_L39N_2	AE20	J5-IO04	43	44	1.2V	-	-	out	-	1.2 V
3.3V	2	I/O	IO_L39P_2	AF20	J5-IO05	45	46	J5-IO25	AF25	IO_L51P_2	I/O	2	3.3V
3.3V	2	I/O	IO_L40N_2	AC19	J5-IO06	47	48	J5-IO26	Y9	IO_L05N_2	I/O	2	3.3V
3.3V	2	I/O	IO_L40P_2	AD19	J5-IO07	49	50	J5-IO27	W9	IO_L05P_2	I/O	2	3.3V
GND	GND	GND	-	-	GND	51	52	J5-IO28	AF3	IO_L06N_2	I/O	2	3.3V
3.3V	2	I/O	IO_L41N_2	AC20	J5-IO08	53	54	J5-IO29	AE3	IO_L06P_2	I/O	2	3.3V
3.3V	2	I/O	IO_L41P_2	AD20	J5-IO09	55	56	J5-IO30	AF4	IO_L07N_2	I/O	2	3.3V
3.3V	2	I/O	IO_L42N_2	U16	J5-IO10	57	58	GND	-	-	GND	GND	GND
3.3V	2	I/O	IO_L42P_2	V16	J5-IO11	59	60	J5-IO31	AE4	IO_L07P_2	I/O	2	3.3V
3.3V	2	I/O	IO_L43N_2	Y17	J5-IO12	61	62	J5-IO32	AD6	IO_L08N_2	I/O	2	3.3V
3.3V	2	I/O	IO_L43P_2	AA17	J5-IO13	63	64	J5-IO33	AC6	IO_L08P_2	I/O	2	3.3V
2.5 V	-	out	-	-	2.5V	65	66	J5-IO34	W10	IO_L09N_2	I/O	2	3.3V
3.3V	2	I/O	IO_L44N_2	AD21	J5-IO14	67	68	J5-IO35	V10	IO_L09P_2	I/O	2	3.3V
3.3V	2	I/O	IO_L44P_2	AE21	J5-IO15	69	70	J5-IO36	Y13	IO_L25N_2 GCLK13	I/O GCLK	2	3.3V
3.3V	2	I/O	IO_L45N_2	AC21	J5-IO16	71	72	GND	-	-	GND	GND	GND
3.3V	2	I/O	IO_L45P_2	AD22	J5-IO17	73	74	J5-IO37	AA13	IO_L25P_2 GCLK12	I/O GCLK	2	3.3V
3.3V	2	I/O	IO_L46N_2	V17	J5-IO18	75	76	J5-IO38	AE13	IO_L26N_2 GCLK15	I/O GCLK	2	3.3V
3.3V	2	I/O	IO_L46P_2	W17	J5-IO19	77	78	J5-IO39	AF13	IO_L26P_2 GCLK14	I/O GCLK	2	3.3V
GND	GND	GND	-	-	GND	79	80	J5-IO40	W13	IO_L20N_2	I/O	2	3.3V

Table 41: pin-out of B2B connector JM5.

18.4 Signal Integrity Considerations

Traces of differential signals pairs are NOT routed symmetrically (as symmetric pairs).

Traces of differential signals pairs are NOT routed with equal length. For applications where traces length has to be matched or timing differences have to be compensated, Table 42 and Table 43 list the trace length of I/O signal lines measured from FPGA balls to B2B connector pins.

Traces of differential signals pairs are routed with a differential impedance between the two traces of 60 ohm.

Pairs of pins that form a differential I/O pair appear colored together in the table. An electronic version of these pin-out tables are available for download from the Trenz Electronic support area of the web site.

18.4.1 JM4 Signals Trace Length

len. mm	FPGA pin	FPGA ball	JM4 singal	JM4	pin	JM4 singal	FPGA ball	FPGA pin	len. mm
				1	2				
26	IO_L20P_0	F15	JM4-IO01	3	4				
29	IO_L21N_0	C16	JM4-IO02	5	6				
				7	8	JM4-IO34	K12	IO_L39N_0	29
26	IO_L21P_0	D17	JM4-IO03	9	10	JM4-IO35	J12	IO_L39P_0	26
24	IO_L22N_0	C15	JM4-IO04	11	12	JM4-IO36	D8	IO_L40N_0	26
26	IO_L22P_0	D16	JM4-IO05	13	14	JM4-IO37	C8	IO_L40P_0	24
21	IO_L23N_0	A15	JM4-IO06	15	16				
20	IO_L23P_0	B15	JM4-IO07	17	18	JM4-IO38	C6	IO_L41N_0	24
22	IO_L24N_0	F14	JM4-IO08	19	20	JM4-IO39	B6	IO_L41P_0	24
18	IO_L24P_0	E14	JM4-IO09	21	22	JM4-IO40	C7	IO_L42N_0	23
				23	24	JM4-IO41	B7	IO_L42P_0	19
20	IO_L25N_0 GCLK5	J14	JM4-IO10	25	26	JM4-IO42	K11	IO_L43N_0	24
21	IO_L25P_0 GCLK4	K14	JM4-IO11	27	28	JM4-IO43	J11	IO_L43P_0	23
11	IO_L26N_0 GCLK7	A14	JM4-IO12	29	30				
11	IO_L26P_0 GCLK6	B14	JM4-IO13	31	32	JM4-IO44	D6	IO_L44N_0	15
17	IO_L27N_0 GCLK9	G13	JM4-IO14	33	34	JM4-IO45	C5	IO_L44P_0	14
16	IO_L27P_0 GCLK8	F13	JM4-IO15	35	36	JM4-IO46	B4	IO_L45N_0	15
				37	38	JM4-IO47	A4	IO_L45P_0	14
13	IO_L28N_0 GCLK11	C13	JM4-IO16	39	40	JM4-IO48	H10	IO_L46N_0	14
12	IO_L28P_0 GCLK10	B13	JM4-IO17	41	42	JM4-IO49	G10	IO_L46P_0	14
14	IO_L29N_0	B12	JM4-IO18	43	44				
14	IO_L29P_0	A12	JM4-IO19	45	46	JM4-IO50	H9	IO_L47N_0	15
27	IO_L30N_0	C12	JM4-IO20	47	48	JM4-IO51	G9	IO_L47P_0	14
30	IO_L30P_0	D13	JM4-IO21	49	50	JM4-IO52	E7	IO_L48N_0	13
				51	52	JM4-IO53	F7	IO_L48P_0	15
20	IO_L33N_0	B10	JM4-IO22	53	54	JM4-IO54	B3	IO_L51N_0	9
17	IO_L33P_0	A10	JM4-IO23	55	56	JM4-IO55	A3	IO_L51P_0	9
20	IO_L34N_0	D10	JM4-IO24	57	58				
21	IO_L34P_0	C10	JM4-IO25	59	60	JM4-IO56	C23	IO_L06N_0	36
29	IO_L35N_0	H12	JM4-IO26	61	62	JM4-IO57	D23	IO_L06P_0	42
30	IO_L35P_0	G12	JM4-IO27	63	64	JM4-IO58	A22	IO_L07N_0	36
				65	66	JM4-IO59	B23	IO_L07P_0	41
27	IO_L36N_0	B9	JM4-IO28	67	68	JM4-IO60	G17	IO_L08N_0	36
27	IO_L36P_0	A9	JM4-IO29	69	70	JM4-IO61	H17	IO_L08P_0	39
28	IO_L37N_0	D9	JM4-IO30	71	72				
34	IO_L37P_0	E10	JM4-IO31	73	74				
29	IO_L38N_0	B8	JM4-IO32	75	76				
28	IO_L38P_0	A8	JM4-IO33	77	78				
				79	80				

Table 42: trace length of signal pins of B2B connector JM4.

18.4.2 JM5 Signals Trace Length

len. mm	FPGA pin	FPGA ball	JM5 singal	JM5	pin	JM5 singal	FPGA ball	FPGA pin	len. mm
				1	2				
				3	4				
				5	6				
				7	8				
				9	10				
21	IO_L22N_2 DOUT	AE15	DOUT	11	12	SPI_D	AB15	IO_L30N_2 MOSI/CSI_B	51
35	IO_L01N_2 M0	AD4	M0	13	14	INIT_B	AA15	IO_L34P_2 INIT_B	51
49	IO_L01P_2 M1	AC4	M1	15	16				
49	IO_L02P_2 M2	Y7	M2	17	18	SPI_Q	AF24	IO_L52P_2 D0/DIN/MISO	52
23	IO_L17P_2 RDWR_B	Y12	RDWR _B	19	20	SPI_/S	AA7	IO_L02N_2 CSO_B	95
				21	22	SPI_/C	AE24	IO_L52N_2 CCLK	75
				23	24	D4	AE12	IO_L24N_2 D4	14
10	IO_L22P_2 AWAKE	AD15	AWAKE	25	26	D5	AF12	IO_L24P_2 D5	13
				27	28	D6	AF10	IO_L22N_2 D6	15
7	IO_L36N_2 D1	AE18	D1	29	30				
7	IO_L36P_2 D2	AF18	D2	31	32	D7	AE10	IO_L22P_2 D7	16
13	IO_L34N_2 D3	Y15	D3	33	34	J5-IO20	AA18	IO_L47N_2	22
13	IO_L27P_2 GCLK0	Y14	J5-IO01	35	36	J5-IO21	AB18	IO_L47P_2	16
				37	38	J5-IO22	AE23	IO_L48N_2	20
9	IO_L28P_2 GCLK2	AF14	J5-IO02	39	40	J5-IO23	AF23	IO_L48P_2	23
12	IO_L29N_2	AC14	J5-IO03	41	42	J5-IO24	AE25	IO_L51P_2	26
17	IO_L39N_2	AE20	J5-IO04	43	44				
19	IO_L39P_2	AF20	J5-IO05	45	46	J5-IO25	AF25	IO_L51P_2	34
21	IO_L40N_2	AC19	J5-IO06	47	48	J5-IO26	Y9	IO_L05N_2	20
22	IO_L40P_2	AD19	J5-IO07	49	50	J5-IO27	W9	IO_L05P_2	20
				51	52	J5-IO28	AF3	IO_L06N_2	10
27	IO_L41N_2	AC20	J5-IO08	53	54	J5-IO29	AE3	IO_L06P_2	11
26	IO_L41P_2	AD20	J5-IO09	55	56	J5-IO30	AF4	IO_L07N_2	11
27	IO_L42N_2	U16	J5-IO10	57	58				
30	IO_L42P_2	V16	J5-IO11	59	60	J5-IO31	AE4	IO_L07P_2	17
36	IO_L43N_2	Y17	J5-IO12	61	62	J5-IO32	AD6	IO_L08N_2	21
36	IO_L43P_2	AA17	J5-IO13	63	64	J5-IO33	AC6	IO_L08P_2	26
				65	66	J5-IO34	W10	IO_L09N_2	31
44	IO_L44N_2	AD21	J5-IO14	67	68	J5-IO35	V10	IO_L09P_2	38
39	IO_L44P_2	AE21	J5-IO15	69	70	J5-IO36	Y13	IO_L25N_2 GCLK13	43
43	IO_L45N_2	AC21	J5-IO16	71	72				
47	IO_L45P_2	AD22	J5-IO17	73	74	J5-IO37	AA13	IO_L25P_2 GCLK12	40
44	IO_L46N_2	V17	J5-IO18	75	76	J5-IO38	AE13	IO_L26N_2 GCLK15	32
45	IO_L46P_2	W17	J5-IO19	77	78	J5-IO39	AF13	IO_L26P_2 GCLK14	35
				79	80	J5-IO40	W13	IO_L20N_2	44

Table 43: trace length of signal pins of B2B connector JM5.

19 Glossary of Abbreviations and Acronyms

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

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API	application programming interface
B2B	board-to-board
DSP	digital signal processing; digital signal processor
EDK	Embedded Development Kit
FUT	Firmware Upgrade Tool
FWU	Firmware Upgrade file
IOB	input / output blocks; I/O blocks
IP	intellectual property
ISP	In-System Programmability
PB	push button
SDK	Software Development Kit
TE	Trenz Electronic
XPS	Xilinx Platform Studio

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21 Document Change History

ver.	date	author	description
1.00	2009-10-22	FDR	Release.
2.00	2009-12-16	FDR	Added USB over B2B connector. Added S1 description. Added JTAG interface. Added I2C bus description. Added SPI bus description. Added VREF0 description. Added LEDs, buttons and switches description. Added clock networks. Added on-board memories description. Added mode select pins. Added configuration options. Improved Bootload.ini file description. Added YouTube reference to product support. Added JM4 and JM5 pin-out tables. Added signal integrity considerations. Improved system requirements. Added glossary Introduced some other minor changes.
2.01	2010-01-18	FDR	Updated number of FPGA I/O pins. Removed TE0320-00B-EV01.
2.02	2010-01-19	FDR	Updated some software package paths. Corrected pin name of JM5 signal RDWR_B (ball Y12). SPI_/S and SPI_/C pins of connector JM5 were swapped in pin-out and trace length tables.
2.03	2010-01-20	FDR	Added legal notices.
2.04	2010-05-17	FDR	Added reference design summaries. Added SPI pin-out summary. Improved assembly options overview.
2.05	2010-05-18	FDR	Added indirect SPI configuration mode
2.06	2010-05-19	FDR	Improved JM5 pin-out: configuration and power management pins.
2.08	2012-02-22	FDR	Improved push buttons description. Corrected slide-switch positions.
2.08	2011-10-03	AIK	Modified block diagram. Added power supply diagram. Little fixes.
2.09	2011-10-05	AIK	Modified B2B section. Changed DDR and SPI specification.
2.10	2011-11-30	AIK	Clarification of SPI Flash options
2.11	2011-12-01	AIK	Board revision and assembly options chapter
2.12	2012-02-16	AIK	Module options chapter
2.13	2012-02-22	AIK	Dimensions image and description modifications
2.14	2012-02-22	AIK	Updated S1 switch description