SPECIFICATION

SPEC. No. H-General-b

D A T E : 2014 May

To

Non-Controlled Copy

CUSTOMER'S PRODUCT NAME	TDK PRODUCT NAME MULTILAYER CERAMIC CHIP CAPACITORS CGJ Series / High Reliability Grade General (Up to 50V) Mid voltage (100 to 630V)

Please return this specification to TDK representatives.
If orders are placed without returned specification, please allow us to judge that specification is accepted by your side.

RECEIPT CONFIRMATION

DATE: YEAR MONTH DAY

TDK Corporation
Sales
Electronic Components
Sales & Marketing Group

TDK-EPC Corporation
Engineering
Ceramic Capacitors Business Group

APPROVED	Person in charge

APPROVED	CHECKED	Person in charge

1. SCOPE

This specification is applicable to chip type multilayer ceramic capacitors with a priority over the other relevant specification.
Manufacturing places defined in this specification shall be TDK-EPC Corporation Japan, and TDK Components USA. Inc.
TDK's CGJ Series MLCC provides an extended life MLCC that meets electrical, mechanical and environmental performance standards from AEC Q200 Rev.D.
Details are referenced within section 7 of this specification.
In addition to our highest quality MLCC, the customer will also receive access to an on-line Sigma Report and internet based product authentication for each lot (which includes electrical characterization data, and estimated product life, as well as anti-counterfeit packaging).
Additionally RFID (radio frequency identification) tags are available as an option.

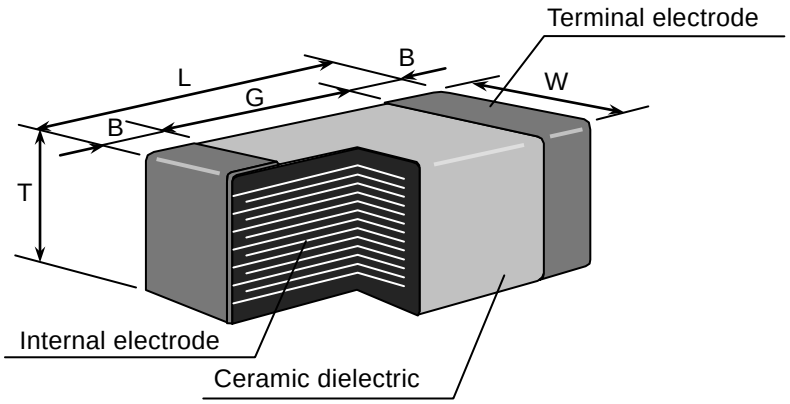
EXPLANATORY NOTE:
This specification warrant the quality of the ceramic chip capacitor. The chips should be evaluated or confirmed a state of mounted on your product.
If the use of the chips go beyond the bounds of this specification, we can not afford to guarantee.

2. CODE CONSTRUCTION

(Example)

Catalog Number :	CGJ2	B	2	X7R	1 C	104	K	050	B	A
(Web)	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)
Item Description :	CGJ2	B	2	X7R	1 C	104	K	T	xxxx	
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(11)	(12)	

(1) Type



Please refer to product list on the web catalog, for the dimension of each product.

(2) Thickness

* As for dimension tolerance, please contact with our sales representative.

Thickness	Dimension (mm)
B	0.50
C	0.60
E	0.80
F	0.85
H	1.15
J	1.25
K	1.30
L	1.60
M	2.00
N	2.30
P	2.50

(3) Guaranteed life test condition

(Details are shown in 7.PERFORMANCE No.21)

Sign	Condition
1	Rated Voltage x 1
2	Rated Voltage x 2
3	Rated Voltage x 1.5
4	Rated Voltage x 1.2

(4) Temperature Characteristics (Details are shown in 7.PREFORMANCE No.8, 9)

(5) Rated Voltage

Symbol	Rated Voltage
2 H	DC 500 V
2 D	DC 200 V
2 A	DC 100 V
1 H	DC 50 V
1 E	DC 25 V
1 C	DC 16 V
1 A	DC 10 V
0 J	DC 6.3 V

(6) Rated Capacitance

Stated in three digits and in units of pico farads (pF).
The first and Second digits identify the first and second significant figures of the capacitance, the third digit identifies the multiplier.
R is designated for a decimal point.

Example 104 → 100,000pF

(7) Capacitance tolerance

Symbol	Tolerance
J	± 5 %
K	± 10 %
M	± 20 %

(8) Thickness code (Only Catalog Number)

(9) Package code (Only Catalog Number)

(10) Special code (Only Catalog Number)

(11) Packaging (Only Item Description)

Symbol	Packaging
T	Taping

(12) Internal code (Only Item Description)

3. RATED CAPACITANCE AND TOLERANCE

3.1 Standard combination of rated capacitance and tolerances

Class	Temperature Characteristics	Capacitance tolerance		Rated capacitance
1	C0G	10pF and under	C (±0.25pF)	1, 1.5, 2, 2.2, 3, 3.3, 4, 4.7, 5
			D (±0.5pF)	6, 6.8, 7, 8, 9, 10
		12pF to 10,000pF	J (± 5 %) K (± 10 %)	E – 12 series
		Over 10,000pF	J (± 5 %) K (± 10 %)	E – 6 series
2	X7R X7S X7T	K (± 10 %) M (± 20 %)		E – 6 series

3.2 Capacitance Step in E series

E series	Capacitance Step											
E- 6	1.0		1.5		2.2		3.3		4.7		6.8	
E-12	1.0	1.2	1.5	1.8	2.2	2.7	3.3	3.9	4.7	5.6	6.8	8.2

4. OPERATING TEMPERATURE RANGE

T.C.	Min. operating Temperature	Max. operating Temperature	Reference Temperature
C0G X7R X7S X7T	-55°C	125°C	25°C

5. STORING CONDITION AND TERM

5 to 40°C at 20 to 70%RH
6 months Max.

6. ENVIRONMENTAL ISSUE

(1) Environmental Conscious Product

This product does not use chemical substances whose use is restricted by the RoHS Directive of End of Life Vehicle (ELV) Directive.
TDK's MLCC capacitors are lead free and conform to the RoHS and REACH directives.
TDK's MLCC do not contain any listed or banned substances nor does TDK use any of the banned substances listed during manufacturing.

(2) INDUSTRIAL WASTE DISPOSAL

Dispose this product as industrial waste in accordance with local industrial waste law.

7. PERFORMANCE

table 1

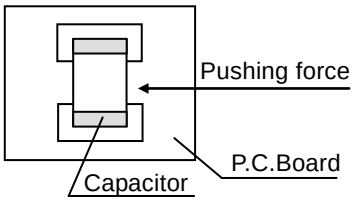
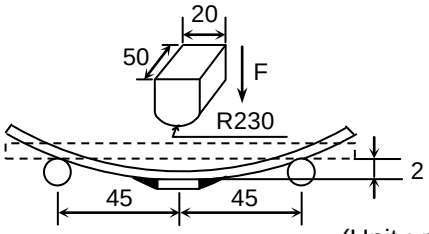
<table>
<tr><th>No.</th><th>Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td>1</td><td>External Appearance</td><td>No defects which may affect performance.</td><td>Inspect with magnifying glass (3×).</td></tr>
<tr><td>2</td><td>Destructive Physical Analysis</td><td>No defects or abnormalities.</td><td>Per EIA-469</td></tr>
<tr><td>3</td><td>Insulation Resistance</td><td>10,000MΩ or 500MΩ·μF min.
(As for the capacitors of rated voltage 16V DC and the item below, 10,000 MΩ or 100MΩ·μF min.,) whichever smaller.</td><td>Apply rated voltage for 60s.</td></tr>
<tr><td>4</td><td>Voltage Proof</td><td>Withstand test voltage without insulation breakdown or other damage.</td><td>
<table>
<tr><th>Class</th><th>Rated voltage</th><th>Apply voltage</th></tr>
<tr><td rowspan="2">Class1</td><td>100V and under</td><td>3 × rated voltage</td></tr>
<tr><td>Over 100V</td><td>1.5 × rated voltage</td></tr>
<tr><td rowspan="2">Class2</td><td>100V and under</td><td>2.5 × rated voltage</td></tr>
<tr><td>Over 100V</td><td>1.5 × rated voltage</td></tr>
</table>
Above DC voltage shall be applied for 1 to 5s.
Charge / discharge current shall not exceed 50mA.</td></tr>
<tr><td>5</td><td>Capacitance</td><td>Within the specified tolerance.</td><td>
<table>
<tr><th>Class</th><th>Capacitance</th><th>Measuring frequency</th><th>Measuring voltage</th></tr>
<tr><td rowspan="2">Class1</td><td>1000pF and under</td><td>1MHz±10%</td><td rowspan="2">0.5 - 5Vrms.</td></tr>
<tr><td>Over 1000pF</td><td>1kHz±10%</td></tr>
<tr><td rowspan="2">Class2</td><td rowspan="2">10uF and under</td><td rowspan="2">1kHz±10%</td><td>0.5±0.2Vrms</td></tr>
<tr><td>1.0±0.2Vrms</td></tr>
<tr><td>Over 10uF</td><td>120Hz±20%</td><td>0.5±0.2Vrms.</td></tr>
</table>
For information which product has which measuring voltage, please contact with our sales representative.</td></tr>
<tr><td>6</td><td>Q
(Class1)</td><td>
<table>
<tr><th>Capacitance</th><th>Q</th></tr>
<tr><td>30pF and over</td><td>1,000 min.</td></tr>
<tr><td>Under 30pF</td><td>400+20×C min.</td></tr>
</table>
C : Rated capacitance (pF)</td><td>See No.5 in this table for measuring condition.</td></tr>
<tr><td>7</td><td>Dissipation Factor
(Class2)</td><td>0.025 max.
0.03 max.
0.05 max.
0.075 max.
For information which product has which Dissipation Factor, please contact with our sales representative.</td><td>See No.5 in this table for measuring condition.</td></tr>
<tr><td>8</td><td>Temperature Characteristics of Capacitance
(Class1)</td><td>
<table>
<tr><th>T.C.</th><th>Temperature Coefficient</th></tr>
<tr><td>C0G</td><td>0 ± 30 (ppm/°C)</td></tr>
</table>
Capacitance drift within ± 0.2% or ± 0.05pF, whichever larger.</td><td>Temperature Coefficient shall be calculated based on values at 25°C and 125°C temperature. The capacitance should be within the tolerance below.
<table>
<tr><th colspan="4">Capacitance change from 25℃(%)</th></tr>
<tr><th colspan="2">-55°C</th><th colspan="2">125°C</th></tr>
<tr><th>Max.</th><th>Min.</th><th>Max.</th><th>Min.</th></tr>
<tr><td>0.58</td><td>-0.24</td><td>0.30</td><td>-0.30</td></tr>
</table></td></tr>
</table>

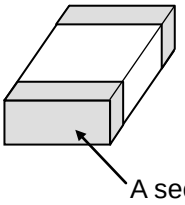
(continued)

<table>
<tr><th>No.</th><th>Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td>9</td><td>Temperature Characteristics of Capacitance (Class2)</td><td>Capacitance Change (%)
No voltage applied

X7R : ± 15

X7S : ± 22

X7T : +22
-33</td><td>Capacitance shall be measured by the steps shown in the following table after thermal equilibrium is obtained for each step.
ΔC be calculated ref. STEP3 reading
<table><tr><th>Step</th><th>Temperature(°C)</th></tr><tr><td>1</td><td>Reference temp. ± 2</td></tr><tr><td>2</td><td>Min. operating temp. ± 2</td></tr><tr><td>3</td><td>Reference temp. ± 2</td></tr><tr><td>4</td><td>Max. operating temp. ± 2</td></tr></table>
Measuring voltage : 0.1, 0.2, 0.5, 1.0Vrms.
For information which product has which Measuring voltage, please contact with our sales representative.</td></tr>
<tr><td>10</td><td>Robustness of Terminations</td><td>No sign of termination coming off, breakage of ceramic, or other abnormal signs.</td><td>Reflow solder the capacitors on a P.C.Board shown in Appendix 1a or Appendix 1b and apply a pushing force of 17.7N with 10±1s.
(2N is applied for CGJ2 type)
 
</td></tr>
<tr><td>11</td><td>Bending</td><td>No mechanical damage.
Capacitance change from initial value should be within 12.5% (Class2) and 5% (Class1).</td><td>Reflow solder the capacitors on a P.C.Board shown in Appendix 2a or Appendix 2b and bend it for 2mm.
 

(Unit : mm)</td></tr>
<tr><td>12</td><td>Solderability</td><td>New solder to cover over 95% of termination.
5% may have pin holes or rough spots but not concentrated in one spot.
Ceramic surface of A sections shall not be exposed due to melting or shifting of termination material.
 
</td><td>Method a)
Preheat:155°C, dry heat for 4h.
Soak terminations in the solder 235°C for 5 (-0.5) sec.

Method b)
Preheat:93±3°C, steam aging for 8h.
Soak terminations in the solder 215°C for 5 (-0.5) sec.

Method c)
Preheat:93±3°C, steam aging for 8h.
Soak terminations in the solder 260°C for 7 ± 0.5 sec.</td></tr>
</table>

(continued)

<table>
<tr><th>No.</th><th colspan="2">Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td rowspan="6">13</td><td rowspan="6">Resistance to solder heat</td><td>External appearance</td><td>No cracks are allowed and terminations shall be covered at least 60% with new solder.</td><td rowspan="6">Completely soak both terminations in solder at 260±5°C for 10±1s.

Preheating condition
Temp. : 150±10°C
Time : 1 to 2min.

Flux : Isopropyl alcohol (JIS K 8839)
Rosin (JIS K 5902) 25% solid solution.

Solder : H63A (JIS Z 3282)

Leave the capacitors in ambient condition for 6 to 24h (Class1) or 24±2h (Class2) before measurement.</td></tr>
<tr><td>Capacitance</td><td><table><tr><th colspan="2">Characteristics</th><th>Change from the value before test</th></tr><tr><td>Class1</td><td>C0G</td><td>Capacitance drift within ± 2.5% or ± 0.25pF, whichever larger.</td></tr><tr><td>Class2</td><td>X7R
X7S
X7T</td><td>± 7.5 %</td></tr></table></td></tr>
<tr><td>Q
(Class1)</td><td><table><tr><th>Capacitance</th><th>Q</th></tr><tr><td>30pF and over</td><td>1,000 min.</td></tr><tr><td>Under 30pF</td><td>400+20×C min.</td></tr></table>C : Rated capacitance (pF)</td></tr>
<tr><td>D.F.
(Class2)</td><td>Meet the initial spec.</td></tr>
<tr><td>Insulation Resistance</td><td>Meet the initial spec.</td></tr>
<tr><td>Voltage proof</td><td>No insulation breakdown or other damage.</td></tr>
<tr><td rowspan="5">14</td><td rowspan="5">Vibration</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="5">Reflow solder the capacitors on a P.C.Board shown in Appendix 1a or Appendix 1b before testing.

Vibrate the capacitor with following conditions.

Applied force : 5G max.
Frequency : 10-2000Hz
Duration : 20 min.
Cycle : 12 cycles</td></tr>
<tr><td>Capacitance</td><td><table><tr><th colspan="2">Characteristics</th><th>Change from the value before test</th></tr><tr><td>Class1</td><td>C0G</td><td>Capacitance drift within ± 2.5% or ± 0.25pF, whichever larger.</td></tr><tr><td>Class2</td><td>X7R
X7S
X7T</td><td>± 7.5 %</td></tr></table></td></tr>
<tr><td>Q
(Class1)</td><td><table><tr><th>Capacitance</th><th>Q</th></tr><tr><td>30pF and over</td><td>1,000 min.</td></tr><tr><td>Under 30pF</td><td>400+20×C min.</td></tr></table>C : Rated capacitance (pF)</td></tr>
<tr><td>D.F.
(Class2)</td><td>Meet the initial spec.</td></tr>
</table>

(continued)

<table>
<tr><th>No.</th><th colspan="2">Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td rowspan="5">15</td><td rowspan="5">Mechanical Shock</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="5">Apply three shocks along 3 mutually Perpendicular axes of the capacitors. (18 shocks)

Test pulse : Half-sine
Duration : 0.5m
Force Peak : 1500G
Velocity change : 4.7m/s</td></tr>
<tr><td>Capacitance</td><td>
<table>
<tr><th colspan="2">Characteristics</th><th>Change from the value before test</th></tr>
<tr><td rowspan="2">Class1</td><td>C0G</td><td>Capacitance drift within ± 2.5% or ± 0.25pF, whichever larger.</td></tr>
<tr><td>X7R
X7S
X7T</td><td>± 7.5 %</td></tr>
</table>
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<tr><td>Q
(Class1)</td><td>
<table>
<tr><th>Capacitance</th><th>Q</th></tr>
<tr><td>30pF and over</td><td>1,000 min.</td></tr>
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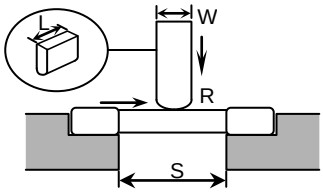
</table>
C : Rated capacitance (pF)
</td></tr>
<tr><td>D.F.
(Class2)</td><td>Meet the initial spec.</td></tr>
<tr><td>Insulation Resistance</td><td>Meet the initial spec.</td></tr>
<tr><td>16</td><td colspan="2">Beam Load</td><td>Breaking strength will be reported during qualification or per customer request.</td><td>Place the capacitor in the beam load fixture and apply force.
 

Force speed : 2.5±0.25mm/s
Jig : R 0.5mm
L 6mm
W 1mm (In case S < 1, W=0.75mm)
S 55% the nominal length of the component tested.</td></tr>
<tr><td rowspan="5">17</td><td rowspan="5">ESD</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="5">AEC-Q200-002, Human Body Model

Max. ESD voltage passed will be reported during qualification or per customer request.</td></tr>
<tr><td>Capacitance</td><td>
<table>
<tr><th colspan="2">Characteristics</th><th>Change from the value before test</th></tr>
<tr><td rowspan="2">Class1</td><td>C0G</td><td>Capacitance drift within ± 2.5% or ± 0.25pF, whichever larger.</td></tr>
<tr><td>X7R
X7S
X7T</td><td>± 7.5 %</td></tr>
</table>
</td></tr>
<tr><td>Q
(Class1)</td><td>
<table>
<tr><th>Capacitance</th><th>Q</th></tr>
<tr><td>30pF and over</td><td>1,000 min.</td></tr>
<tr><td>Under 30pF</td><td>400+20×C min.</td></tr>
</table>
C : Rated capacitance (pF)
</td></tr>
<tr><td>D.F.
(Class2)</td><td>Meet the initial spec.</td></tr>
<tr><td>Insulation Resistance</td><td>Meet the initial spec.</td></tr>
</table>

(continued)

<table>
<tr><th>No.</th><th colspan="2">Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td rowspan="6">18</td><td rowspan="6">High Temp. Exposure (Storage)</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="6">Reflow solder the capacitors on a P.C.Board shown in Appendix 1a or Appendix 1b before testing.

Test condition : 125±3°C for 1,000±12h.

Leave the capacitors in ambient condition for 6 to 24h (Class 1) or 24±2h (Class 2) before measurement.</td></tr>
<tr><td>Capacitance</td><td><table><tr><th colspan="2">Characteristics</th><th>Change from the value before test</th></tr><tr><td>Class1</td><td>C0G</td><td>Capacitance drift within ± 2.5% or ± 0.25pF, whichever larger.</td></tr><tr><td>Class2</td><td>X7R
X7S
X7T</td><td>± 7.5 %</td></tr></table></td></tr>
<tr><td>Q
(Class1)</td><td><table><tr><th>Capacitance</th><th>Q</th></tr><tr><td>30pF and over</td><td>1,000 min.</td></tr><tr><td>Under 30pF</td><td>400+20×C min.</td></tr></table>C : Rated capacitance (pF)</td></tr>
<tr><td>D.F.
(Class2)</td><td>Meet the initial spec.</td></tr>
<tr><td>Insulation Resistance</td><td>Meet the initial spec.</td></tr>
<tr><td>Voltage proof</td><td>No insulation breakdown or other damage.</td></tr>
<tr><td rowspan="6">19</td><td rowspan="6">Temperature cycle</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="6">Reflow solder the capacitors on a P.C.Board shown in Appendix 1a or Appendix 1b before testing.

Expose the capacitors in the condition step1 through step 4 and repeat 1000 times consecutively.

Leave the capacitors in ambient condition for 6 to 24h (Class 1) or 24±2h (Class 2) before measurement.
<table><tr><th>Step</th><th>Temperature(°C)</th><th>Time (min.)</th></tr><tr><td>1</td><td>Min. operating temp. ±3</td><td>30 ± 3</td></tr><tr><td>2</td><td>Reference Temp. ±2</td><td>2 - 5</td></tr><tr><td>3</td><td>Max. operating temp. ±2</td><td>30 ± 2</td></tr><tr><td>4</td><td>Reference Temp. ±2</td><td>2 - 5</td></tr></table></td></tr>
<tr><td>Capacitance</td><td><table><tr><th colspan="2">Characteristics</th><th>Change from the value before test</th></tr><tr><td>Class1</td><td>C0G</td><td>Capacitance drift within ± 2.5% or ± 0.25pF, whichever larger.</td></tr><tr><td>Class2</td><td>X7R
X7S
X7T</td><td>± 7.5 %</td></tr></table></td></tr>
<tr><td>Q
(Class1)</td><td><table><tr><th>Capacitance</th><th>Q</th></tr><tr><td>30pF and over</td><td>1,000 min.</td></tr><tr><td>Under 30pF</td><td>400+20×C min.</td></tr></table>C : Rated capacitance (pF)</td></tr>
<tr><td>D.F.
(Class2)</td><td>Meet the initial spec.</td></tr>
<tr><td>Insulation Resistance</td><td>Meet the initial spec.</td></tr>
<tr><td>Voltage proof</td><td>No insulation breakdown or other damage.</td></tr>
</table>

(continued)

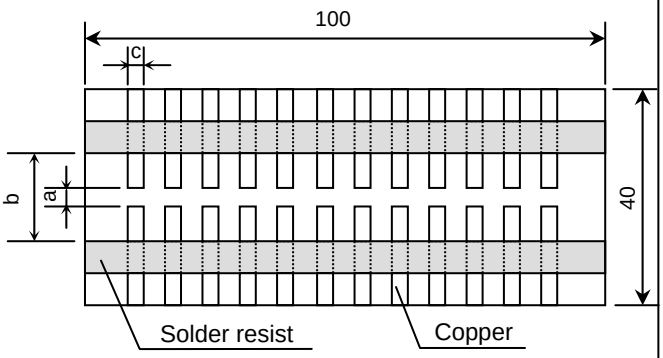
<table>
<tr><th>No.</th><th colspan="2">Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td>20</td><td>Biased Humidity</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="5">Reflow solder the capacitors on a P.C.Board shown in Appendix 1a or Appendix 1b before testing.
Apply the rated voltage at temperature 85°C and 85%RH for 1000 +24,0h.
Charge/discharge current shall not exceed 50mA.
Leave the capacitors in ambient condition for 6 to 24h (Class1) or 24±2h (Class2) before measurement.
Voltage conditioning (only for class 2)
Voltage treat the capacitors under testing temperature and voltage for 1 hour.
Leave the capacitors in ambient condition for 24±2h before measurement.
Use this measurement for initial value.</td></tr>
<tr><td></td><td></td><td>Capacitance</td><td><table><tr><th colspan="2">Characteristics</th><th>Change from the value before test</th></tr><tr><td>Class1</td><td>C0G</td><td>Capacitance drift within ± 7.5% or ± 0.75pF, whichever larger.</td></tr><tr><td>Class2</td><td>X7R
X7S
X7T</td><td>± 12.5 %</td></tr></table></td></tr>
<tr><td></td><td></td><td>Q
(Class1)</td><td><table><tr><th>Capacitance</th><th>Q</th></tr><tr><td>30pF and over</td><td>200 min.</td></tr><tr><td>Under 30pF</td><td>100+10/3×C min.</td></tr></table>C : Rated capacitance (pF)</td></tr>
<tr><td></td><td></td><td>D.F.
(Class2)</td><td>Characteristics
X7R/X7S/X7T
: 200% of initial spec. max.</td></tr>
<tr><td></td><td></td><td>Insulation Resistance</td><td>500MΩ or 25MΩ·μF min.
(As for the capacitors of rated voltage 16V DC and item below, 500MΩ or 5MΩ·μF min.,) whichever smaller.</td></tr>
<tr><td>21</td><td>Life</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="5">Reflow solder the capacitors on a P.C.Board shown in Appendix 1a or Appendix 1b before testing.
Test condition : maximum operating temperature ±2°C for 2,000 +48,0h
As for applied voltage, please refer to “(4) Voltage condition in the life test” at page 2.
Charge/discharge current shall not exceed 50mA.
Leave the capacitors in ambient condition for 6 to 24h (Class1) or 24±2h (Class2) before measurement.
Voltage conditioning
Voltage treat the capacitors under testing temperature and voltage for 1 hour.
Leave the capacitors in ambient condition for 24±2h before measurement.
Use this measurement for initial value.</td></tr>
<tr><td></td><td></td><td>Capacitance</td><td><table><tr><th colspan="2">Characteristics</th><th>Change from the value before test</th></tr><tr><td>Class1</td><td>C0G</td><td>Capacitance drift within ± 3% or ± 0.3pF, whichever larger.</td></tr><tr><td>Class2</td><td>X7R
X7S
X7T</td><td>± 15 %</td></tr></table></td></tr>
<tr><td></td><td></td><td>Q
(Class1)</td><td><table><tr><th>Capacitance</th><th>Q</th></tr><tr><td>30pF and over</td><td>350 and over</td></tr><tr><td>10pF and over to under 30pF</td><td>275+5/2×C min.</td></tr><tr><td>Under 10pF</td><td>200+10×C min.</td></tr></table>C : Rated capacitance (pF)</td></tr>
<tr><td></td><td></td><td>D.F.
(Class2)</td><td>Characteristics
X7R/X7S/X7T
: 200% of initial spec. max.</td></tr>
<tr><td></td><td></td><td>Insulation Resistance</td><td>1,000MΩ or 50MΩ·μF min.
(As for the capacitors of rated voltage 16V DC and the item below, 1,000 MΩ or 10MΩ·μF min.,) whichever smaller.</td></tr>
</table>

*As for the initial measurement of capacitors (Class2) on number 9, 13, 14, 15, 17, 18 and 19 leave capacitors at 150 –10,0°C for 1 hour and measure the value after leaving capacitors for 24±2h in ambient condition.

Appendix - 1a

P.C. Board for reliability test

Applied for CGJ2, CGJ3, CGJ4, CGJ5

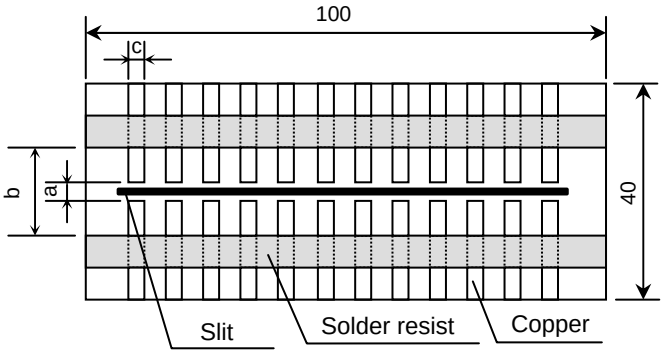


(Unit : mm)

Appendix - 1b

P.C. Board for reliability test

Applied for CGJ6

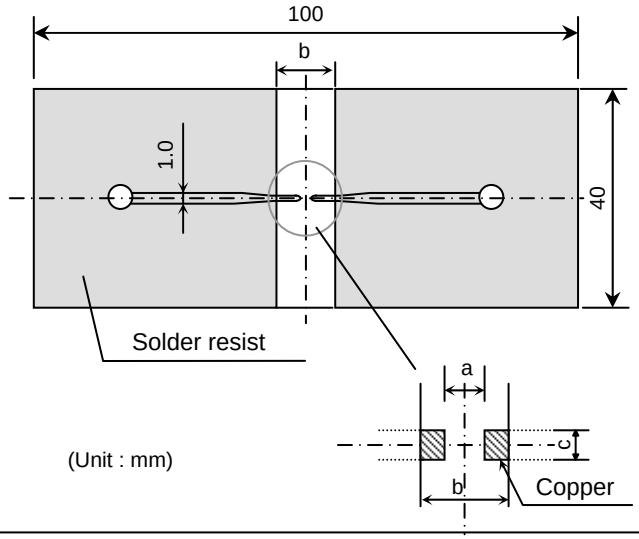


(Unit : mm)

Appendix - 2a

P.C. Board for bending test

Applied for CGJ2

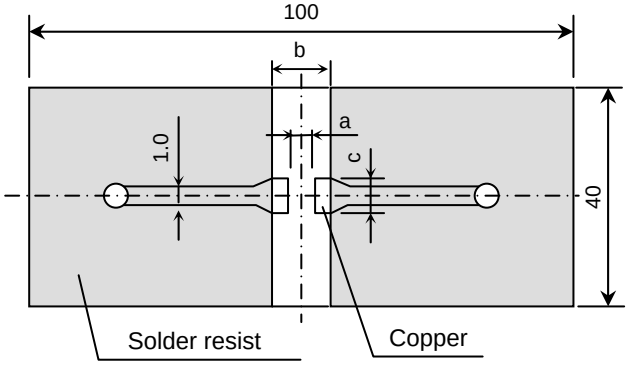


(Unit : mm)

Appendix - 2b

P.C. Board for bending test

Applied for CGJ3, CGJ4, CGJ5, CGJ6



(Unit : mm)

Material : Glass Epoxy (As per JIS C6484 GE4)

P.C. Board thickness : Appendix-2a 0.8mm

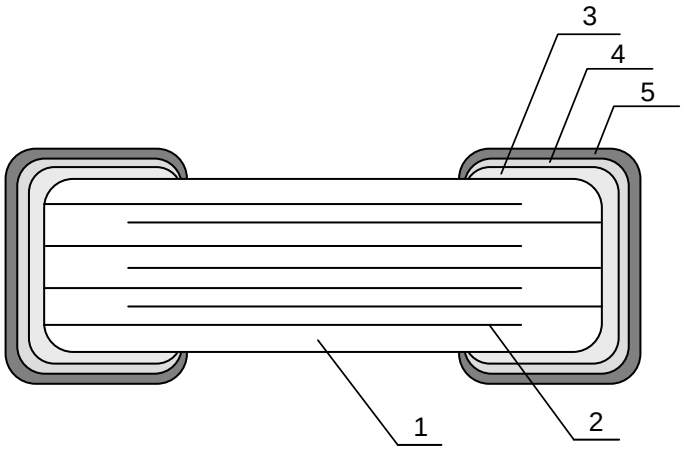
Appendix-1a, 1b, 2b 1.6mm

Copper (thickness 0.035mm)

Solder resist

TDK (EIA style)	Dimensions (mm)		
	a	b	c
CGJ2 (CC0402)	0.4	1.5	0.5
CGJ3 (CC0603)	1.0	3.0	1.2
CGJ4 (CC0805)	1.2	4.0	1.65
CGJ5 (CC1206)	2.2	5.0	2.0
CGJ6 (CC1210)	2.2	5.0	2.9

8. INSIDE STRUCTURE AND MATERIAL



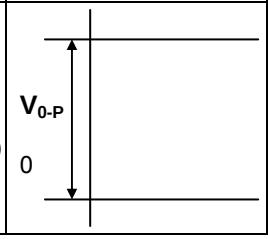
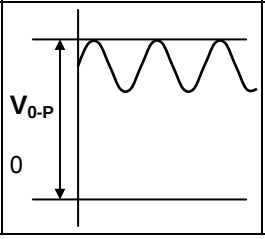
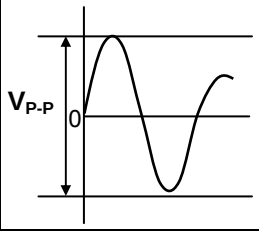
No.	NAME	MATERIAL	
		Class1	Class2
1	Dielectric	$CaZrO_3$	$BaTiO_3$
2	Electrode	Nickel (Ni)	
3	Termination	Copper (Cu)	
4		Nickel (Ni)	
5		Tin (Sn)	

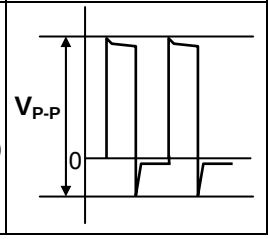
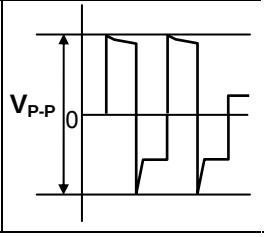
9. SOLDERING CONDITION

As for CGJ2(CC0402) types, reflow soldering only.

10. Caution

No.	Process	Condition
1	Operating Condition (Storage, Transportation)	1-1. Storage 1) The capacitors must be stored in an ambient temperature of 5 to 40°C with a relative humidity of 20 to 70%RH. The products should be used within 6 months upon receipt. 2) The capacitors must be operated and stored in an environment free of dew condensation and these gases such as Hydrogen Sulphide, Hydrogen Sulphate, Chlorine, Ammonia and sulfur. 3) Avoid storing in sun light and falling of dew. 4) Do not use capacitors under high humidity and high and low atmospheric pressure which may affect capacitors reliability. 5) Capacitors should be tested for the solderability when they are stored for long time. 1-2. Handling in transportation In case of the transportation of the capacitors, the performance of the capacitors may be deteriorated depending on the transportation condition. (Refer to JEITA RCR-2335B 9.2 Handling in transportation)
2	Circuit design ⚠ Caution	2-1. Operating temperature Operating temperature should be followed strictly within this specification, especially be careful with maximum temperature. 1) Do not use capacitors above the maximum allowable operating temperature. 2) Surface temperature including self heating should be below maximum operating temperature. (Due to dielectric loss, capacitors will heat itself when AC is applied. Especially at high frequencies around its SRF, the heat might be so extreme that it may damage itself or the product mounted on. Please design the circuit so that the maximum temperature of the capacitors including the self heating to be below the maximum allowable operating temperature. Temperature rise at capacitor surface shall be below 20°C) 3) The electrical characteristics of the capacitors will vary depending on the temperature. The capacitors should be selected and designed in taking the temperature into consideration. 2-2. Operating voltage 1) Operating voltage across the terminals should be below the rated voltage. When AC and DC are super imposed, V_{0-P} must be below the rated voltage. ——— (1) and (2) AC or pulse with overshooting, V_{P-P} must be below the rated voltage. ——— (3), (4) and (5) When the voltage is started to apply to the circuit or it is stopped applying, the irregular voltage may be generated for a transit period because of resonance or switching. Be sure to use the capacitors within rated voltage containing these Irregular voltage.

Voltage	(1) DC voltage	(2) DC+AC voltage	(3) AC voltage
Positional Measurement (Rated voltage)			

Voltage	(4) Pulse voltage (A)	(5) Pulse voltage (B)
Positional Measurement (Rated voltage)		

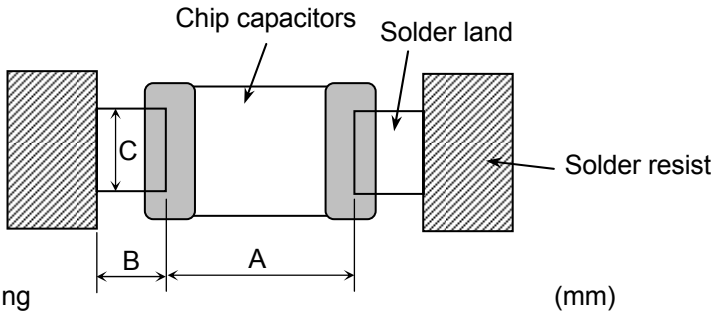
<table>
<tr><th>No.</th><th>Process</th><th>Condition</th></tr>
<tr><td>2</td><td>Circuit design
⚠ Caution</td><td>2) Even below the rated voltage, if repetitive high frequency AC or pulse is applied, the reliability of the capacitors may be reduced.

3) The effective capacitance will vary depending on applied DC and AC voltages. The capacitors should be selected and designed in taking the voltages into consideration.

2-3. Frequency
When the capacitors (Class 2) are used in AC and/or pulse voltages, the capacitors may vibrate themselves and generate audible sound.</td></tr>
<tr><td>3</td><td>Designing
P.C.board</td><td>The amount of solder at the terminations has a direct effect on the reliability of the capacitors.
1) The greater the amount of solder, the higher the stress on the chip capacitors, and the more likely that it will break. When designing a P.C.board, determine the shape and size of the solder lands to have proper amount of solder on the terminations.

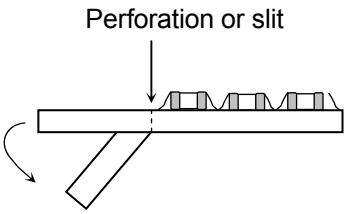
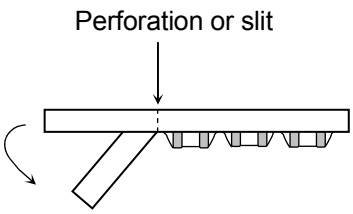
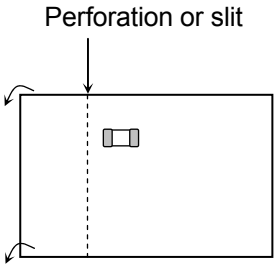
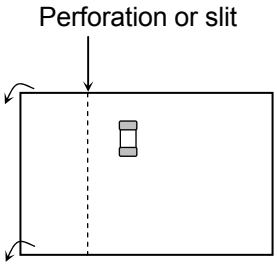
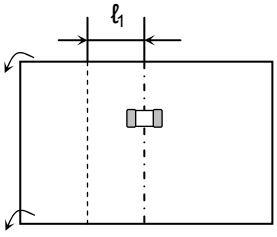
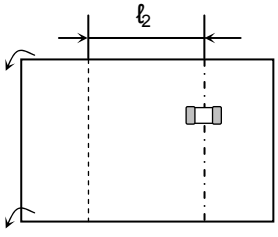
2) Avoid using common solder land for multiple terminations and provide individual solder land for each terminations.

3) Size and recommended land dimensions.

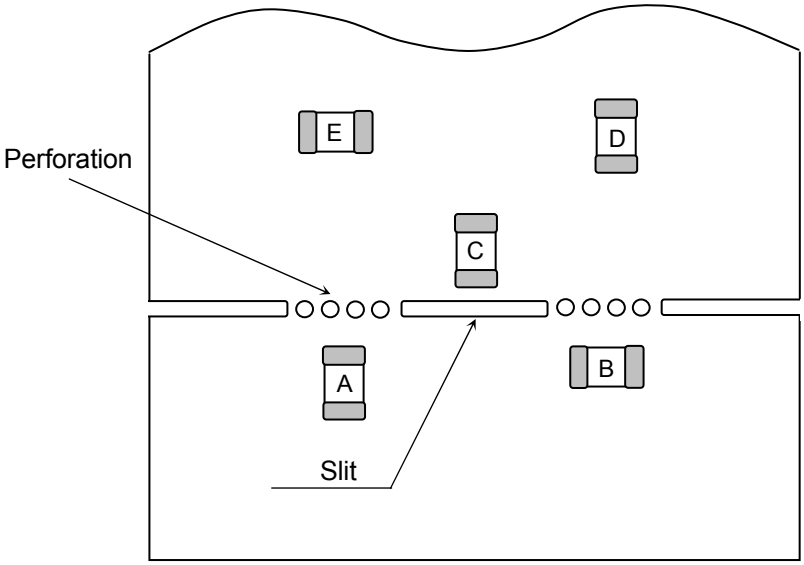
 

Flow soldering (mm)
<table>
<tr><th>Symbol \ Type</th><th>CGJ3 (CC0603)</th><th>CGJ4 (CC0805)</th><th>CGJ5 (CC1206)</th></tr>
<tr><td>A</td><td>0.7 - 1.0</td><td>1.0 - 1.3</td><td>2.1 - 2.5</td></tr>
<tr><td>B</td><td>0.8 - 1.0</td><td>1.0 - 1.2</td><td>1.1 - 1.3</td></tr>
<tr><td>C</td><td>0.6 - 0.8</td><td>0.8 - 1.1</td><td>1.0 - 1.3</td></tr>
</table>
Reflow soldering (mm)
<table>
<tr><th>Symbol \ Type</th><th>CGJ2 (CC0402)</th><th>CGJ3 (CC0603)</th><th>CGJ4 (CC0805)</th><th>CGJ5 (CC1206)</th></tr>
<tr><td>A</td><td>0.3 - 0.5</td><td>0.6 - 0.8</td><td>0.9 - 1.2</td><td>2.0 - 2.4</td></tr>
<tr><td>B</td><td>0.35 - 0.45</td><td>0.6 - 0.8</td><td>0.7 - 0.9</td><td>1.0 - 1.2</td></tr>
<tr><td>C</td><td>0.4 - 0.6</td><td>0.6 - 0.8</td><td>0.9 - 1.2</td><td>1.1 - 1.6</td></tr>
</table>
<table>
<tr><th>Symbol \ Type</th><th>CGJ6 (CC1210)</th></tr>
<tr><td>A</td><td>2.0 - 2.4</td></tr>
<tr><td>B</td><td>1.0 - 1.2</td></tr>
<tr><td>C</td><td>1.9 - 2.5</td></tr>
</table></td></tr>
</table>

No.	Process	Condition
3	Designing P.C.board	4) Recommended chip capacitors layout is as following. (CGJ2,CGJ3,CGJ4,CGJ5)

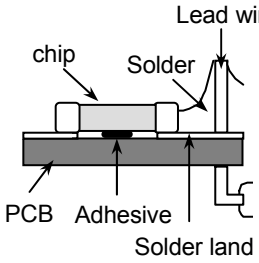
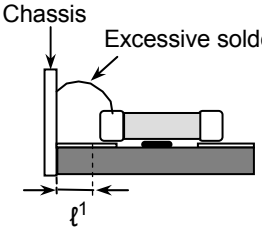
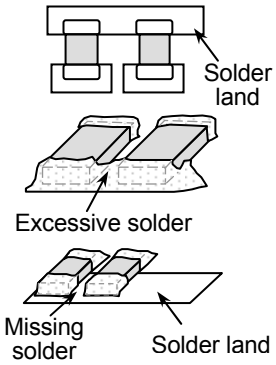
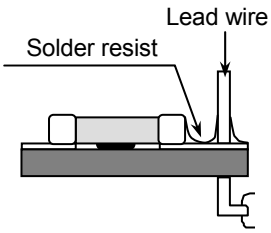
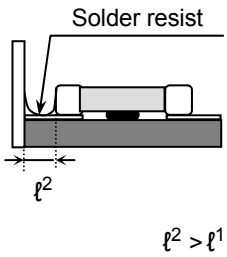
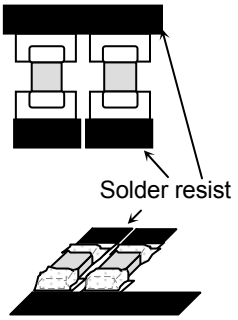
	Disadvantage against bending stress	Advantage against bending stress
Mounting face	 Break P.C.board with mounted side up.	 Break P.C.board with mounted side down.
Chip arrangement (Direction)	Mount perpendicularly to perforation or slit 	Mount in parallel with perforation or slit 
Distance from slit	Closer to slit is higher stress  $(\ell_1 < \ell_2)$	Away from slit is less stress  $(\ell_1 < \ell_2)$

No.	Process	Condition
3	Designing P.C.board	5) Mechanical stress varies according to location of chip capacitors on the P.C.board.

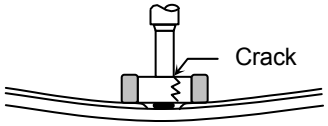
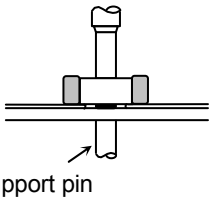
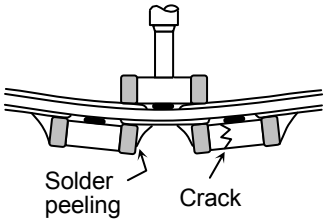
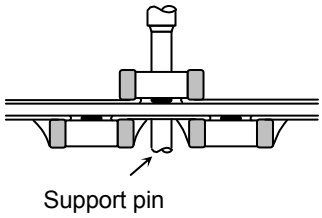


The stress in capacitors is in the following order.
A > B = C > D > E

6) Layout recommendation

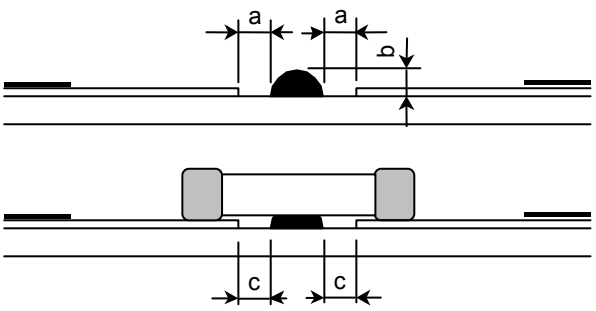
Example	Use of common solder land	Soldering with chassis	Use of common solder land with other SMD
Need to avoid			
Recommen-dation			

No.	Process	Condition
4	Mounting	4-1. Stress from mounting head If the mounting head is adjusted too low, it may induce excessive stress in the chip capacitors to result in cracking. Please take following precautions. 1) Adjust the bottom dead center of the mounting head to reach on the P.C.board surface and not press it. 2) Adjust the mounting head pressure to be 1 to 3N of static weight. 3) To minimize the impact energy from mounting head, it is important to provide support from the bottom side of the P.C.board. See following examples.

	Not recommended	Recommended
Single sided mounting		
Double-sides mounting		

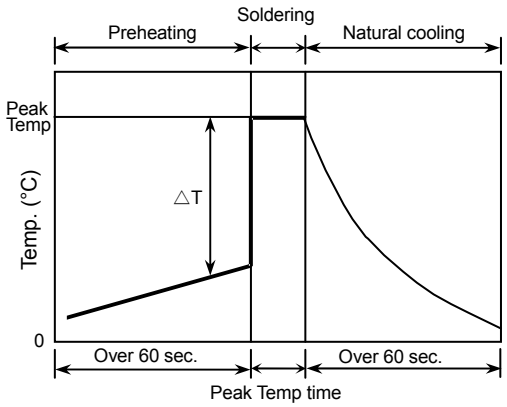
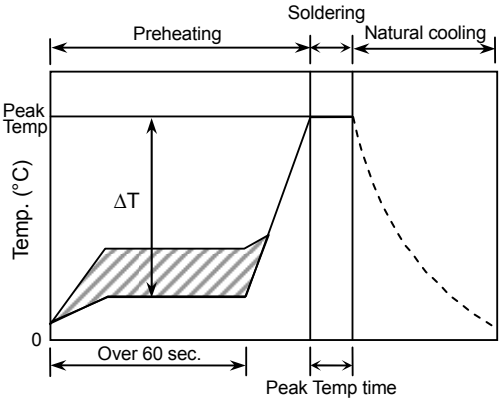
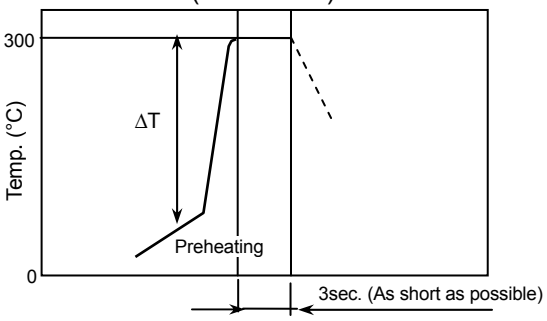
When the centering jaw is worn out, it may give mechanical impact on the capacitors to cause crack. Please control the close up dimension of the centering jaw and provide sufficient preventive maintenance and replacement of it.

4-2. Amount of adhesive



Example : CGJ4 (CC0805), CGJ5 (CC1206)

a	0.2mm min.
b	70 - 100μm
c	Do not touch the solder land

No.	Process	Condition
5	Soldering	5-1. Flux selection Although highly-activated flux gives better solderability, substances which increase activity may also degrade the insulation of the chip capacitors. To avoid such degradation, it is recommended following. 1) It is recommended to use a mildly activated rosin flux (less than 0.1wt% chlorine). Strong flux is not recommended. 2) Excessive flux must be avoided. Please provide proper amount of flux. 3) When water-soluble flux is used, enough washing is necessary. 5-2. Recommended soldering profile by various methods Wave soldering  Reflow soldering  Manual soldering (Solder iron)  APPLICATION As for CGJ3 (CC0603), CGJ4 (CC0805) and CGJ5 (CC1206), applied to wave soldering and reflow soldering. As for CGJ2 (CC0402) and CGJ6 (CC1210), applied only to reflow soldering. 5-3. Recommended soldering peak temp and peak temp duration

Temp./Duration / Solder	Wave soldering		Reflow soldering	
	Peak temp(°C)	Duration(sec.)	Peak temp(°C)	Duration(sec.)
Pb-Sn Solder	250 max.	3 max.	230 max.	20 max.
Lead Free Solder	260 max.	5 max.	260 max.	10 max.

Recommended solder compositions
Sn-37Pb (Pb-Sn solder)
Sn-3.0Ag-0.5Cu (Lead Free Solder)

No.	Process	Condition
5	Soldering	5-4. Avoiding thermal shock 1) Preheating condition

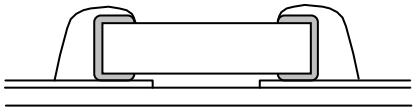
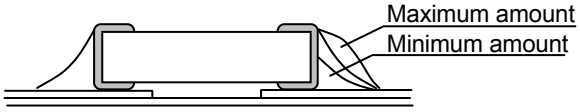
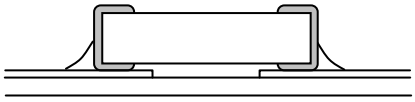
Soldering	Type	Temp. (°C)
Wave soldering	CGJ3(CC0603), CGJ4(CC0805)	ΔT ≤ 150
Reflow soldering	CGJ2(CC0402), CGJ3(CC0603), CGJ4(CC0805), CGJ5(CC1206)	ΔT ≤ 150
	CGJ6(CC1210)	ΔT ≤ 130
Manual soldering	CGJ2(CC0402), CGJ3(CC0603), CGJ4(CC0805), CGJ5(CC1206)	ΔT ≤ 150
	CGJ6(CC1210)	ΔT ≤ 130

2) Cooling condition

Natural cooling using air is recommended. If the chips are dipped into a solvent for cleaning, the temperature difference (ΔT) must be less than 100°C.

5-5. Amount of solder

Excessive solder will induce higher tensile force in chip capacitors when temperature changes and it may result in chip cracking. In sufficient solder may detach the capacitors from the P.C.board.

Excessive solder		Higher tensile force in chip capacitors to cause crack
Adequate		
Insufficient solder		Low robustness may cause contact failure or chip capacitors come off the P.C.board.

5-6. Solder repair by solder iron

1) Selection of the soldering iron tip

Tip temperature of solder iron varies by its type, P.C.board material and solder land size. The higher the tip temperature, the quicker the operation. However, heat shock may cause a crack in the chip capacitors.

Please make sure the tip temp. before soldering and keep the peak temp and time in accordance with following recommended condition. (Please preheat the chip capacitors with the condition in 5-4 to avoid the thermal shock.)

<table>
<tr><th>No.</th><th>Process</th><th>Condition</th></tr>
<tr><td>5</td><td>Soldering</td><td>
Recommended solder iron condition (Pb-Sn Solder and Lead Free Solder)
<table>
<tr><th>Temp. (°C)</th><th>Duration (sec.)</th><th>Wattage (W)</th><th>Shape (mm)</th></tr>
<tr><td>300 max.</td><td>3 max.</td><td>20 max.</td><td>Ø 3.0 max.</td></tr>
</table>
2) Direct contact of the soldering iron with ceramic dielectric of chip capacitors may cause crack. Do not touch the ceramic dielectric and the terminations by solder iron.

5-7. Sn-Zn solder
Sn-Zn solder affects product reliability.
Please contact TDK in advance when utilize Sn-Zn solder.

5-8. Countermeasure for tombstone
The misalignment between the mounted positions of the capacitors and the land patterns should be minimized. The tombstone phenomenon may occur especially the capacitors are mounted (in longitudinal direction) in the same direction of the reflow soldering.
(Refer to JEITA RCR-2335B Annex A (Informative) Recommendations to prevent the tombstone phenomenon)
</td></tr>
<tr><td>6</td><td>Cleaning</td><td>
1) If an unsuitable cleaning fluid is used, flux residue or some foreign articles may stick to chip capacitors surface to deteriorate especially the insulation resistance.

2) If cleaning condition is not suitable, it may damage the chip capacitors.

2)-1. Insufficient washing
(1) Terminal electrodes may corrode by Halogen in the flux.

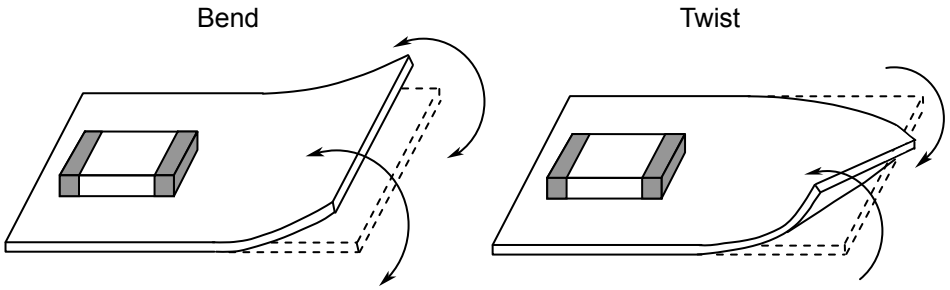
(2) Halogen in the flux may adhere on the surface of capacitors, and lower the insulation resistance.

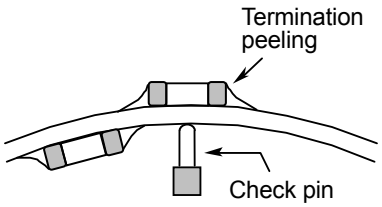
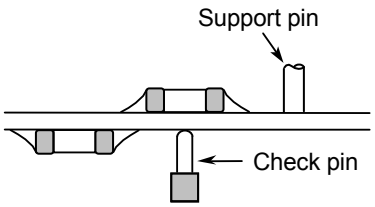
(3) Water soluble flux has higher tendency to have above mentioned problems (1) and (2).

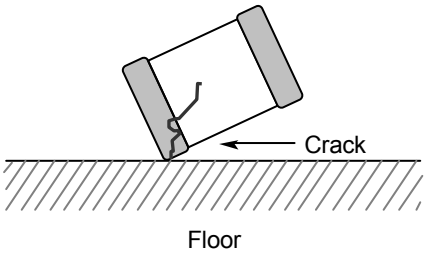
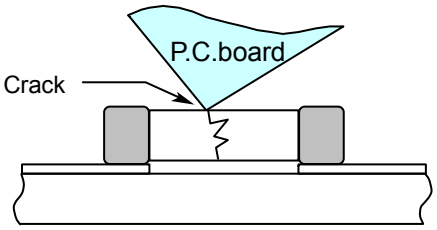
2)-2. Excessive washing
When ultrasonic cleaning is used, excessively high ultrasonic energy output can affect the connection between the ceramic chip capacitor's body and the terminal electrode. To avoid this, following is the recommended condition.

Power : 20 W/ℓ max.
Frequency : 40 kHz max.
Washing time : 5 minutes max.

2)-3. If the cleaning fluid is contaminated, density of Halogen increases, and it may bring the same result as insufficient cleaning.
</td></tr>
</table>

No.	Process	Condition
7	Coating and molding of the P.C.board	1) When the P.C.board is coated, please verify the quality influence on the product. 2) Please verify carefully that there is no harmful decomposing or reaction gas emission during curing which may damage the chip capacitors. 3) Please verify the curing temperature.
8	Handling after chip mounted ⚠ Caution	1) Please pay attention not to bend or distort the P.C.board after soldering in handling otherwise the chip capacitors may crack. 
		2) When functional check of the P.C.board is performed, check pin pressure tends to be adjusted higher for fear of loose contact. But if the pressure is excessive and bend the P.C.board, it may crack the chip capacitors or peel the terminations off. Please adjust the check pins not to bend the P.C.board.

Item	Not recommended	Recommended
Board bending		

No.	Process	Condition
9	Handling of loose chip capacitors	1) If dropped the chip capacitors may crack. Once dropped do not use it. Especially, the large case sized chip capacitors are tendency to have cracks easily, so please handle with care.  2) Piling the P.C.board after mounting for storage or handling, the corner of the P.C. board may hit the chip capacitors of another board to cause crack. 
10	Capacitance aging	The capacitors (Class 2) have aging in the capacitance. They may not be used in precision time constant circuit. In case of the time constant circuit, the evaluation should be done well.
11	Estimated life and estimated failure rate of capacitors	The estimated life and failure rate depend on the applied temperature and the voltage. This can be calculated by the equation described in JEITA RCR-2335B Annex 6(Informative) “Calculation of the estimated life time and the estimated failure rate.” (Voltage acceleration coefficient : 3 multiplication rule, Temperature acceleration coefficient : 10°C rule) The failure rate can be decreased by reducing the temperature and the voltage but they will not be guaranteed.

11. PACKAGING LABEL

11.1 Packaging shall be done to protect the components from the damage during transportation and storing, and a label which has the following information shall be attached.
(See Figure. 11.1)

1) Inspection No.
2) TDK P/N
3) Customer's P/N
4) Quantity

*Composition of Inspection No.

Example F 2 A – OO – OOO
(a) (b) (c) (d) (e)

a) Line code
b) Last digit of the year
c) Month and A for January and B for February and so on. (Skip I)
d) Inspection Date of the month.
e) Serial No. of the day

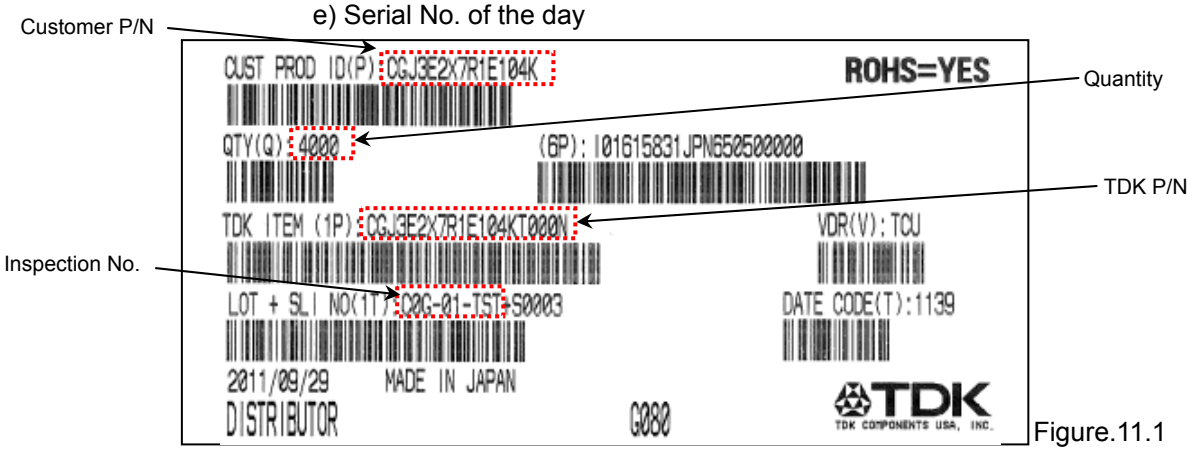


Figure.11.1

11.2 Anti-counterfeit Label

The anti-counterfeit label with a unique identification code is placed over the reel flanges to ensure material authenticity.

Product authentication can be confirmed by visiting TDK.com and entering the requested information. The secure on-line system will provide an immediate response to the authenticity of the TDK product from the information provided.

Figure.11.2

DO NOT USE if: the seal is broken or evidence of tampering is present.
Contact your local TDK representative for further instructions.

11.3 Radio Frequency Identification (RFID) label.

TDK's optional RFID reel tags are commissioned with lot specific information such as: lot number, customer part number, and quantity. RFID reel tag data can be customized to meet individual customer RFID requirements, as up to 64 bits of data can be stored on the RFID tag. Please contact your TDK sales representative for more information regarding customized information for RFID reel tags.

Below is an example of TDK standard RFID reel tag data (red font indicates data identifiers).

PCGJ2B1C104K, 1PCGJ2B2X7R1C104KT000N, Q10000
(customer part no.) (TDK item description) (reel quantity)

TDK's RFID tag is compliant to ISO/IEC 18000-6 :2010 requirements and can be read within the standard operating frequency range for the United States (902-928Mhz) and international regulated frequencies within the Ultra High Frequency (UHF) bandwidth for Europe (865-868Mhz) and Japan (952-957Mhz).

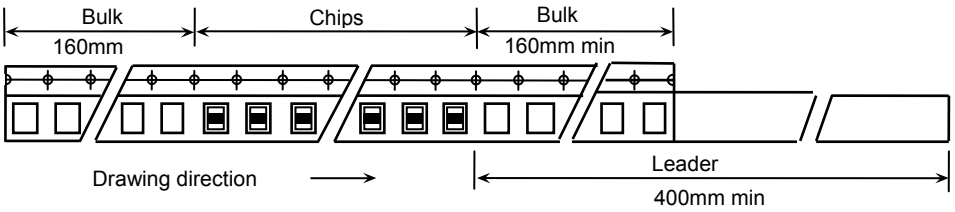
12. TAPE PACKAGING SPECIFICATION

1. CONSTRUCTION AND DIMENSION OF TAPING

1-1. Dimensions of carrier tape

Dimensions of paper tape shall be according to Appendix 3, 4.
Dimensions of plastic tape shall be according to Appendix 5.

1-2. Bulk part and leader of taping

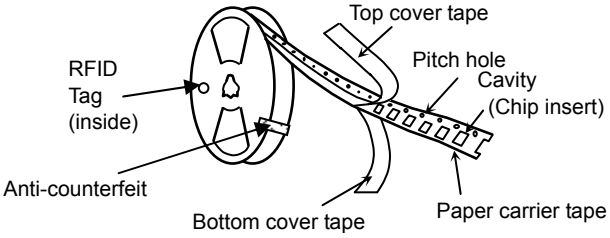


1-3. Dimensions of reel

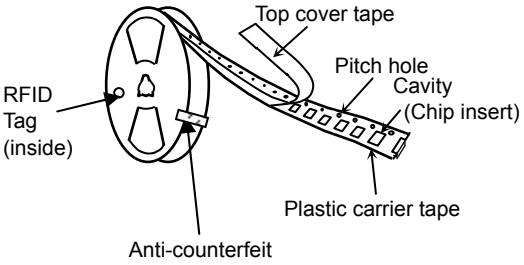
Dimensions of Ø178 reel shall be according to Appendix 6, 7.
Dimensions of Ø330 reel shall be according to Appendix 8, 9.

1-4. Structure of taping

Type 1



Type 2



2. CHIP QUANTITY

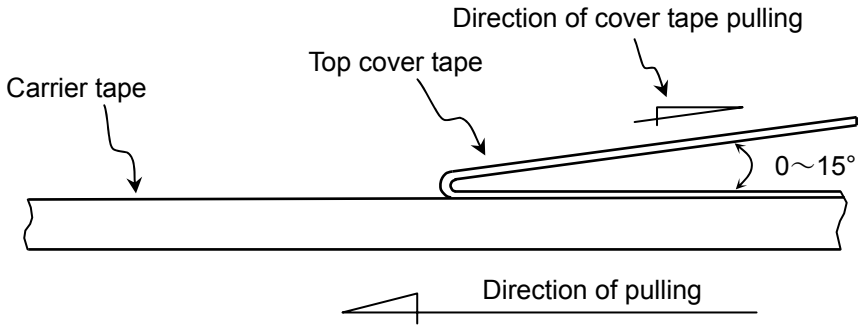
Type	Thickness of chip	Taping Material	Chip quantity(pcs.)	
			Ø 178mm reel	Ø 330mm reel
CGJ2	0.50 mm	Paper	10,000	50,000
CGJ3	0.80 mm	Paper	4,000	10,000
CGJ4	0.60mm	Paper	4,000	
	0.85 mm	Paper		10,000
	1.25 mm	Plastic	2,000	
CGJ5	0.60 mm	Paper	4,000	10,000
	0.85 mm			
	1.15 mm	Plastic	2,000	
	1.30 mm			
	1.60 mm			8,000
CGJ6	1.60 mm	Plastic	2,000	8,000
	2.00 mm		1,000	5,000

3. PERFORMANCE SPECIFICATIONS

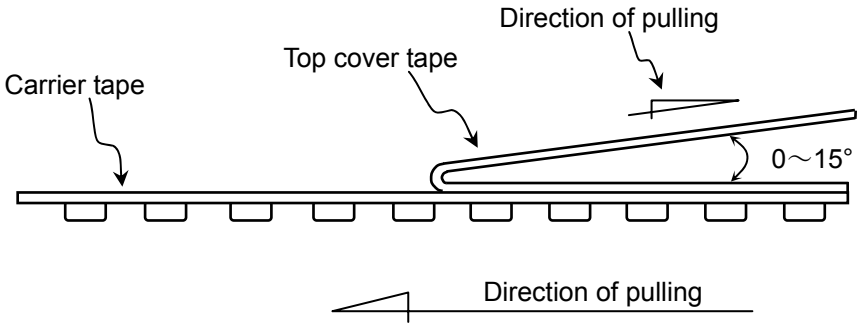
3-1. Fixing peeling strength (top tape)

0.05-0.7N. (See the following figure.)

TYPE 1 (Paper)



TYPE 2 (Plastic)



3-2. Carrier tape shall be flexible enough to be wound around a minimum radius of 30mm with components in tape.

3-3. The missing of components shall be less than 0.1%

3-4. Components shall not stick to fixing tape.

3-5. The fixing tapes shall not protrude beyond the edges of the carrier tape not shall cover the sprocket holes.

13. Sigma Report

Sigma Report will be performed for each lot. The results will be available on-line by visiting TDK.com and entering the requested information.
The Sigma Report will include performance (electrical and mechanical) and reliability metrics (FIT and MTTF).
A list of test completed is provided below.

Ref.	Test
1	Appearance
2	Destructive Physical Analysis
3	Insulation Resistance
4	Voltage Proof
5	Capacitance
6/7	Q/DF
8/9	Tem. Characteristics
11	Bending
12	Solderability
21	Life
	HALT
	Physical Dimensions

14. Warranty

TDK's CGJ Series MLCCs are designed and warranted to meet the performance standards shown in Table1 of Section 7(Performance Table) of this specification using the test and inspection methods specified herein.

While TDK's CGJ Series MLCCs are intended for high reliability applications within the range of conditions set forth in this specification, TDK is not aware of all applications in which these parts may be used, or the requirements of your particular application.
This series is not designed or warranted to meet any specifications of any intermediate or end user different from or in addition to those contained in this specification, nor are they intended or warranted for use in the applications excluded below.

Excluded Applications:

- Aerospace/aviation equipment (where the application is related to flight);
- FDA Class III medical equipment (and including any in-the-body medical application or any other medical application where of the TDK part could possibly endanger human life or health);
- Nuclear energy-related equipment; and/or
- Military equipment (where designed to (i) destructive or explosive functionality including ammunition, firearms, warheads, mines and/or bombs, or (ii) discharging, emitting or blast-off functionality including artillery or missiles, or (iii) military aircraft or spacecraft).

Additionally, if you intend to use TDK's CGJ Series MLCCs in any of the applications listed below ("Specialized Applications"), you should carefully review the requirements of the particular application as against this specification so as to ensure the suitability of these parts for that application. TDK cannot ensure the suitability of these parts for the Specialized Applications below.

Specialized Applications:

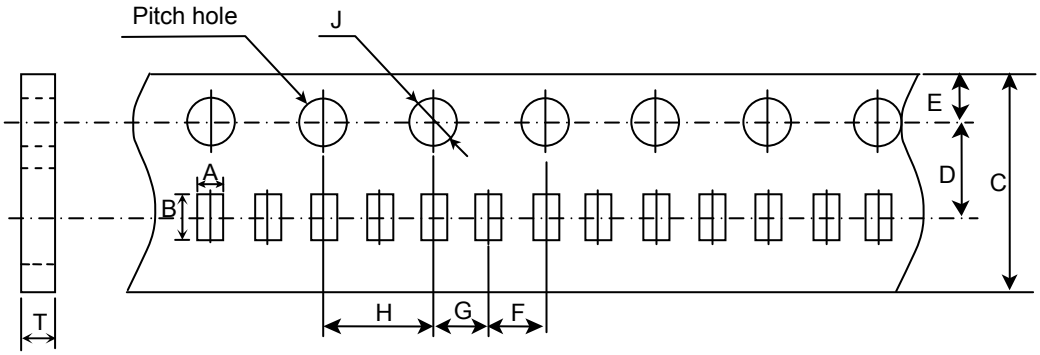
- FDA Class I & II medical equipment (with the sale of parts for FDA Class II applications subject to prior TDK consultation).
- Transportation equipment (electric trains, ships, etc.) [other than automotive applications];
- Transportation control equipment;
- Power-generation control equipment;
- Seabed equipment;
- Public information processing equipment;
- Electric heating apparatus and/or burning equipment;
- Disaster/crime prevention equipment; and/or
- Safety equipment.

TDK MAKES NO OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING THE WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR PURPOSE.
IN NO EVENT SHALL TDK BE RESPONSIBLE FOR ANY DAMAGE OR LIABILITY CAUSED BY USE OF THESE PARTS
IN ANY OF THE EXCLUDED APPLICATIONS LISTED ABOVE OR FOR ANY OTHER USE EXCEEDING THE RANGE OR CONDITIONS SET FORTH IN THIS SPECIFICATION.

Please note that when designing your product, device, or equipment-even for general purpose applications - you should secure a protection circuit/device or provide backup circuits in your product, device, or equipment.

Appendix 3

Paper Tape



(Unit : mm)

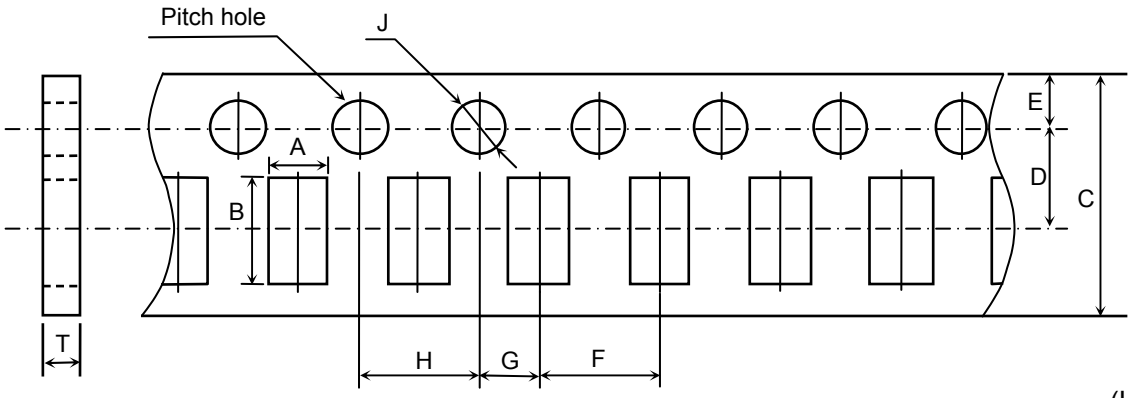
Symbol / Type	A	B	C	D	E	F
CGJ2 (CC0402)	(0.65)	(1.15)	8.00 ± 0.30	3.50 ± 0.05	1.75 ± 0.10	2.00 ± 0.05

Symbol / Type	G	H	J	T
CGJ2 (CC0402)	2.00 ± 0.05	4.00 ± 0.10	Ø 1.5 $^{+0.10}_{0}$	0.60 ± 0.15

* The values in the parentheses ( ) are for reference

Appendix 4

Paper Tape



(Unit : mm)

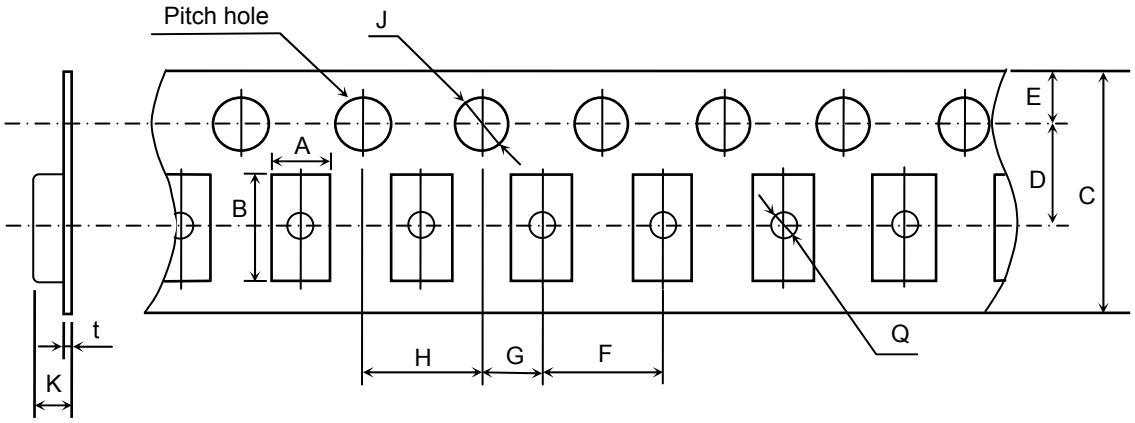
Symbol / Type	A	B	C	D	E	F
CGJ3 (CC0603)	(1.10)	(1.90)	8.00 ± 0.30	3.50 ± 0.05	1.75 ± 0.10	4.00 ± 0.10
CGJ4 (CC0805)	(1.50)	(2.30)				
CGJ5 (CC1206)	(1.90)	(3.50)				

Symbol / Type	G	H	J	T
CGJ3 (CC0603)	2.00 ± 0.05	4.00 ± 0.10	Ø 1.5 $^{+0.10}_{0}$	1.20 max.
CGJ4 (CC0805)				
CGJ5 (CC1206)				

* The values in the parentheses ( ) are for reference.

Appendix 5

Plastic Tape



(Unit : mm)

Symbol / Type	A	B	C	D	E	F
CGJ4 (CC0805)	(1.50)	(2.30)	8.00 ± 0.30 [12.0 ± 0.30]	3.50 ± 0.05 [5.50 ± 0.05]	1.75 ± 0.10	4.00 ± 0.10
CGJ5 (CC1206)	(1.90)	(3.50)				
CGJ6 (CC1210)	(2.90)	(3.60)				

Symbol / Type	G	H	J	K	t	Q
CGJ4 (CC0805)	2.00 ± 0.05	4.00 ± 0.10	Ø 1.5 +0.10 0	2.50 max.	0.30 max.	Ø 0.50 min.
CGJ5 (CC1206)						
CGJ6 (CC1210)				3.20 max.	0.60 max.	

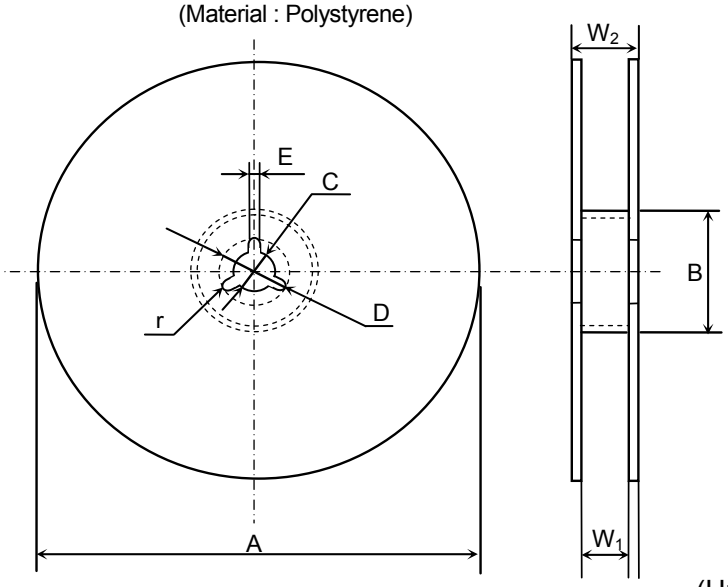
* The values in the parentheses ( ) are for reference.

* As for 2.5mm thickness products, apply values in the brackets [ ].

Appendix 7

CGJ2, CGJ3, CGJ4, CGJ5, CGJ6 (As for CGJ6 type, any thickness of the item except 2.5mm)

(Material : Polystyrene)



(Unit : mm)

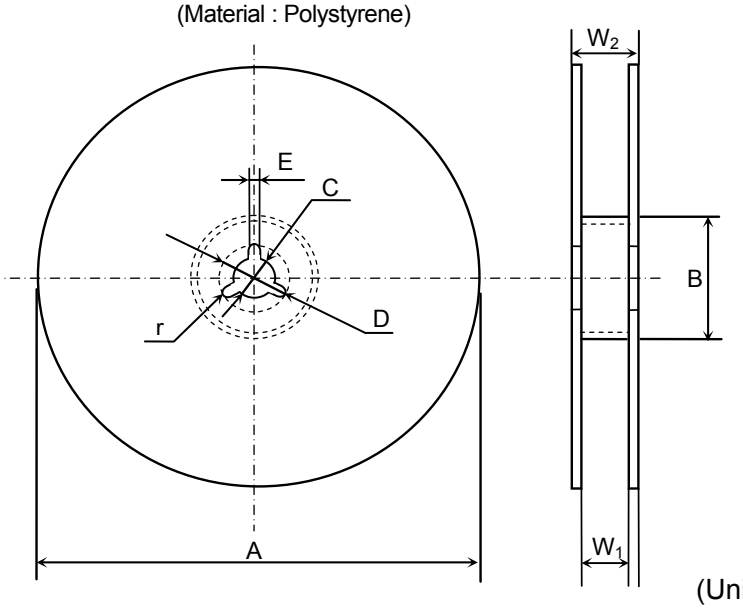
Symbol	A	B	C	D	E	W_1
Dimension	Ø178 ± 2.0	Ø60 ± 2.0	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	9.0 ± 0.3

Symbol	W_2	r
Dimension	13.0 ± 1.4	1.0

Appendix 8

CGJ6 (Applied to 2.5mm thickness products)

(Material : Polystyrene)



(Unit : mm)

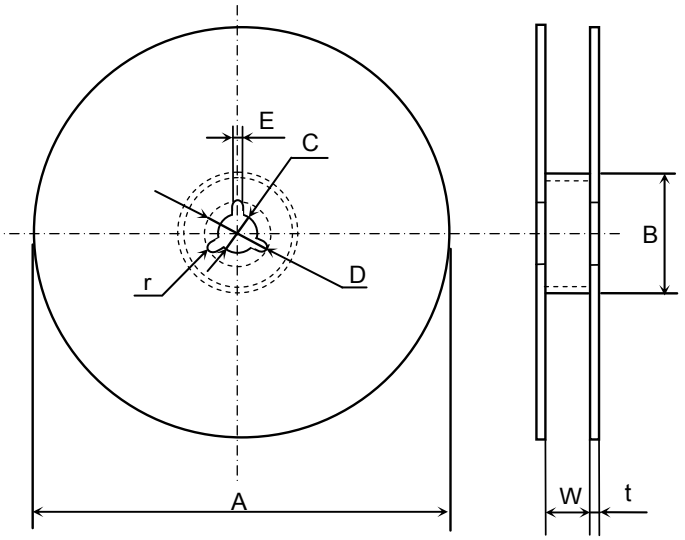
Symbol	A	B	C	D	E	W_1
Dimension	Ø178 ± 2.0	Ø60 ± 2.0	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	13.0 ± 0.3

Symbol	W_2	r
Dimension	17.0 ± 1.4	1.0

Appendix 9

CGJ2, CGJ3, CGJ4, CGJ5, CGJ6 (As for CGJ6 type, any thickness of the item except 2.5mm)

(Material : Polystyrene)



(Unit : mm)

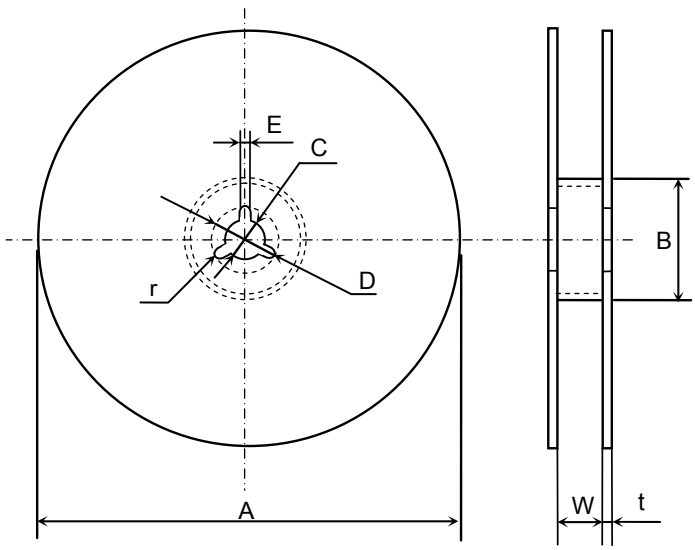
Symbol	A	B	C	D	E	W
Dimension	Ø382 max. (Nominal Ø330)	Ø50 min.	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	10.0 ± 1.5

Symbol	t	r
Dimension	2.0 ± 0.5	1.0

Appendix 10

CGJ6 (Applied to 2.5mm thickness products)

(Material : Polystyrene)



(Unit : mm)

Symbol	A	B	C	D	E	W
Dimension	Ø382 max. (Nominal Ø330)	Ø50 min.	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	14.0 ± 1.5

Symbol	t	r
Dimension	2.0 ± 0.5	1.0