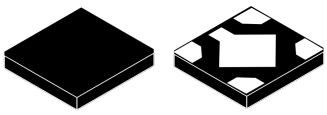
LD56050

Datasheet

500 mA ultra-low dropout linear regulator with bias supply



DFN4 1.2 x 1.2

Maturity status link
LD56050

Features

- Input voltage from 0.8 to 5.5 V
- Bias supply pin
- Ultra low-dropout voltage (80 mV typ. at 500 mA load)
- Low ground current (27 µA typ. at no-load)
- Output voltage tolerance: ± 1.5% overtemperature, 0.5% at 25 °C
- 500 mA guaranteed output current
- 50 mV output voltage step available from 0.8 V to 3.6 V
- Logic-controlled electronic shutdown
- Internal current limit with foldback
- Thermal shutdown
- Output active discharge function
- Available in DFN4 1.2 x 1.2 mm package
- Temperature range: -40 °C to 85 °C

Applications

- Mobile phones
- Tablets
- Battery-powered systems
- Camera supply

Description

The LD56050 is a high accuracy voltage regulator, which provides 0.5 A of current. It is equipped with an NMOS pass transistor, whose gate is biased by a dedicated pin, thus allowing an ultra low-drop performance even at very low input voltages.

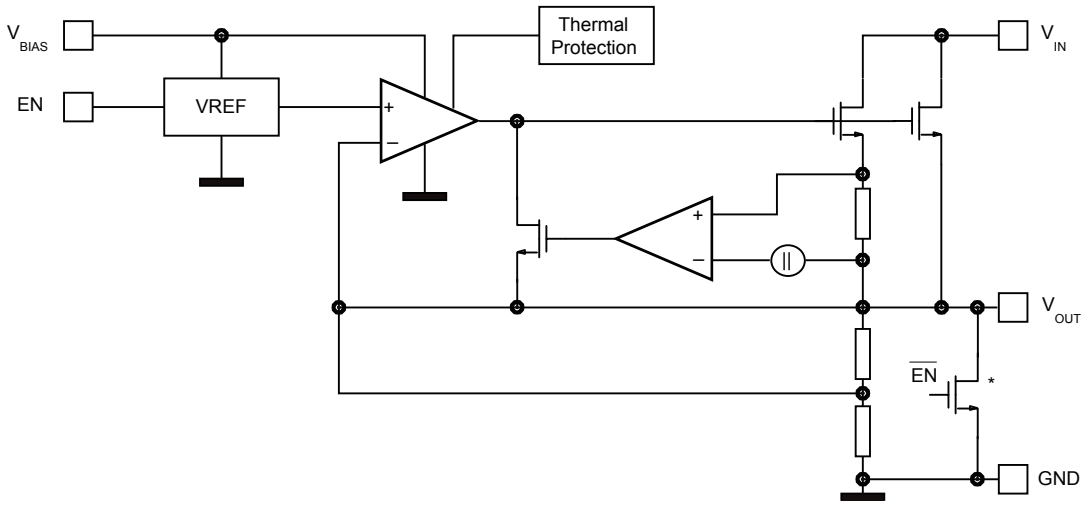
It is available in DFN4 1.2 x 1.2 package, allowing the maximum space saving.

The device is stabilized with a small ceramic capacitor on the output. The ultra low-drop, low quiescent current and short circuit current foldback make the LD56050 suitable for low power battery-operated applications.

An enable logic control function puts the LD56050 in shutdown mode allowing a total current consumption lower than 0.1 µA. Thermal protection is also included.

1 Diagram

Figure 2. **Block diagram**



Note: (*) Output discharge MOSFET.

2 Pin configuration

Figure 3. **Pin connection (top view)**

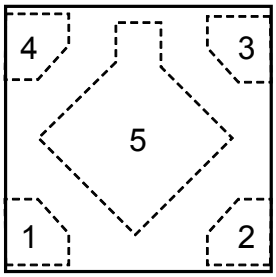


Table 1. **Pin description**

Pin n° DFN8	Symbol	Function
1	V_{OUT}	Output voltage
2	V_{BIAS}	Bias supply input
3	EN	Enable pin logic input: low = shutdown, high = active. Not internally pulled-up. Don't leave floating.
4	V_{IN}	Input voltage (power element)
5	GND	Common ground

3 Typical application

Figure 4. **Typical application circuit**

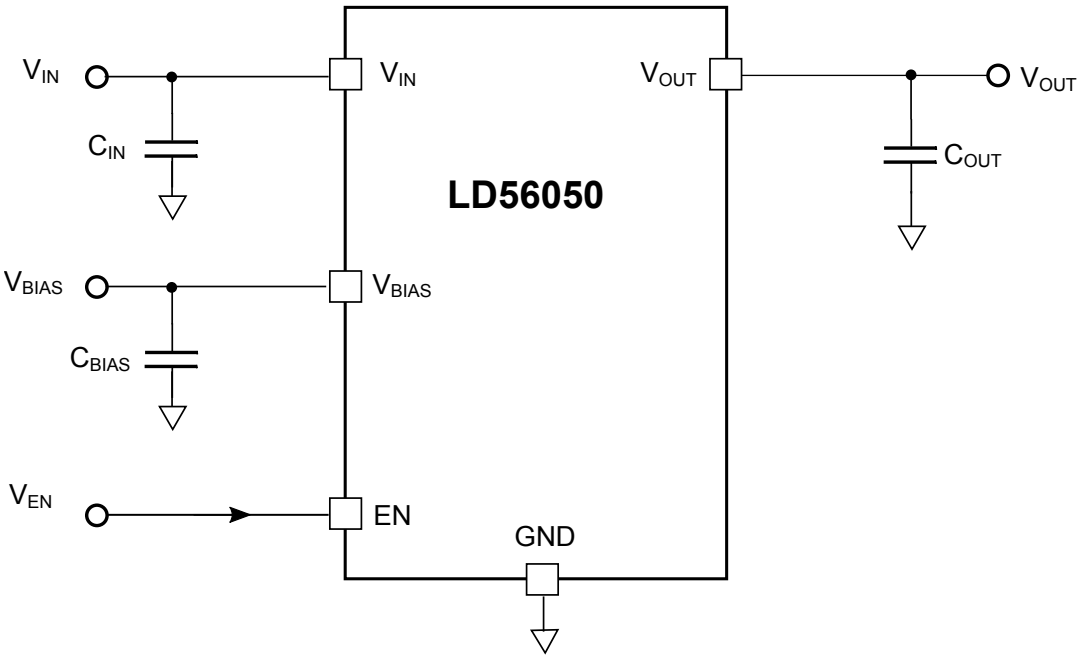


Table 2. **Typical bill of material**

Symbol	Value	Description	Note
C_{IN}	1 µF	Output voltage	Ceramic type
C_{BIAS}	100 nF	Bias supply input	
C_{OUT}	2.2 µF	Input voltage (power element)	

4 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input voltage	- 0.3 to 7	V
V_{OUT}	Output voltage	- 0.3 to V_{IN} + 0.3	V
V_{EN}	Enable input voltage	- 0.3 to 7	V
I_{OUT}	Output current	Internally limited	mA
P_D	Power dissipation	Internally limited	mW
T_{STG}	Storage temperature range	- 40 to 150	°C
T_{OP}	Operating junction temperature range	- 40 to 85	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	170	°C/W

Table 5. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	2	kV
		CDM	500	V

5 Electrical characteristics

V_{BIAS} = 2.7 V or V_{OUT} + 1.6 V (whichever is greater); V_{IN} = $V_{OUT(NOM)}$ + 0.3 V; I_{OUT} = 1 mA; C_{IN} = 1 µF, C_{OUT} = 2.2 µF; V_{EN} = 1 V; typical values are at T_J = 25 °C; min./max. values are at -40 °C ≤ T_J ≤ 85 °C, unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		V_{OUT} + V_{DROP}		5.5	V
V_{BIAS}	Operating bias voltage	V_{OUT} ≤ 1 V	2.4		5.5	V
		V_{OUT} > 1 V	V_{OUT} + 1.4		5.5	V
V_{UVLO}	BIAS undervoltage lockout	V_{BIAS} rising		1.6		V
		Hysteresis		0.2		
V_{OUT}	Output voltage accuracy			±0.5		%
		$V_{OUT(NOM)}$ + 0.3 V ≤ V_{IN} ≤ $V_{OUT(NOM)}$ + 1.0 V; 2.7 V or $V_{OUT(NOM)}$ + 1.6 V (whichever is greater) ≤ V_{BIAS} ≤ 5.5 V; I_{OUT} = 1 mA to 0.5 A; -40°C ≤ T_J ≤ 85°C	-1.5		+1.5	%
ΔV_{OUT-IN}	V_{IN} static regulation(1)	$V_{OUT(NOM)}$ + 0.3 V ≤ V_{IN} ≤ 5.0 V, I_{OUT} = 1 mA		0.02	0.1	%/V
$\Delta V_{OUT-BIAS}$	V_{BIAS} line regulation(1)	2.7 V or $V_{OUT(NOM)}$ + 1.6 V (whichever is greater) ≤ V_{BIAS} ≤ 5.5 V; I_{OUT} = 1 mA		0.01	0.1	%/V
ΔV_{OUT}	Static load regulation	I_{OUT} = 1 mA to 500 mA		1.5		mV
V_{DROP}	Dropout voltage	I_{OUT} = 0.15 A; V_{OUT} = 97% of $V_{OUT(NOM)}$		27	75	mV
		I_{OUT} = 0.5 A; V_{OUT} = 97% of $V_{OUT(NOM)}$		80	250	
$V_{DROP-BIAS}$	Dropout voltage	V_{BIAS} = V_{IN}; I_{OUT} = 0.5 A		0.9	1.5	V
e_N	Output noise voltage	$V_{OUT(NOM)}$ = 1.05 V; V_{IN} = 1.5 V 10 Hz to 100 kHz, I_{OUT} = 1 mA		38		μV_{RMS}
SVR_{IN}	V_{IN} supply voltage rejection	V_{IN} = $V_{OUT(NOM)}$+ 0.5 V +/- V_{RIPPLE} V_{RIPPLE} = 0.2 V, freq=1 kHz, I_{OUT} = 150 mA; V_{BIAS} = 2.7 V or V_{OUT} + 1.6 V (whichever is greater)		75		dB
SVR_{BIAS}	V_{BIAS} supply voltage rejection	V_{BIAS} = 2.9 V or V_{OUT} + 1.8 V (whichever is greater) +/- V_{RIPPLE} V_{RIPPLE} = 0.2 V freq = 1 kHz I_{OUT} = 150 mA; V_{IN} = $V_{OUT(NOM)}$+ 0.5 V		76		dB
I_{BIAS}	V_{BIAS} operating current	I_{OUT} = 0 mA; V_{BIAS} = 2.7 V		27	40	µA
$I_{Standby-BIAS}$	V_{BIAS} standby current	V_{BIAS} input current in OFF MODE: V_{EN} = GND		0.03	1	µA
$I_{Standby-IN}$	V_{IN} standby current	V_{IN} input current in OFF MODE: V_{EN} = GND		0.03	1	µA
I_{LIM}	Output current limit	V_{OUT}= 0.9 x $V_{OUT(NOM)}$	550	700	1000	mA
I_{SC}	Short-circuit current	V_{OUT} = 0 (foldback protection)		365	500	mA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{ON}	Output voltage discharge MOSFET			110		Ω
V_{EN}	Enable input logic low				0.4	V
	Enable input logic high		0.9			
I_{EN}	Enable pin input current	V_{EN} = 5.5 V			400	nA
T_{ON} (2)	Turn on time	$V_{OUT(NOM)}$ = 1.0 V		110		µs
T_{SHDN}	Thermal shutdown			160		°C
	Hysteresis			20		
C_{OUT}	Output capacitor		1	2.2	22	µF

1. *Not applicable for $V_{OUT(NOM)}$ ≥ 5.0 V.*
2. *Turn-on time is time measured between the enable input just exceeding V_{EN} high value and the output voltage just reaching 98% of its nominal value.*

Note: Values over the temperature range are guaranteed by design and correlation and not tested in production.

6 Application information

6.1 VBIAS pin voltage requirements

The bias input is the supply of the internal driving and control circuitry. In order to ensure proper biasing of the N-channel power element, the bias pin must have a minimum voltage of 2.4 V and 1.6 V (typically) higher than the output. If V_{IN} supply voltage meets these requirements then the bias pin can be tied to V_{IN}.

6.2 Output discharge function

The LD56050 integrates a MOSFET connected between V_{OUT} and GND. This transistor is activated when the EN pin goes to low logic level and has the function to quickly discharge the output capacitor when the device is disabled by the user.

6.3 Short circuit and current limitation

The LD56050 is protected against short-circuit on the output. The load current is limited to the maximum value of I_{LIM} when V_{OUT} is equal to 90% of its nominal value. If the V_{OUT} decreases even more due to a lower output load resistance then the foldback circuit starts operating limiting the current to I_{SC} when V_{OUT} = 0.

6.4 Thermal protection

Thermal protection acts when the junction temperature reaches 160 °C typical. At this point the output of the IC shuts down. As soon as the junction temperature falls below the thermal hysteresis value the device starts working again.

In order to calculate the maximum power that the device can dissipate, keeping the junction temperature below the maximum operating value, the following formula is used:

$P_{DMAX} = (85 - T_{AMB}) / R_{thJA}$

6.5 Input and output capacitors

The LD56050 requires external capacitors to assure the regulator control loop stability.

Any good quality ceramic capacitor can be used but, the X5R and the X7R are suggested since they guarantee a very stable combination of capacitance and ESR across the temperature range.

Locating the input/output capacitors as close as possible to the relative pins is recommended. The LD56050 requires a V_{IN} capacitor with a minimum value of 1 µF and a V_{BIAS} capacitor of 100 nF minimum. These capacitors must be located as close as possible to the input pins of the device and returned to a clean analog ground.

The control loop is designed to be stable with any good quality output ceramic capacitor (such as X5R/X7R types) with a minimum value of 1.0 µF and equivalent series resistance in the [3 – 300 mΩ] range. It is important to highlight that the output capacitor must maintain its capacitance and ESR in the stable region over the full operating temperature, load and input voltage ranges, to assure stability. Therefore, capacitance and ESR variations must be taken into account in the design phase to ensure the device works in the expected stability region.

7 Typical characteristics

(V_{OUT} = 1.05 V ; C_{IN} = 1 µF, C_{OUT} = 2.2 µF; V_{EN} = 1 V; unless otherwise specified.)

Figure 5. V_{DROP} vs. temperature (V_{BIAS} = 2.7 V)

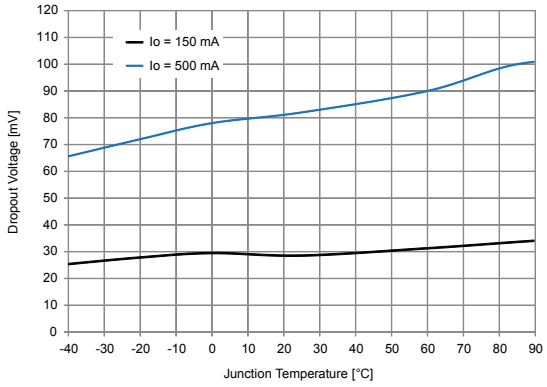


Figure 6. $V_{DROP-BIAS}$ vs. temperature (I_{OUT} = 500 mA; V_{BIAS} = V_{IN})

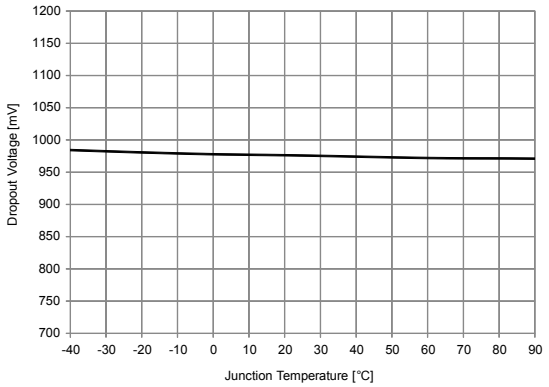


Figure 7. V_{DROP} vs. I_{OUT} (V_{BIAS} = 2.7 V)

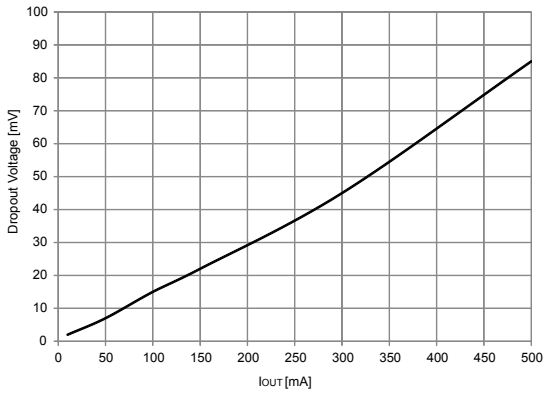


Figure 8. V_{DROP} vs. I_{OUT} (V_{BIAS} = V_{IN})

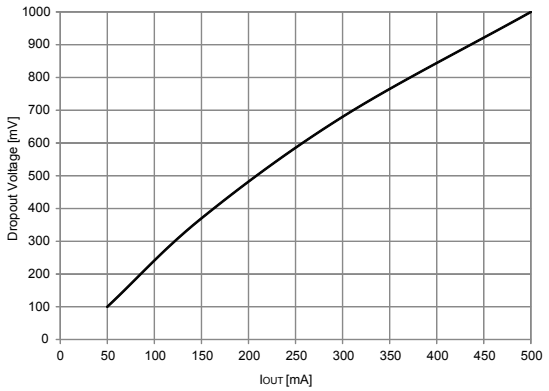


Figure 9. I_{SC} vs. temperature (V_{IN} = 1.4 V; V_{BIAS} = 2.7 V)

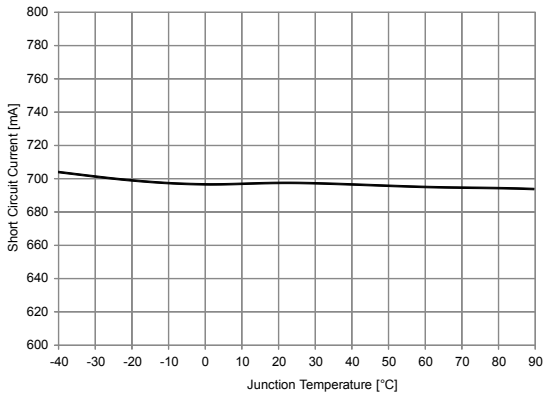


Figure 10. I_{LIM} vs. temperature (V_{IN} = 1.4 V; V_{BIAS} = 2.7 V)

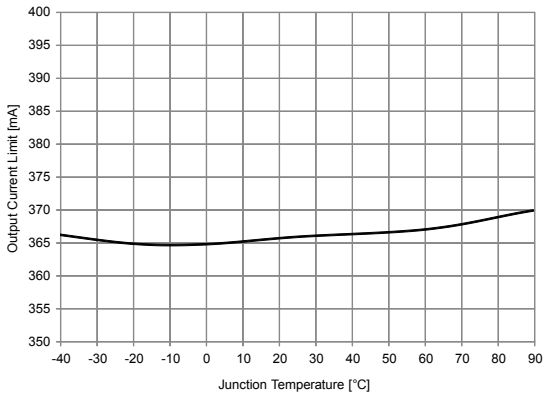


Figure 11. I_{BIAS} vs. temperature (I_{OUT} = 0 mA; V_{BIAS} = 2.7 V)

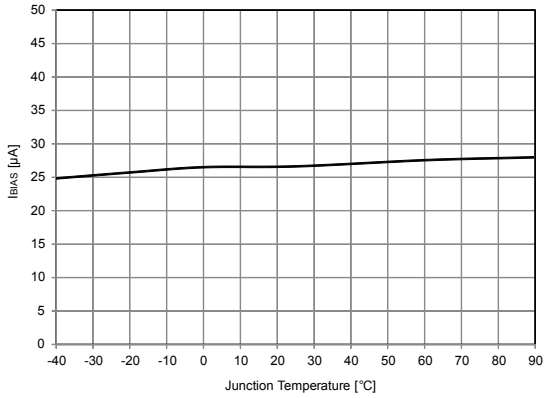


Figure 12. I_{BIAS} vs. V_{IN} (V_{BIAS} = 2.7 V)

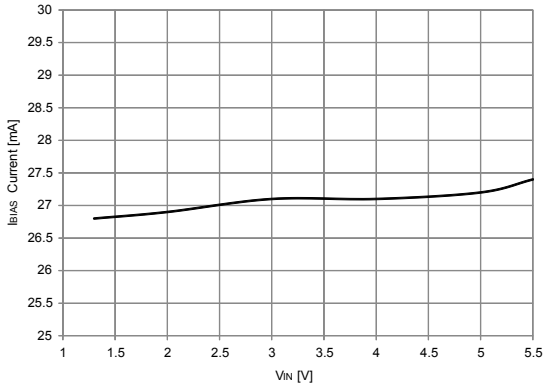


Figure 13. SVR_{IN} vs. frequency (V_{IN} = 1.5 V; V_{BIAS} = 2.7 V; V_{OUT} = 1.05 V)

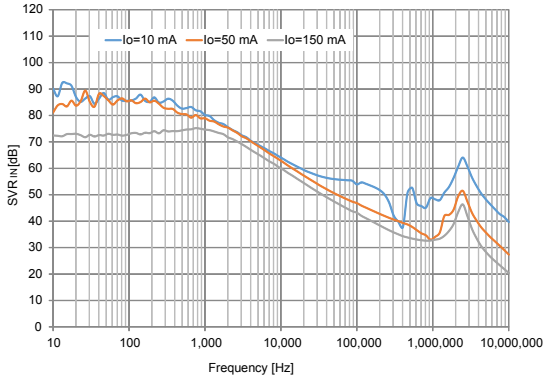


Figure 14. SVR_{BIAS} vs. frequency (V_{IN} = 1.5 V; V_{BIAS} = 2.9 V; V_{OUT} = 1.05 V)

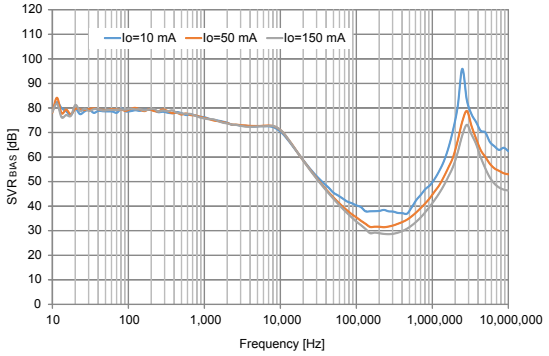


Figure 15. Noise vs. frequency (V_{IN} = 1.5 V; V_{BIAS} = 2.7 V; V_{OUT} = 1.05 V)

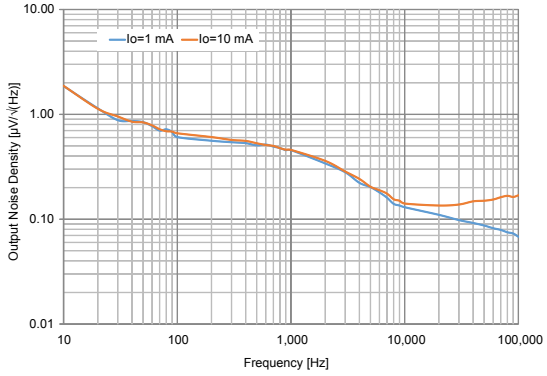


Figure 16. Output voltage vs. junction temperature

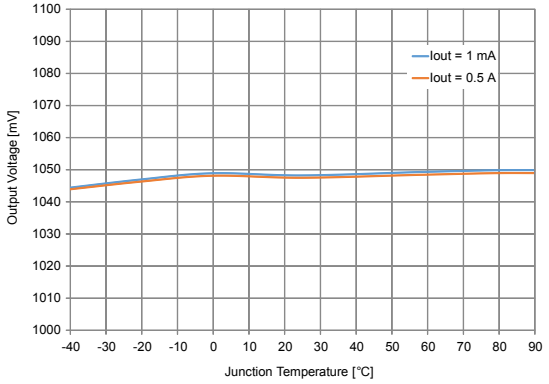


Figure 17. Turn-on time (I_{OUT} = 1 mA; V_{BIAS} = 2.7 V)

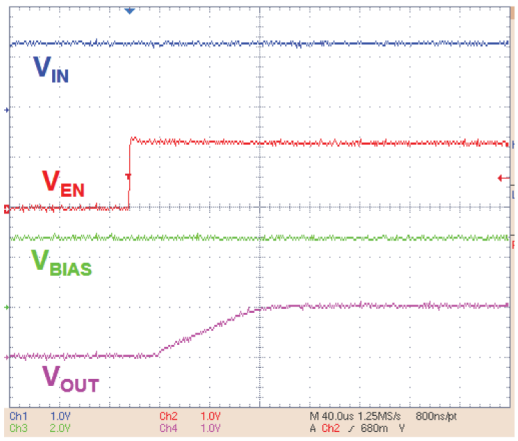


Figure 18. Turn-on time at full load (I_{OUT} = 500 mA; V_{BIAS} = 2.7 V)

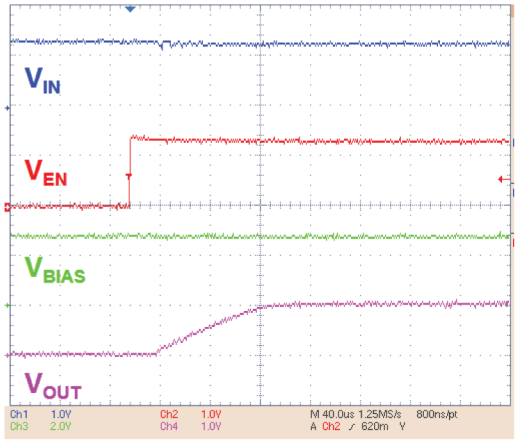


Figure 19. Line transient (V_{BIAS} = 2.7 V, V_{IN} from 1.35 V to 2.35 V; t_R = 5 µs)

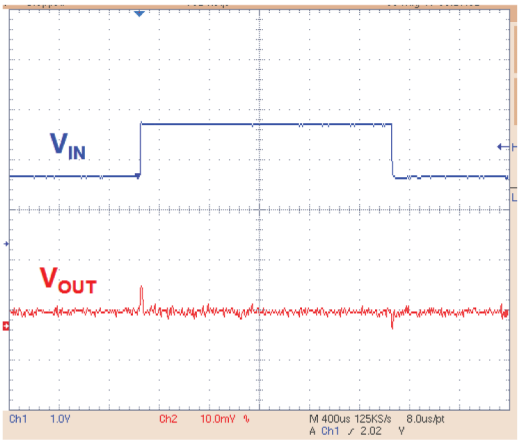
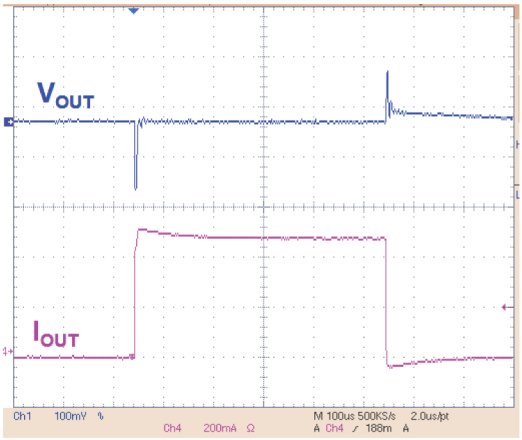


Figure 20. Load transient (V_{BIAS} = 2.7 V, V_{IN} = 1.35 V; I_{OUT} 1 to 500 mA)



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

8.1 DFN4 1.2 x 1.2 package information

Figure 21. **DFN4 1.2 x 1.2 package outline**

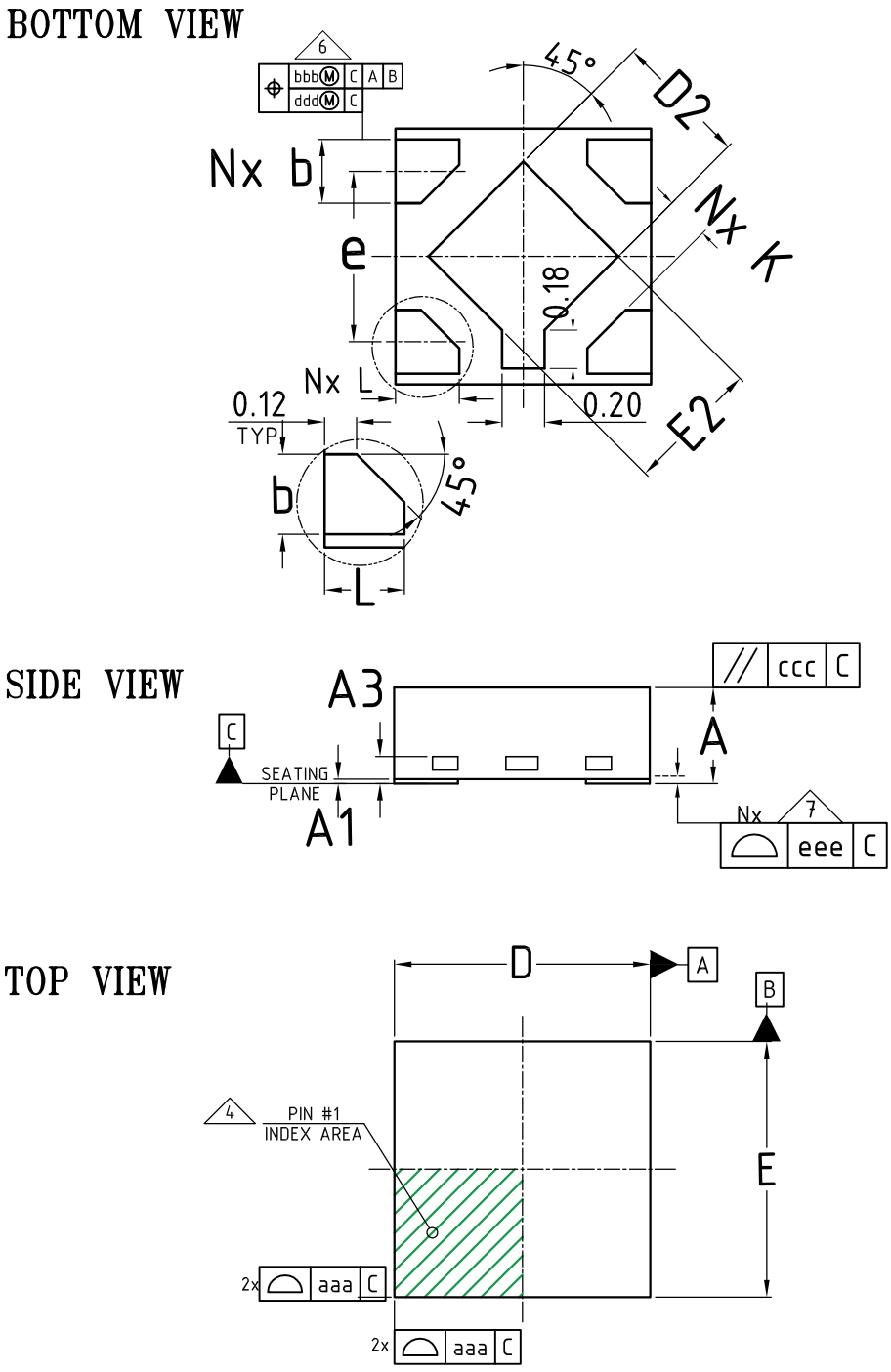
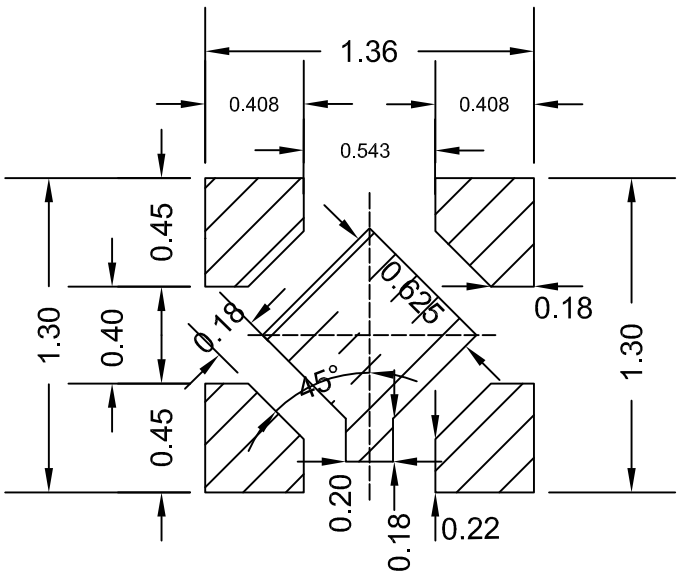


Table 7. DFN4 1.2 x 1.2 mechanical data

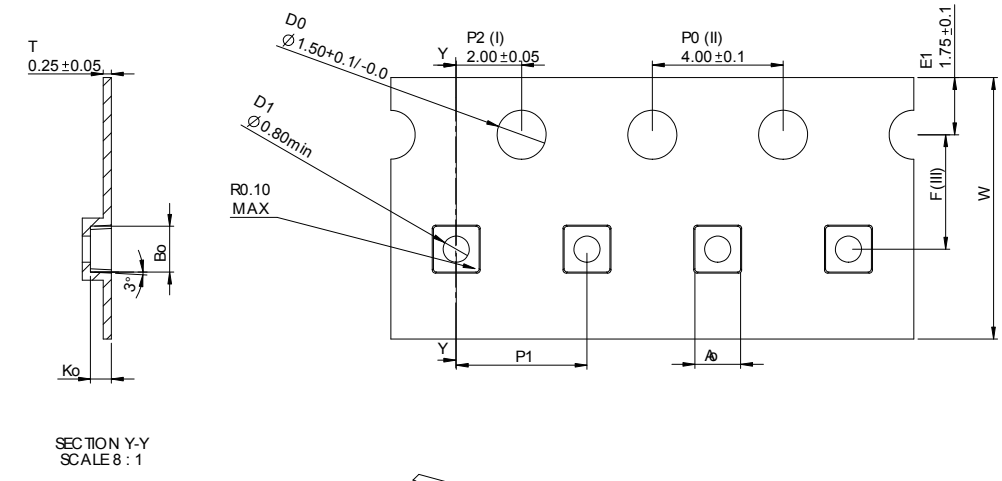
Dim.	mm.		
	Min.	Typ.	Max.
A	0.41	0.45	0.50
A1	0.00	0.02	0.05
A3		0.127 Ref.	
b	0.25	0.30	0.35
D		1.20 BSC	
E		1.20 BSC	
e		0.80 BSC	
D2	0.58	0.63	0.68
E2	0.58	0.63	0.68
K	0.20	--	--
L	0.25	0.30	0.35
N		4	
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
ND		2	

Figure 22. DFN4 1.2 x 1.2 recommended footprint



Note: All dimensions are in millimeters.

Figure 23. DFN4 1.2 x 1.2 tape and reel



Ao	1.40	+/- 0.05
Bo	1.40	+/- 0.05
Ko	0.64	+/- 0.05
F	3.50	+/- 0.05
P1	4.00	+/- 0.10
W	8.00	+/- 0.10

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Note: Pin 1 orientation: bottom-left.

9 Ordering information

Table 8. **Order code**

Order code	Discharge function	Output voltage (V)	Marking
LD56050DPU100R	Yes	1.00	UD
LD56050DPU105R	Yes	1.05	UA
LD56050DPU110R	Yes	1.10	UB
LD56050DPU115R	Yes	1.15	UE
LD56050DPU120R	Yes	1.20	UC
LD56050DPU150R	Yes	1.50	UF

Revision history

Table 9. Document revision history

Date	Revision	Changes
02-Feb-2018	1	Initial release.
09-Apr-2018	2	Updated: Figure 5. V_{DROP} vs. temperature (V_{BIAS} = 2.7 V) and Figure 6. $V_{DROP-BIAS}$ vs. temperature (I_{OUT} = 500 mA; V_{BIAS} = V_{IN}). Added: Figure 16. Output voltage vs. junction temperature .

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