Implementing the HIP1011 in the CompactPCI™ Hot Swap Application

This application offers to the CompactPCI peripheral and system board designer under voltage and programmable over current protection, soft start ramp turn on for all four supplies and simultaneous latch off upon fault detection.

Figure 1 illustrates the HIP1011 CompactPCI Hot Swap implementation. The shaded components are the external components necessary to accomplish both controlled power up and provide reset of the board upon fault.

Because of the staggered pin length CompactPCI connector, the ground connection is made first as the board is inserted into the slot. Next to engage are the four power supplies (+3.3V, +5V, ±12V), and the data and control signal lines. The HIP1011 is in control with all the power bus switches held off. Not until the board is fully inserted does the HIP1011 turn on the power bus switches connecting the board to the power bus.

How does this Application of the HIP1011 in the CompactPCI Hot Swap Environment Work?

Insertion Sequence

As the board is inserted into the slot the ground bus plane is connected first via the longest pins referencing the HIP1011 by way of the PWRON and OCSET pins through R4 and R3 respectively. Additionally the three-state driver, U1 address line is referenced through R6

Subsequently the medium length pins engage to connect the +3.3V, +5V, +12V, -12V lines to the inputs, activating the HIP1011, and the 2 logic devices, U1 and U2. At this time the HIP1011 is in control holding off all the MOSFET

switches, as PWRON is being held low. With the logic devices powered the inverter U2 input, is pulled high putting a low on the three-state driver U1 input which is passed through to the PWRON pin.

Upon complete insertion the shortest length pin, "board present" which is tied to ground on the backplane finally engages the inverter input. The inverter output pulls high turning on the HIP1011 through U1 thus the board is fully powered only upon complete insertion.

Fault Reset

If an overcurrent or undervoltage condition is detected on the board by the HIP1011 all the switches are simultaneously switched off protecting the system, the board and its components. The master board or system controller is then notified of the fault occurrence by the FLTN signal.

Reset of the faulted card is accomplished by a positive pulse on the three-state $\overline{oe}$ input. The pulse puts U1 output into a high Z state allowing R4 to pull the HIP1011 PWRON pin low, resetting the HIP1011. The HIP1011 switches turn back on when U1 $\overline{oe}$ input returns to a low state resulting in PWRON going high. The reset pulse can be generated by either the system restart / reset to the master board or from the master board to any of the peripheral boards in the system.

Reference Material and Note on Logic Type

The HIP1011EVAL2 platform demonstrates this application. In addition, reference the HIP1011 data sheet and application note AN973 for additional information.
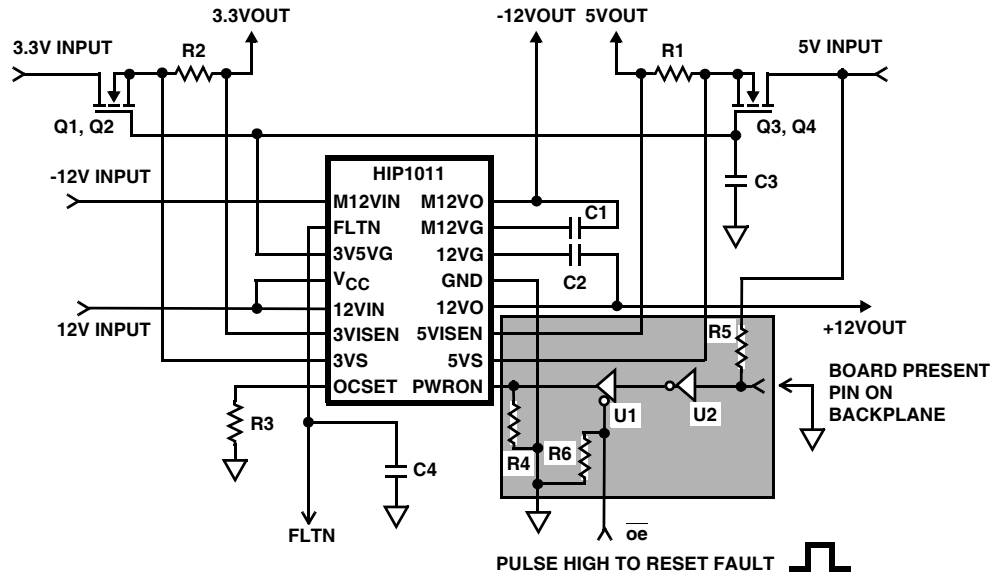
FIGURE 1.

NOTES:

1. Each test point (TP) on HIP1011EVAL2 refers to device pin number.

2. SIGNAL_GND, SHIELD_GND and SHORTPIN_GND can be jumpered together for ease of evaluation.

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