# Low Skew PCI / PCI-X Buffer

## General Description

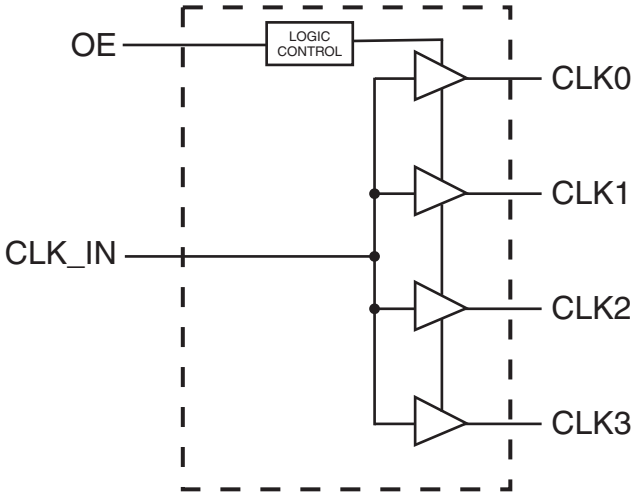
The **ICS9112-27** is a high performance, low skew, low jitter PCI / PCI-X clock driver. It is designed to distribute high speed signals in PCI / PCI-X applications operating at speeds from 0 to 140 MHz.

The **ICS9112-27** is characterized for operation from -40°C to 85°C for automotive and industrial applications.

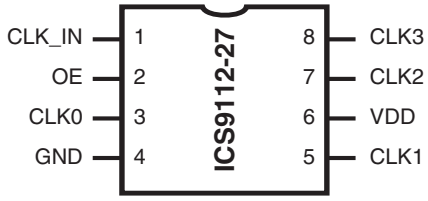
## Features

- Frequency range 0 - 140 MHz (3.3V)
- Less than 200 ps Jitter between outputs
- Skew controlled outputs < 100 ps
- Distribute one clock input to one bank of four outputs
- 3.3V ±10% operation
- Available in 8 pin TSSOP, and SOIC packages.

## Block Diagram




## Pin Configuration




**8 pin TSSOP & SOIC**

### Functionality Table

| INPUTS | | OUTPUTS |
|---|---|---|
| CLK_IN | OE | CLK(3:0) |
| 0 | 0 | Tristate |
| 0 | 1 | 0 |
| 1 | 0 | Tristate |
| 1 | 1 | 1 |

## Pin Descriptions

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | CLK_IN | IN | Input reference frequency. |
| 2 | OE | IN | Output enable. When OE is low, it tristates the clock outputs |
| 3 | CLK0 | OUT | Buffered clock output |
| 4 | GND | PWR | Ground |
| 5 | CLK1 | OUT | Buffered clock output |
| 6 | VDD | PWR | Power supply for 3.3V |
| 7 | CLK2 | OUT | Buffered clock output |
| 8 | CLK3 | OUT | Buffered clock output |

## Absolute Maximum Ratings

Supply voltage range $V_{DD}$ ..... -0.5V to 4.3 V
Input voltage range $V_I$ (see notes 1 & 2) ..... -0.5V to $V_{DD}$ + 0.5V
Output voltage range $V_O$ (see notes 1 & 2) ..... -0.5V to $V_{DD}$ + 0.5V
Input clamp current $I_{IK}$ ($V_I$< 0 or $V_I$ >$V_{DD}$) ..... ±50 mA
Output clamp current $I_{OK}$ ($V_O$< 0 or $V_O$) ..... ±50 mA
Continuous total output current, $I_O$ ($V_O$ = 0 to $V_{DD}$) ..... ±50 mA
Package thermal impedance $Ø_{JA}$ (see note 3): PW package230.5°C/W
Storage temperature rante, $T_{stg}$ ..... -65°C to 150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**Notes:**

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

### Recommended Operating Conditions

| | Min | Nom | Max | Unit |
|---|---|---|---|---|
| Supply voltage, $V_{DD}$ | 3 | 3.3 | 3.6 | V |
| High-level input voltage, $V_{IH}$ | $0.7_X V_{DD}$ | | | V |
| Low-level input voltage, $V_{IL}$ | | | $0.3_X V_{DD}$ | V |
| Input voltage, $V_I$ | 0 | | $V_{DD}$ | V |
| High-level output current, $I_{OH}$ | | | -24 | mA |
| Low-level output current, $I_{OL}$ | | | 24 | mA |
| Operating free-air temperature, $T_A$ | -40 | | 85 | °C |

### Timing requirements over recommended ranges of supply voltage and operating free-air temperature

| | Min | Nom | Max | Unit |
|---|---|---|---|---|
| Clock frequency $f_{CLK}$ | 0 | | 140 | MHz |

## Electrical Characteristics at 3.3V

$T_A$ = -40° to 85°C; Supply Voltage $V_{DD}$ = 3.3 V +/-10% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input voltage | $V_{IK}$ | $V_{DD}$ = 3.3V, $I_I$ = -18 mA | | | -1.2 | V |
| High-level Output Voltage | $V_{OH}$ | $V_{DD}$ = min to max, $I_{OH}$ = -1 mA | $V_{DD}$ - 0.2 | 3.3 | | V |
| | | $V_{DD}$ = 3V, $I_{OH}$ = -24 mA | 2 | 2.3 | | |
| | | $V_{DD}$ = 3V, $I_{OH}$ = 12 mA | 2.4 | 2.7 | | |
| Low-level Output Voltage | $V_{OL}$ | $V_{DD}$ = min to max, $I_{OH}$ = 1 mA | | 0.022 | 0.2 | V |
| | | $V_{DD}$ = 3V, $I_{OH}$ = 24 mA | | 0.61 | 0.8 | |
| | | $V_{DD}$ = 3V, $I_{OH}$ = 12 mA | | 0.31 | 0.55 | |
| High-level Input Current | $I_{OH}$ | $V_{DD}$ = 3V, $V_O$ = 1V | | -53 | -40 | mA |
| | | $V_{DD}$ = 3.3V, $V_O$ = 1.65V | | -54 | | |
| Low-level Input Current | $I_{OL}$ | $V_{DD}$ = 3V, $V_O$ = 2V | 40 | 53 | | mA |
| | | $V_{DD}$ = 3.3V, $V_O$ = 1.65V | | 57 | | |
| Input Current | $I_I$ | V = $V_O$ or $V_{DD}$ | -5 | | 5 | mA |
| Dynamic Supply Current | $I_{DD}$ | Unloaded outputs at 66.67 MHz | | 13 | 37 | mA |
| Input Capacitance[1] | $C_I$ | $V_{DD}$ = 3.3V, $V_I$ = 0V or 3.3V | | 3 | | pF |
| Output Capacitance[1] | $C_O$ | $V_{DD}$ = 3.3V, $V_I$ = 0V or 3.3V | | 3.2 | | pF |

1. Guaranteed by design, not 100% tested in production.

## Switching Characteristics at 3.3V

$T_A$ = -40° to 0 85°C; Supply Voltage $V_{DD}$ = 3.3 V +/-10% (For loading, see figures 1 and 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| High-to-low Propagation Delay[1] | $t_{PLH}$ | $V_O$ = $V_{DD}$/2 | 1.8 | 3.1 | 3.8 | ns |
| Low-to-high Propagation Delay[1] | $t_{PHL}$ | $V_O$ = $V_{DD}$/2 | 1.8 | 2.9 | 3.8 | ns |
| Output Skew Window[1] | $T_{sk}(o)$ | $V_O$ = $V_{DD}$/2 | | 50 | 100 | ps |
| Pulse Skew = $\lvert t_{PLH} - t_{PHL} \rvert$[1] | $T_{sk}(p)$ | $V_O$ = $V_{DD}$/2 | | | 300 | ps |
| Process Skew[1] | $T_{sk}(pr)$ | $V_O$ = $V_{DD}$/2 | | | 500 | ps |
| CLKIN High Time[1] | $T_{high}$ | 66 MHz | 6 | | | ns |
| | | 140 MHz | 3 | | | |
| CLKIN Low Time[1] | $T_{low}$ | 66 MHz | 6 | | | ns |
| | | 140 MHz | 3 | | | |
| Output Rise Slew Rate[1] | $T_r$ | 0.3 to 0.6 $V_{DD}$ | 1.5 | 2.1 | 4 | V/ns |
| Output Rise Slew Rate[1] | $T_f$ | 0.6 to 0.3 $V_{DD}$ | 1.5 | 2.4 | 4 | V/ns |

1. Guaranteed by design, not 100% tested in production.

## Parameter Measurement Information

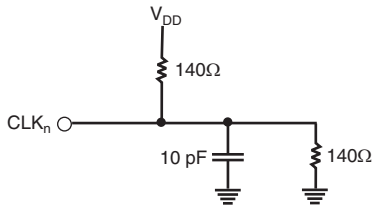



Figure 1. Test Load Circuit

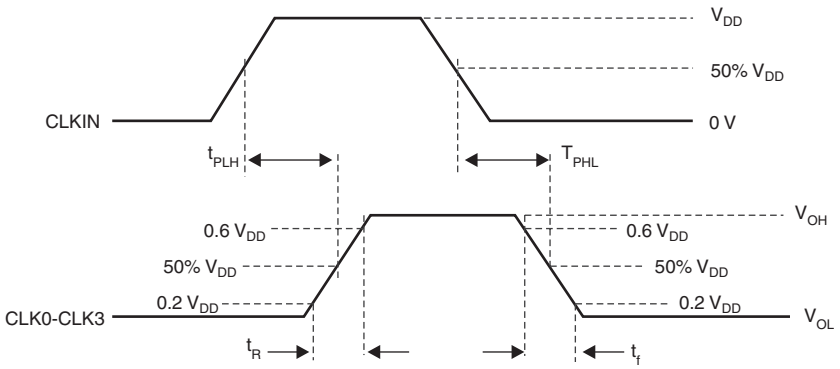



Figure 2. Voltage Thresholds for Propagation Delay ($t_{pd}$) Measurements

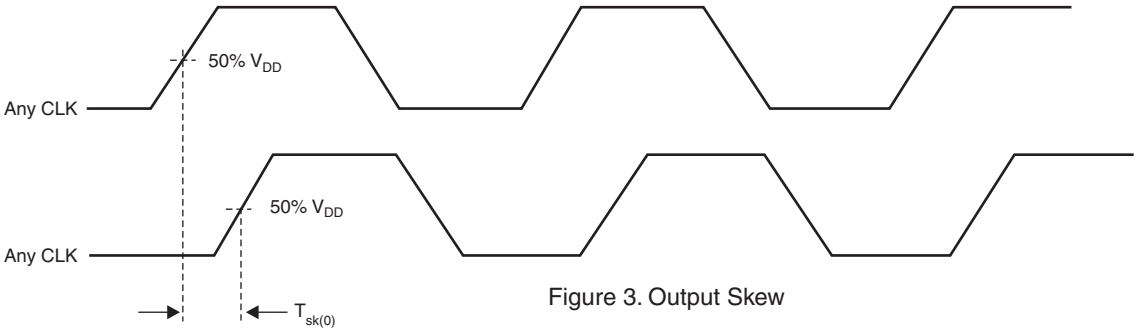



Figure 3. Output Skew

| Parameter | Value | Unit |
|---|---|---|
| $V_{IH(Min)}$ | 0.5 $V_{DD}$ | V |
| $V_{IL(Max)}$ | 0.35 $V_{DD}$ | V |
| $V_{test}$ | 0.4 $V_{DD}$ | V |

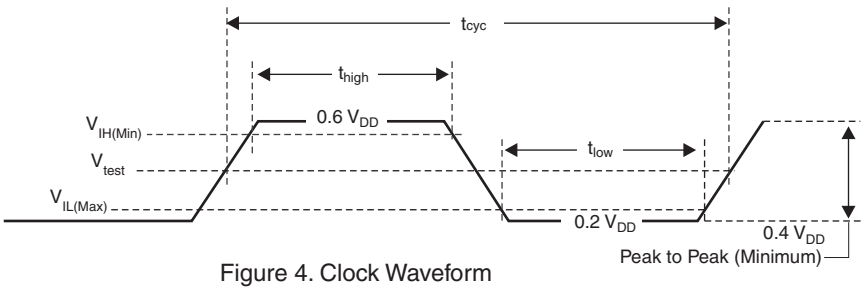
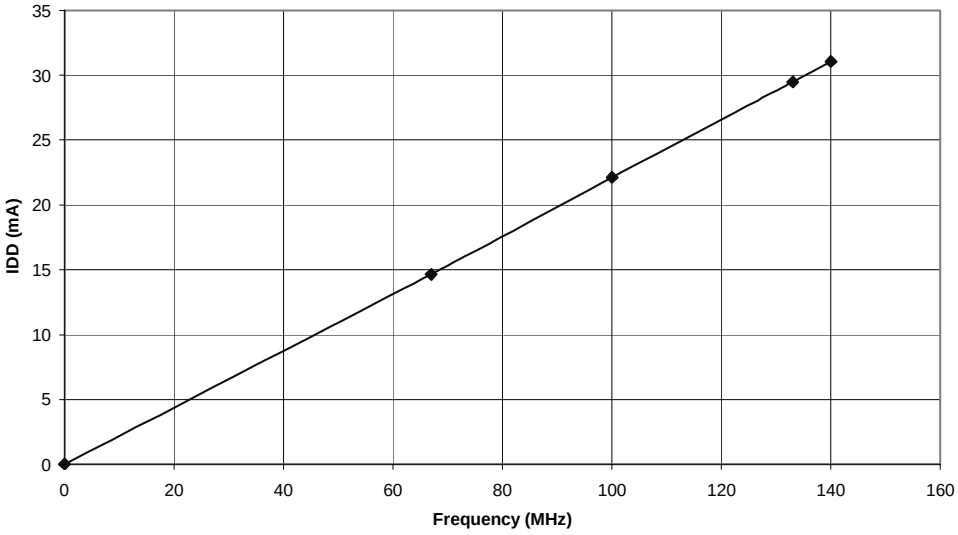


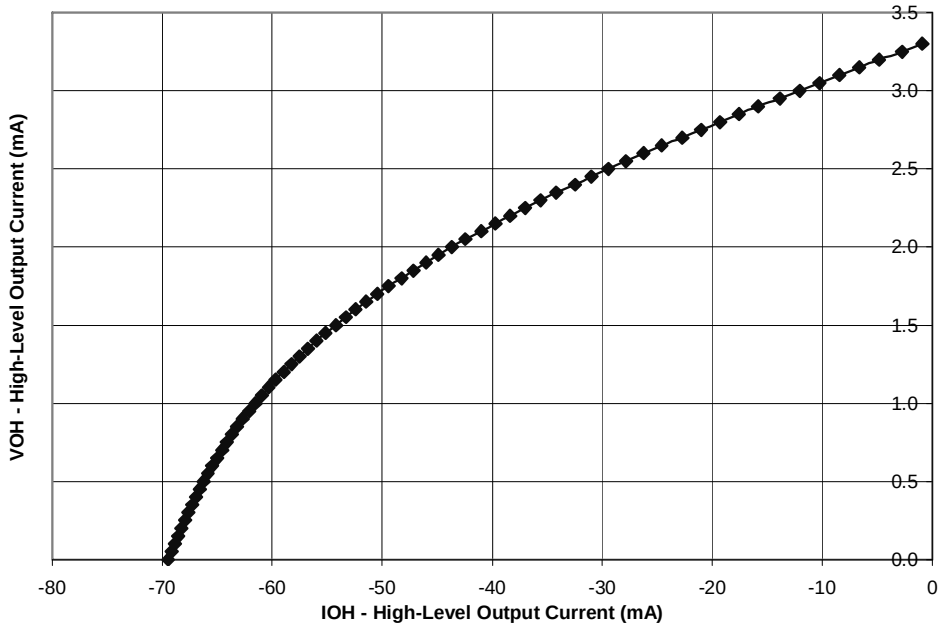

Figure 4. Clock Waveform

Note: All parameters in Figure 4 are according to PCI-X 1.0 specifications.

**ICS9112AG-27**
**SUPPLY CURRENT**
**vs.**
**FREQUENCY**
**$V_{DD}$ = 3.63 V, $T_A$ = 85°C**

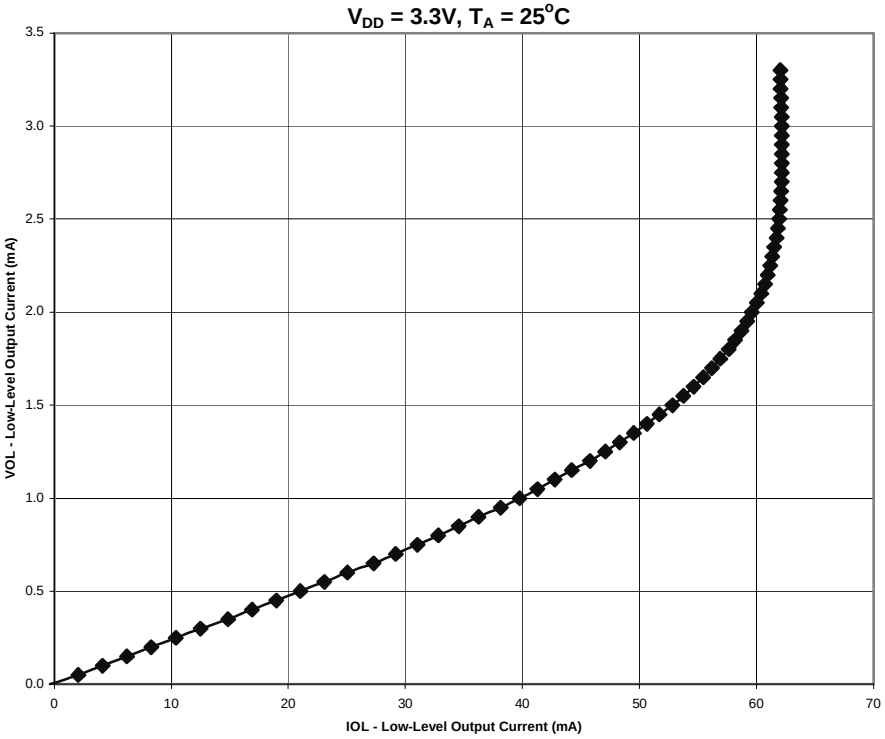


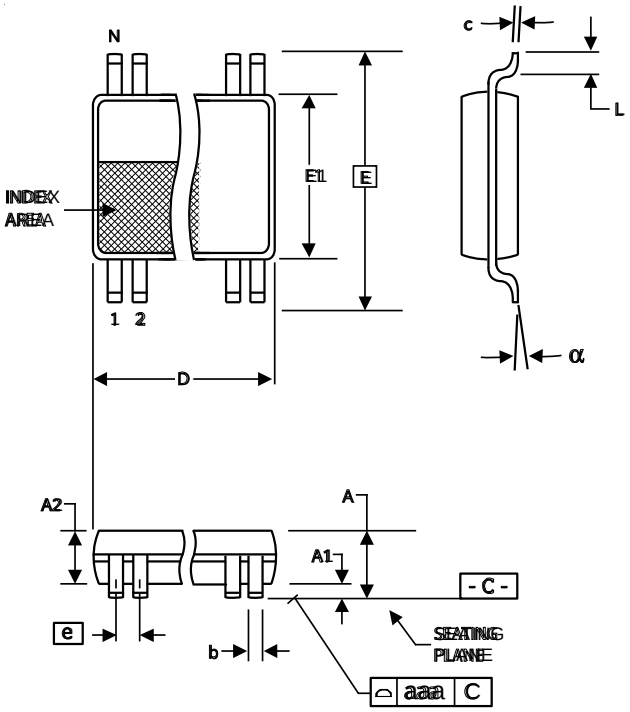

**ICS9112AG-27**
**HIGH-LEVEL OUTPUT VOLTAGE**
**vs**
**HIGH-LEVEL OUTPUT CURRENT**
**$V_{DD}$ = 3.3V, $T_A$ = 25°C**



## ICS9112AG-27

**LOW-LEVEL OUTPUT VOLTAGE**
**vs**
**LOW-LEVEL OUTPUT CURRENT**
**$V_{DD}$ = 3.3V, $T_A$ = 25°C**






**4.40 mm. Body, 0.65 mm. pitch TSSOP**
**(173 mil) (0.0256 Inch)**

**4.40 mm. Body, 0.65 mm. Pitch TSSOP**
**(173 mil) (25.6 mil)**

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.19 | 0.30 | .007 | .012 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 6.40 BASIC | | 0.252 BASIC | |
| E1 | 4.30 | 4.50 | .169 | .177 |
| e | 0.65 BASIC | | 0.0256 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | .004 |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 8 | 2.90 | 3.10 | .114 | .122 |

Reference Doc.: JEDEC Publication 95, MO-153
10-0035

## Ordering Information

**9112AG-27LFT**

Example:

**XXXX A G -YYLF T**

- **T** — **Designation for tape and reel packaging**
- **LF** — **Annealed Lead Free (Optional)**
- **YY** — **Die revision code**
- **G** — **Package Type** G = TSSOP
- **A** — **Revision Designator** (will not correlate with datasheet revision)
- **XXXX** — **Device Type**

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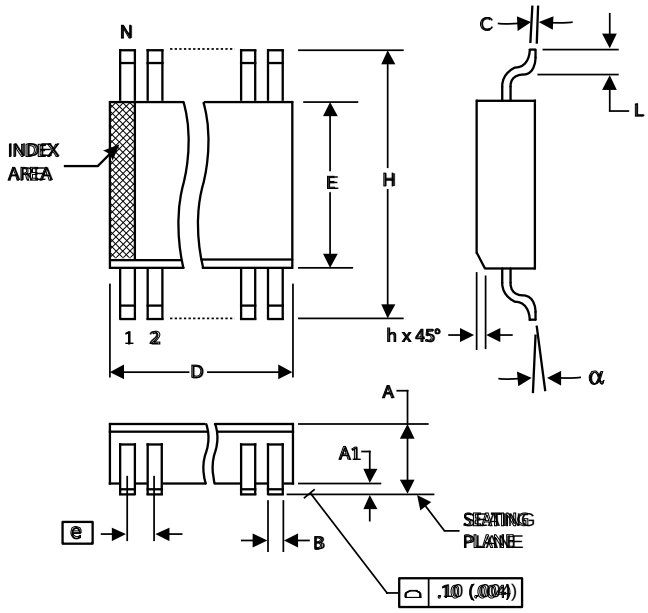


**150 mil (Narrow Body) SOIC**

**150 mil (Narrow Body) SOIC**

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | .0532 | .0688 |
| A1 | 0.10 | 0.25 | .0040 | .0098 |
| B | 0.33 | 0.51 | .013 | .020 |
| C | 0.19 | 0.25 | .0075 | .0098 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 3.80 | 4.00 | .1497 | .1574 |
| e | 1.27 BASIC | | 0.050 BASIC | |
| H | 5.80 | 6.20 | .2284 | .2440 |
| h | 0.25 | 0.50 | .010 | .020 |
| L | 0.40 | 1.27 | .016 | .050 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 8 | 4.80 | 5.00 | .1890 | .1968 |

Reference Doc.: JEDEC Publication 95, MS-012
10-0030

## Ordering Information

**9112AM-27LFT**

Example:

**XXXX A M -YYLF T**

- **Designation for tape and reel packaging**
- **Annealed Lead Free (Optional)**
- **Die revision code**
- **Package Type**
  M = SOIC
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**

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