

# P3PS550AH

## High Drive General Purpose Peak EMI Reduction IC

### Product Description

The P3PS550AH is a versatile 2.3 V to 3.6 V, Timing-Safe™, high drive spread spectrum frequency modulator designed specifically for a wide range of clock frequencies. The P3PS550AH reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of all clock dependent signals. The P3PS550AH allows significant system cost savings by reducing the number of circuit board layers ferrite beads, shielding that are traditionally required to pass EMI regulations.

### Features

- High Drive, LVCMOS Peak EMI reduction IC
- Input Clock Frequency: 18 MHz – 36 MHz
- Output Clock Frequency: 18 MHz – 36 MHz
- Eight different selectable Spread options
- Power Down option for power save
- Supply Voltage: 2.3 V – 3.6 V
- 8-pin WDFN, 2 mm x 2 mm (TDFN) Package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

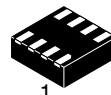
### Applications

- The P3PS550AH is targeted towards consumer electronic applications.



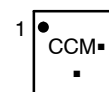
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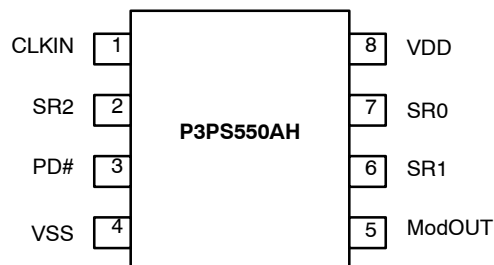
WDFN8  
CASE 511AQ

### MARKING DIAGRAMS



CC = Specific Device Code  
M = Date Code  
▪ = Pb-Free Device

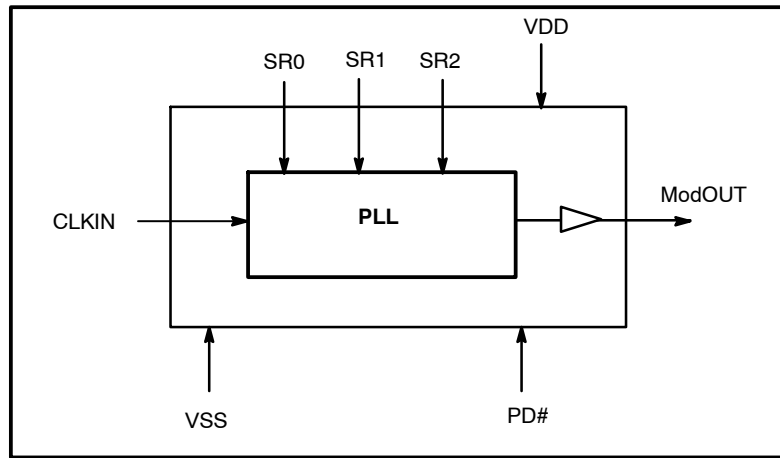
### PIN CONFIGURATION



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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**Figure 1. Block Diagram**

P3PS550AH modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum clock generation’.

P3PS550AH accepts an input from an external reference clock and locks to a 1x modulated clock output. SR0, SR1 and SR2 pins enable selecting one of the eight different frequency deviations (Refer *Frequency Deviation Selection table*). P3PS550AH also features power down option for power save. P3PS550AH operates over a supply voltage range of 2.3 V to 3.6 V. P3PS550AH is available in an 8 Pin WDFN, (2 mm x 2 mm) Package.

**Table 1. PIN DESCRIPTION**

Pin#	Pin Name	Type	Description
1	CLKIN	I	External reference clock input.
2	SR2	I	Digital logic input used to select Spreading Range. There is NO default state. Refer <i>Frequency Deviation Selection Table</i> .
3	PD#	I	Power–down control pin. Powers down the entire chip. There is NO default state. Pull low to enable power–down mode. Connect to VDD to disable Power Down. Output Clock will be LOW when power down is enabled
4	VSS	P	Ground connection.
5	ModOUT	O	Spread Spectrum Clock Output.
6	SR1	I	Digital logic input used to select Spreading Range. This pin has an internal pull–up resistor. Refer <i>Modulation Selection Table</i> .
7	SR0	I	Digital logic input used to select Spreading Range. There is NO default state. Refer <i>Frequency Deviation Selection Table</i> .
8	VDD	P	Power supply for the entire chip

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**Table 2. FREQUENCY DEVIATION SELECTION TABLE**

SR2	SR1	SR0	Spreading Range (± %) (@ 24 MHz)
0	0	0	1
0	0	1	2.5
0	1	0	1.25
0	1	1	1.5
1	0	0	0.4
1	0	1	0.75
1	1	0	1.75
1	1	1	2

**Table 3. OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>DD</sub>	Supply Voltage with respect to V <sub>SS</sub>	2.3	3.6	V
T <sub>A</sub>	Operating temperature	-20	+85	°C
C <sub>L</sub>	Load Capacitance		15	pF
C <sub>IN</sub>	Input Capacitance		7	pF

**Table 4. ABSOLUTE MAXIMUM RATING**

Symbol	Parameter	Rating	Unit
V <sub>DD</sub> , V <sub>IN</sub>	Voltage on any input pin with respect to V <sub>SS</sub>	-0.5 to +4.6	V
T <sub>STG</sub>	Storage temperature	-65 to +125	°C
T <sub>s</sub>	Max. Soldering Temperature (10 sec)	260	°C
T <sub>J</sub>	Junction Temperature	150	°C
T <sub>DV</sub>	Static Discharge Voltage (As per JEDEC STD22-A114-B)	2	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 5. DC ELECTRICAL CHARACTERISTICS**

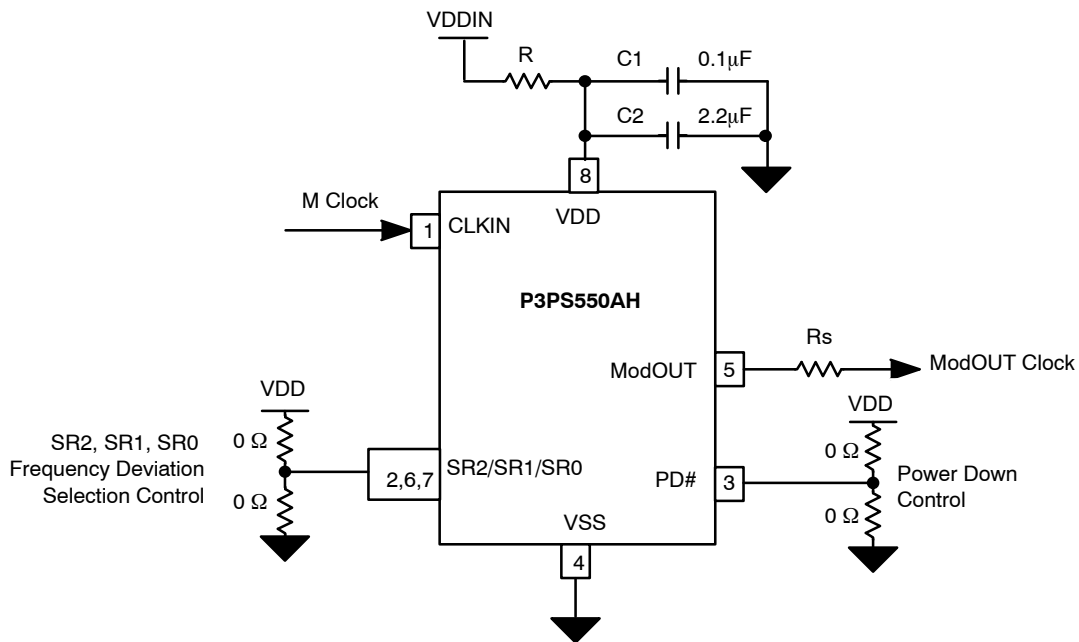
Symbol	Parameter	Min	Typ	Max	Unit
V <sub>DD</sub>	Supply Voltage with respect to V <sub>SS</sub>	2.3	2.8	3.6	V
V <sub>IH</sub>	Input high voltage	0.65 * V <sub>DD</sub>			V
V <sub>IL</sub>	Input low voltage			0.3 * V <sub>DD</sub>	V
I <sub>IH</sub>	Input high current (SR1 control pin)			50	μA
I <sub>IL</sub>	Input low current (SR1 control pin)			50	μA
V <sub>OH</sub>	Output high voltage (I <sub>OH</sub> = - 16 mA)	0.75 * V <sub>DD</sub>			V
V <sub>OL</sub>	Output low voltage (I <sub>OL</sub> = 16 mA)			0.2 * V <sub>DD</sub>	V
I <sub>CC</sub>	Static supply current (PD# pulled to V <sub>SS</sub> )			1	μA
I <sub>DD</sub>	Dynamic supply current (Unloaded Output @ 24 MHz)		6	9	mA
Z <sub>OUT</sub>	Output impedance		20		Ω

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**Table 6. AC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Min	Typ	Max	Unit
CLKIN	Input Clock frequency	18	24	36	MHz
ModOUT	Output Clock frequency	18	24	36	MHz
$t_{LH}$ (Note 1)	Output rise time (Measured between 20% to 80%)	Unloaded Output	0.4	0.8	ns
		$C_L = 15$ pF	1.4	2.2	
$t_{HL}$ (Note 1)	Output fall time (Measured between 80% to 20%)	Unloaded Output	0.3	0.6	ns
		$C_L = 15$ pF	1.1	1.9	
$t_{JC}$ (Note 1)	Jitter (cycle to cycle) Unloaded Output		$\pm 175$	$\pm 250$	ps
$t_D$ (Note 1)	Output duty cycle	45	50	55	%
$t_{ON}$ (Note 1)	PLL lock Time (Stable power supply, valid clock presented on CLKIN pin, PD# toggled from Low to High)			3	ms
$fd_{var}$	Frequency Deviation Variation across PVT		$\pm 2.5$	$\pm 5$	%

1. Parameter is guaranteed by design and characterization. Not 100% tested in production



NOTE: Refer Pin Description table for Functionality details.

**Figure 2. Typical Application Schematic**

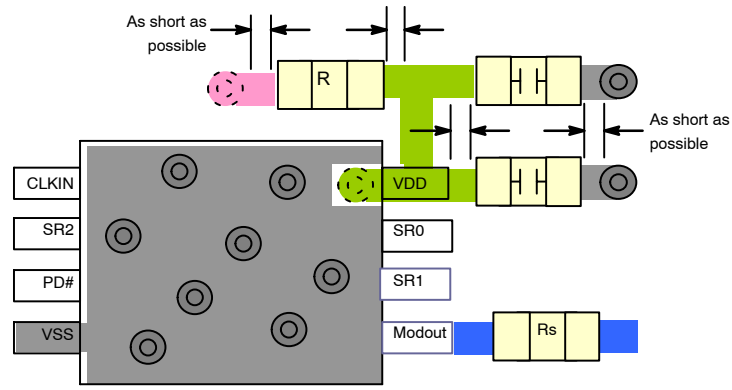
## PCB Layout Recommendation

For optimum device performance, following guidelines are recommended.

- Dedicated VDD and GND planes.
- The device must be isolated from system power supply noise. A 0.1µF and a 2.2 µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin and the ground via should be kept as short as possible. All the VDD pins should have decoupling capacitors.
- In an optimum layout all components are on the same side of the board, minimizing vias through other signal layers.

A typical layout is shown in the figure

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**Figure 3.**

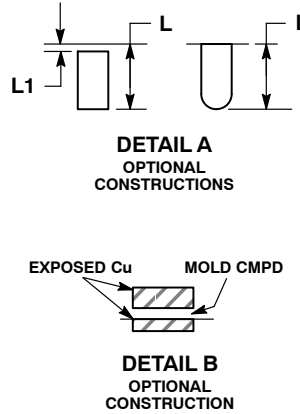
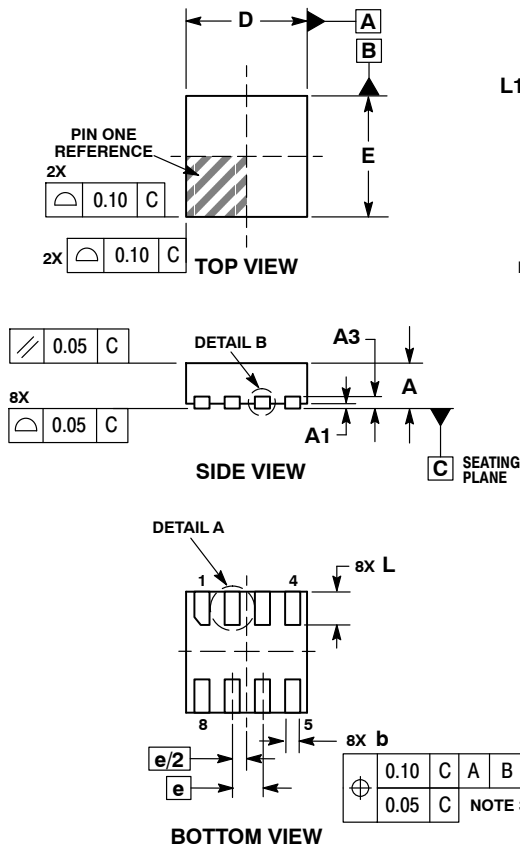
## ORDERING INFORMATION

Part Number	Top Marking	Temperature	Package Type	Shipping <sup>†</sup>
P3PS550AHG-08CR	CC	-20°C to +85°C	8-pin (2 mm x 2 mm) WDFN	Tape & Reel

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## PACKAGE DIMENSIONS

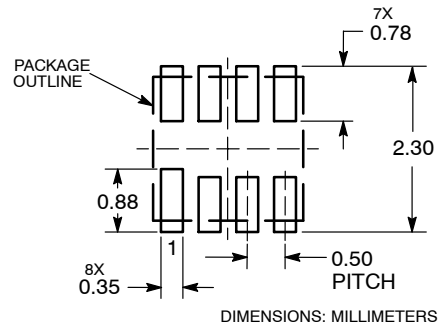
WDFN8 2x2, 0.5P  
CASE 511AQ-01  
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
E	2.00 BSC	
e	0.50 BSC	
L	0.50	0.60
L1	---	0.15

### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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