AX2061

LCD Driver for Low Multiplex Rates

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ORDERING INFORMATION

Device	Package	Shipping
AX2061−1−WD1	Wafer/Die	Contact Sales

See additional information on page 16 of this data sheet.

OVERVIEW

The AX2061 is an LCD driver for low multiplex rates. Figure 1 shows the block diagram of the AX2061. The chip is controlled by a microcontroller using the SPI interface. The microcontroller writes pixel (segment) data into the pixel data memory. Display updates may be delayed using the pixel data latches. The pixel data latches drive the segment drivers, while the row counter drives the row drivers.

Features

- Single−chip LCD Controller/Driver 5 Row, 76 Segment Outputs
- Wide Power Supply Range: from 2.2 V to 3.6 V
- 4−bit Contrast Register
- Selectable Row Drive Configuration: Static or 2/3/4/5 Row Multiplexing
- Internal Generation of LCD Bias Voltages with Charge Pump from a Single 2.2 to 3.6 V Power Supply
- 76 × 5−bit RAM for Display Data Storage
- Auto−incremented Display Data Loading
- Low Power Consumption
- Internal 32 kHz Oscillator
- SPI−Bus Interface

BLOCK DIAGRAM

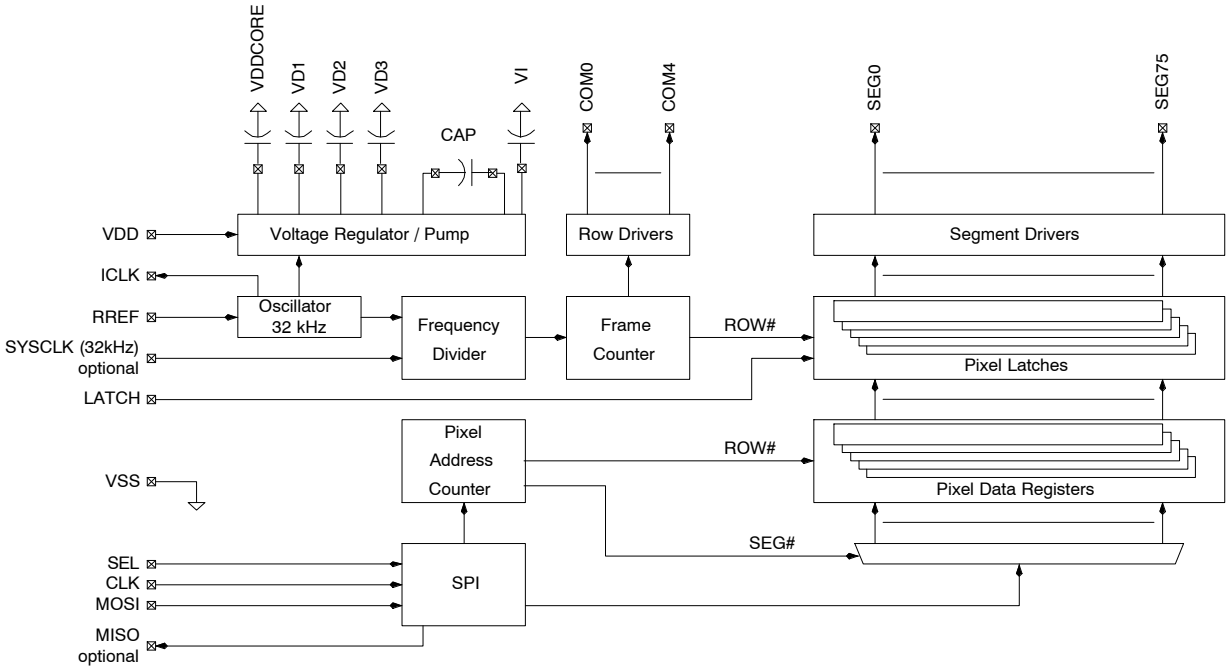


Figure 1. Functional Block Diagram of the AX2061

Table 1. PIN FUNCTION DESCRIPTIONS

Symbol	Number of Pins	Type	Description
COM0−4	5	A	Row driver outputs
SEG0−75	76	A	Segment driver outputs
SEL	1	I	SPI select
CLK	1	I	SPI clock
MISO	1	O	SPI data output Can optionally be connected to read back register contents from the AX2061. Reading registers is not required for the AX2061 functionality.
MOSI	1	I	SPI data input
LATCH	1	I/O	Latch pixel data into pixel latches For alternative functionalities as well as required handling if not used see the circuit description section
SYSCLK	1	I/O	32 kHz clock input (default) For alternative functionalities as well as required handling if not used see the circuit description section
ICLK	1	I/O	Internal 32 kHz clock output For alternative functionalities as well as required handling if not used see the circuit description section
RREF	1	A	Reference resistor for internal 32kHz oscillator Connect 1 MΩ from RREF pin to VSS Note that the reference resistor is required even if the internal 32 kHz oscillator is not used to generate the framing clock
VD1	2	A	Decoupling output for internally generated LCD voltage VD1 Connect 100 nF capacitor from VD1 to VSS
VD2	2	A	Decoupling output for internally generated LCD voltage VD2 Connect 220 nF capacitor from VD2 to VSS
VD3	2	A	Decoupling output for internally generated LCD voltage VD3 Connect 100 nF capacitor from VD3 to VSS
VI	2	A	Decoupling output for internal charge pump Connect 1 μF capacitor from VI to VSS, note that voltage levels on this pin can reach up to 5.2 V
VDD	2	P	Supply voltage input
VDDCORE	2	A	Decoupling output for internally generated supply voltage for the core functionality of the IC Connect 1 μF capacitor from VDDCORE to VSS
CAPN	2	A	Charge pump floating capacitor negative terminal Connect 100 nF capacitor between CAPN and CAPP
CAPP	2	A	Charge pump floating capacitor positive terminal Connect 1 μF capacitor between CAPN and CAPP
VSS	10	P	Ground
TST	1	N	Pin used for production testing, leave unconnected
Total	116		

A = analog input
I = digital input signal
O = digital output signal
I/O = digital input/output signal
N = not to be connected
P = power or ground

All digital inputs are Schmitt trigger inputs, digital input and output levels are LVCMOS/LVTTL compatible and 5 V tolerant.

Table 2.

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	SEG0	30	SEG29	59	ICLK	88	SEG47
2	SEG1	31	SEG30	60	SYSCLK	89	SEG48
3	SEG2	32	SEG31	61	LATCH	90	SEG49
4	SEG3	33	SEG32	62	MOSI	91	SEG50
5	SEG4	34	SEG33	63	MISO	92	SEG51
6	SEG5	35	SEG34	64	TST	93	SEG52
7	SEG6	36	COM0	65	VD1	94	SEG53
8	SEG7	37	COM1	66	VD1	95	SEG54
9	SEG8	38	COM2	67	VSS	96	SEG55
10	SEG9	39	COM3	68	RREF	97	SEG56
11	SEG10	40	COM4	69	VSS	98	SEG57
12	SEG11	41	VDD	70	VD2	99	SEG58
13	SEG12	42	VDD	71	VD2	100	SEG59
14	SEG13	43	VSS	72	VSS	101	SEG60
15	SEG14	44	VSS	73	VSS	102	SEG61
16	SEG15	45	VDDCORE	74	VD3	103	SEG62
17	SEG16	46	VDDCORE	75	VD3	104	SEG63
18	SEG17	47	VSS	76	SEG35	105	SEG64
19	SEG18	48	VSS	77	SEG36	106	SEG65
20	SEG19	49	VI	78	SEG37	107	SEG66
21	SEG20	50	VI	79	SEG38	108	SEG67
22	SEG21	51	VSS	80	SEG39	109	SEG68
23	SEG22	52	VSS	81	SEG40	110	SEG69
24	SEG23	53	CAPN	82	SEG41	111	SEG70
25	SEG24	54	CAPN	83	SEG42	112	SEG71
26	SEG25	55	CAPP	84	SEG43	113	SEG72
27	SEG26	56	CAPP	85	SEG44	114	SEG73
28	SEG27	57	SEL	86	SEG45	115	SEG74
29	SEG28	58	CLK	87	SEG46	116	SEG75

SPECIFICATIONS

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Condition	Min	Max	Units
VDD_IO	Supply voltage		−0.5	5.5	V
IDD	Supply current			100	mA
P_{tot}	Total power consumption			800	mW
I_{I1}	DC current into any pin		−10	10	mA
I_O	Output Current			40	mA
V_{ia}	Input voltage digital pins		−0.5	5.5	V
V_{es}	Electrostatic handling	HBM	−2000	2000	V
T_{amb}	Operating temperature		−40	85	°C
T_{stg}	Storage temperature		−65	150	°C
T_j	Junction Temperature			150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied.
2. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Table 4. SUPPLIES

Symbol	Description	Condition	Min	Typ	Max	Units
T_{AMB}	Operational ambient temperature		−40	27	85	°C
VDD	Power supply voltage		2.2	3.0	3.6	V
I_{STB}	Total standby current	Register Settings: Reg 2 = 0x310 Reg 3 = 0x054 Reg 4 = 0x00C Reg 5 = 0x000 Reg 6 = 0x50f Reg 7 = 0x0C3 VD1, VD2, VD3, VI, VDDCORE decoupling and capacitor between CAPN and CAPP according to the section Application Information. (Note 1)		4		μA
I_{DDRUN}	Total operating current	Register Settings: Reg 2 = 0x31C Reg 3 = 0x700 Reg 4 = 0x007 Reg 5 = 0x000 Reg 6 = 0x50f Reg 7 = 0x043 VD1, VD2, VD3, VI, VDDCORE decoupling and capacitor between CAPN and CAPP according to the section Application Information.		10		μA

1. It is not recommended to use any mode with CPENA=0 as the settling time to low current consumption can be very long after CPENA is switched from 1 to 0. Recommended usage is to keep CPENA=1 even when the row and segment outputs are disabled.

Table 5. LOGIC

Symbol	Description	Condition	Min	Typ	Max	Units
Digital Inputs						
V_{T+}	Schmitt trigger low to high threshold point			1.9		V
V_{T-}	Schmitt trigger high to low threshold point			1.2		V
V_{IL}	Input voltage, low				0.8	V
V_{IH}	Input voltage, high		2.0			V
I_L	Input leakage current		−1		1	μA
Digital Outputs						
I_{OH}	Output Current, high	VDD = 3 V, V_{OH} = 2.4 V	4			mA
I_{OL}	Output Current, low	VDD = 3 V, V_{OL} = 0.4 V	4			mA

AC Characteristics

Table 6. OSCILLATOR

Symbol	Description	Condition	Min	Typ	Max	Units
f_{osc}	Internal oscillator frequency	FREQ_OSC[3:0]=0101	25	32	39	kHz
		FREQ_OSC[3:0]=1111		20		
f_{ext}	External clock input	Input at pin SYSCLK (Note 1)	0.02	32	80	kHz
N_{div}	Clock frequency divider ratio	Programmable via register DIVIDER	1		2^{22}	
R_{EXT}	External resistor	Between pin RREF and VSS (Note 2)	0.99	1	1.01	MΩ

1. The usable frequency range will depend on the characteristics of the display used.
2. AX2061 will work with less accurate resistors, but the spread of fosc will be larger.

Table 7. LCD Drive Characteristics

Unless otherwise specified: VDD = 3.0 V, VSS = 0 V, internal 32 kHz oscillator, T_{amb} = 25°C. VD1, VD2, VD3, VI, VDDCORE decoupling and capacitor between CAPN and CAPP according to the section Application Information.

Item	Symbol	Condition		Min.	Typ.	Max.	Units
LCD drive voltages	VD1	LCD segment and row pins are open−circuit	CONTRAST[3:0] = 0000	Typ. −100mV	0.98	Typ. +100mV	V
			CONTRAST[3:0] = 0001		1.00		
			CONTRAST[3:0] = 0010		1.02		
			CONTRAST[3:0] = 0011		1.04		
			CONTRAST[3:0] = 0100		1.06		
			CONTRAST[3:0] = 0101		1.09		
			CONTRAST[3:0] = 0110		1.11		
			CONTRAST[3:0] = 0111		1.13		
			CONTRAST[3:0] = 1000		1.16		
			CONTRAST[3:0] = 1001		1.19		
			CONTRAST[3:0] = 1010		1.21		
			CONTRAST[3:0] = 1011		1.24		
			CONTRAST[3:0] = 1100		1.27		
			CONTRAST[3:0] = 1101		1.30		
			CONTRAST[3:0] = 1110		1.34		
			CONTRAST[3:0] = 1111		1.38		
	VD2	LCD segment and row pins are open−circuit (without panel load)		2•VD1•0.9		2•VD1	V
	VD3	LCD segment and row pins are open−circuit		3•VD1•0.9		3•VD1	V
Common and segment voltage drop	VDR	Each common is loaded with 100 μA and each segment is loaded with 10 μA			50		mV

Table 8. SPI TIMING

Symbol	Description	Condition	Min.	Typ.	Max.	Units
Tss	SEL falling edge to CLK rising edge		10			ns
Tsh	CLK falling edge to SEL rising edge		10			ns
Tssd	SEL falling edge to MISO driving		0		10	ns
Tssz	SEL rising edge to MISO high−Z		0		10	ns
Ts	MOSI setup time		10			ns
Th	MOSI hold time		10			ns
Tst	CLK falling edge to MISO output				10	ns
Tck	CLK period		50			ns
Tcl	CLK low duration		40			ns
Tch	CLK high duration		40			ns

For a figure showing the SPI timing parameters see section Serial Interface.

CIRCUIT DESCRIPTION

Overview

Figure 1 shows the block diagram of the AX2061. The chip is controlled by a microcontroller using the SPI interface. The microcontroller writes pixel (segment) data into the pixel data memory. Display updates may be delayed using the pixel data latches. The pixel data latches drive the segment drivers, while the row counter drives the row drivers.

The pixel data latch may be controlled by a dedicated signal, or via control register writes. This allows delayed display updates. At the beginning of an update, the latch can be set to opaque. The following pixel data writes will not be visible until the latch is again set to transparent.

An on−board voltage regulator and charge pump generates all the necessary LCD voltages, namely VD1, VD2 and VD3 from VDD. A 4 bit contrast D/A converter adjusts these voltages.

Clocking may be derived either from the internal 32 kHz oscillator or via external clock inputs.

Reset

The AX2061 generates an internal power−on reset once VDDCORE has reached a level allowing safe operation of the circuit.

The device condition after power−on reset is:

- LCD voltage generation off (CPENA = 0)
- Internal 32 kHz oscillator running
- SPI ready for use
- All LCD pins driven to ground (MODE=0000)
- Pixel Data memory is undefined

After power−up it is possible to reset the device via an SPI access by writing the bit RST first to 1 then clearing it to 0.

Clock Sources

After reset the device is configured to generating the frame clock from a clock input at the pin SYSCLK. This input is passed through the frequency division system which consists of a pre−scaler and a main divider. By default the total division ratio is 1. Other division factors are set by programming the register DIVIDER.

The AX2061 contains an internal 32 kHz oscillator. This oscillator is started−up at power−on and is used to clock the charge pump for the LCD voltage generation. It can be used to derive the frame clock instead of an input via a device pin. To set this clock source DIVCLKSCRC must be set to 1.

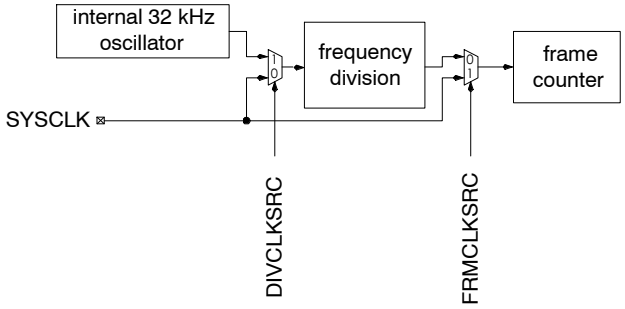


Figure 2. Frame Clocking Options

Both the device pin SYSCLK as well as the pin ICLK can be configured to output either the internal 32 kHz oscillator output, the frequency divider output or a frame synchronisation output by programming the PINCFG register. The frame synchronisation output allows multiple AX2061 devices to be synchronized. In order to synchronize multiple AX2061, one device must be the master device. The master device should output the divider clock output on SYSCLK, and the frame sync signal on ICLK. These signals should be routed to the SYSCLK and ICLK pins of the slave devices. Slave devices must be configured to accept the frame sync signal on ICLK (FRMSYNC=1) and to accept the framing clock from SYSCLK (FRMCLKSRC=1).

Unused pins must either be set to “high impedance / input” and externally be bonded to ground, or be set to “drive 0” and left unconnected.

LCD Drive Configurations

The AX2061 has 5 row terminals (COM0—COM4) and 76 segment terminals (SEG0—SEG75), so that it can drive an LCD display with a maximum of 380 (76 x 5) segments. The driving method is 1/1 duty to 1/5 duty dynamic drive with four voltages VSS, VD1, VD2 and VD3. It is also possible to set static drive. LCD display on/off can be controlled by software.

LCD Voltage Generation

The LCD drive voltages VD1−VD3 are generated by the built−in LCD system voltage circuit. The LCD system voltage circuit is turned on and off using the control register (bit CPENA).

Pixel Address to Segment / Row Mapping

The mapping between pixel addresses and rows/segments is detailed in the table below:

Table 9. MAPPING BETWEEN PIXEL ADDRESSES AND ROWS/SEGMENTS

Pixel Address									
9	8	7	6	5	4	3	2	1	0
Row Number			Segment Number						

Table 10. DETAILED MAPPING BETWEEN PIXEL ADDRESSES AND ROWS/SEGMENTS

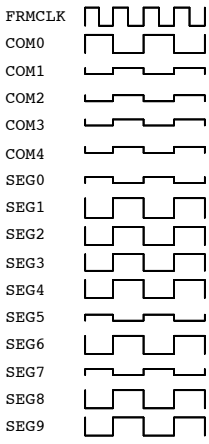
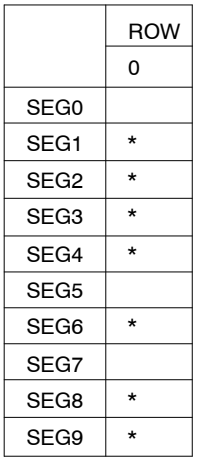
Pixel Address	Coordinate
0	Row 0, Segment 0
…	…
75	Row 0, Segment 75
76	n/a
…	…
127	n/a
128	Row 1, Segment 0
…	…
203	Row 1, Segment 75
204	n/a
…	…
255	n/a
256	Row 2, Segment 0
…	…
331	Row 2, Segment 75
332	n/a
…	…
383	n/a
384	Row 3, Segment 0
…	…
459	Row 3, Segment 75
450	n/a
…	…
511	n/a
512	Row 4, Segment 0
…	…
587	Row 4, Segment 75
488	n/a
…	…
639	n/a

Control of LCD Display and Drive Waveform

Setting of Drive Duty

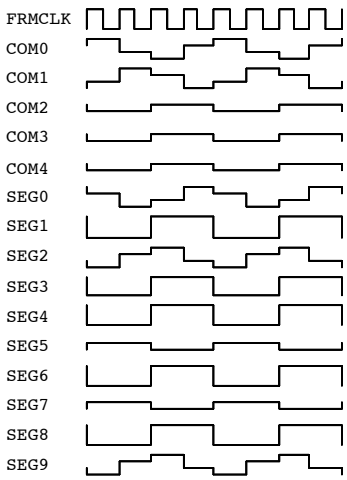
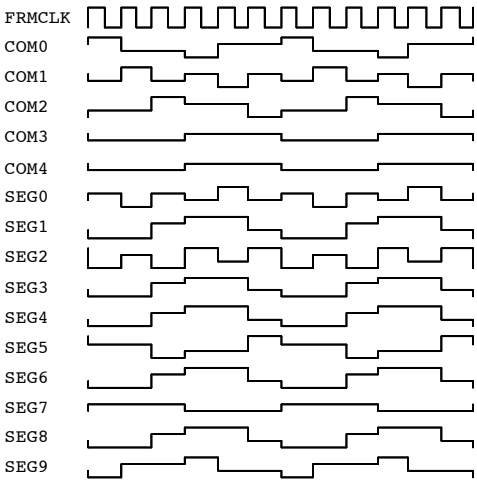
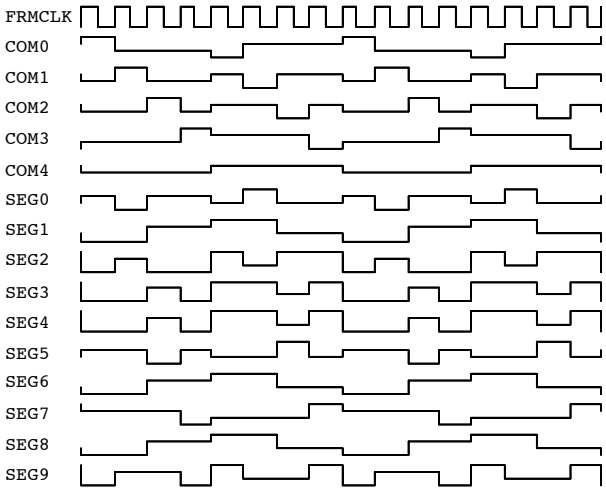
In the AX2061, the drive duty can be set to 1/1 to 1/5 using the configuration register MODE[3:0].

Table 11. WAVEFORMS

Duty	Mode	Waveform	Memory
1/1	1000		

	ROW
	0
SEG0	
SEG1	*
SEG2	*
SEG3	*
SEG4	*
SEG5	
SEG6	*
SEG7	
SEG8	*
SEG9	*

Table 11. WAVEFORMS

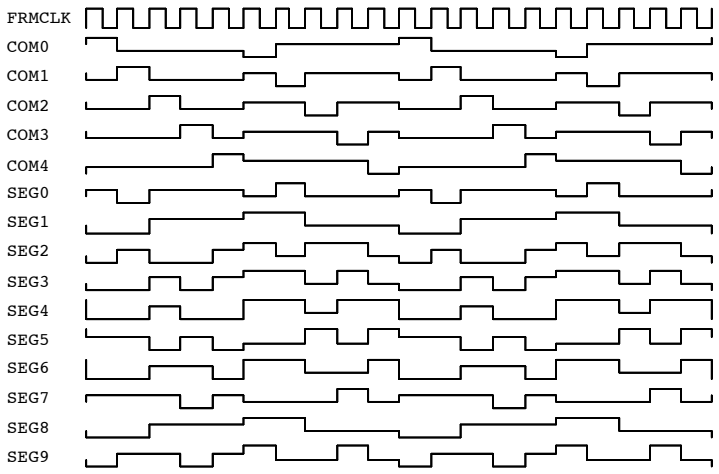
Duty	Mode	Waveform	Memory
1/2	1001		
1/3	1010		
1/4	1011		

	ROW	
	0	1
SEG0		*
SEG1	*	*
SEG2	*	
SEG3	*	*
SEG4	*	*
SEG5		
SEG6	*	*
SEG7		
SEG8	*	*
SEG9	*	

	ROW		
	0	1	2
SEG0		*	
SEG1	*	*	
SEG2	*		*
SEG3	*	*	
SEG4	*	*	
SEG5			*
SEG6	*	*	
SEG7			
SEG8	*	*	
SEG9	*		

	ROW			
	0	1	2	3
SEG0		*		
SEG1	*	*		
SEG2	*		*	*
SEG3	*	*		*
SEG4	*	*		*
SEG5			*	
SEG6	*	*		
SEG7				*
SEG8	*	*		
SEG9	*			*

Table 11. WAVEFORMS

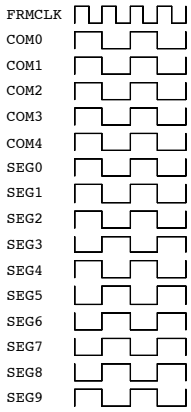
Duty	Mode	Waveform	Memory
1/5	1100		

	ROW				
	0	1	2	3	4
SEG0		*			
SEG1	*	*			
SEG2	*		*	*	
SEG3	*	*		*	
SEG4	*	*		*	*
SEG5			*		*
SEG6	*	*			*
SEG7				*	
SEG8	*	*			
SEG9	*			*	

Static Drive

The AX2061 provides software setting of the LCD static drive. Static drive can be selected using the control register MODE[3:0] field. Pixel data memory row 0 then controls the corresponding SEG waveform.

Table 12. WAVEFORMS

Mode	Waveform	Memory
0010		

	ROW
	0
SEG0	
SEG1	
SEG2	
SEG3	*
SEG4	
SEG5	*
SEG6	*
SEG7	*
SEG8	*
SEG9	

Serial Interface

The AX2061 can be programmed via a four wire serial interface according SPI using the pins CLK, MOSI, MISO and SEL. When the interface signal SEL is pulled low, a four byte command (T0−T3), followed by a variable length configuration data stream (T4−Tx) is expected on the input signal pin MOSI. Data read from the interface appears on MISO.

Reading of most registers is possible but it is never necessary for the functionality of the AX2061. This means that it is optional to connect the MOSI pin to the mater microcontroller.

Figure 3 shows a write/read access to the interface.

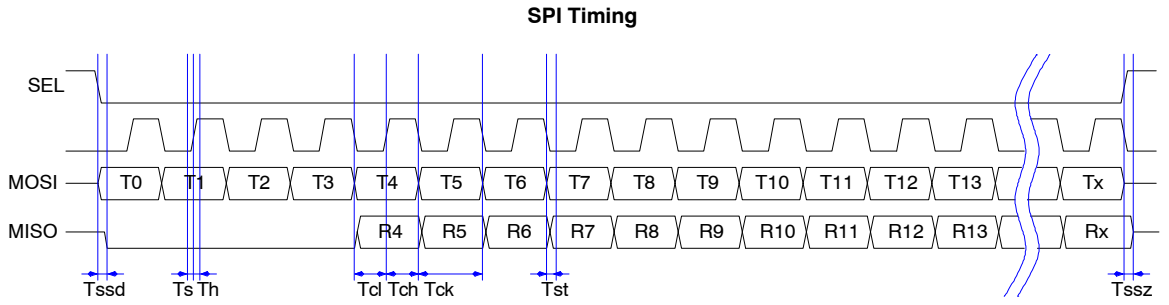


Figure 3. Serial Interface Timing

CIRCUIT DESCRIPTION

This section describes the bits of the register bank in detail.

No checks are made whether the programmed combination of bits makes sense! Bit 0 is always the LSB.

NOTE: Whole registers or register bits marked as reserved should be kept at their default values.

NOTE: All addresses not documented here must not be accessed, neither in reading nor in writing.

SPI Frame Formats

SPI transactions start with a falling edge on SEL. The first four bits indicate the command, the following bits are interpreted according to the command bits.

SPI transaction can be of variable length. The first 4 bits of each SPI transaction code the command to be executed by the AX2061. The first command bit, T0, distinguishes Write (0) from Read(1) accesses. The following three command bits (T1:T3) specify the register to access.

Even though many registers can be read as well as written, reading a register is never required for the functionality of the AX2061.

Register 000 (Pixel Data) has variable length, i.e. as many consecutive data elements as required can be read or written in a single SPI transaction. All other registers are twelve bits long.

Table 13. REGISTER OVERVIEW

Cmd	Name	Reset	Bit												Description
T1 :T2 :T3			11	10	9	8	7	6	5	4	3	2	1	0	
000	PIXELDATA	-----	PIXELDATA…												Pixel Data
010	CONFIG	0000 0001 0000	RST	–	CP ENA	DIV CLK SRC	FRM CLK SRC	FRM SYNC	LATCH[1:0]		MODE[3:0]				Configuration
011	DIVIDER	0000 0000 0000	PRESCALER[3:0]				DIVIDER[7:0]								Divider
100	CONTRAST	0000 0010 0111	REVISION[7:0]								CONTRAST[3:0]				Contrast
101	PINCFG	0111 0111 0111	LAT CHR	LATCHDRV[2:0]			SYS CLKR	SYSCLKDRV[2:0]			ICLKR	ICLKDRV[2:0]			Pin Configuration
110	INT	0101 0000 0001	reserved		CONTRAST_OFF[1 :0]		reserved				BUF_CUR[3:0]				Internal Configuration
111	OSCILLATOR	0000 0010 0011	reserved				CONF	EN_OSC_PROG	FREQ_OSC[3:0]				reserved		Oscillator frequency programming

Pixel Data Register

The first command bit, T0, distinguishes Write (0) from Read(1) accesses. The command code (T1:T2:T3 = 000) is followed by a 10 bit Pixel Address (PA), and two dummy bits. After that, Pixel Data (PD) can be read or written, one pixel at a time. The Pixel Address auto increments. An arbitrary number of consecutive pixels may be read or written in a single transaction.

Table 14. PIXEL DATA REGISTER

T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	T17	T18
0	0	0	0	Pixel Address PA(9:0)										–	–	PD(PA)	PD(PA+1)	…

For a description of the mapping between pixel addresses and rows/segments see the section Pixel address to segment / row mapping.

CONFIG Register

Table 15. CONFIG REGISTER

Name	Bits	R/W	Reset	Description
MODE	3:0	RW	0000	See table below
LATCH	5:4	RW	01	See table below
FRMSYNC	6	RW	0	When 1, the framing generator is restarted if ICLK = 1; this allows synchronisation of multiple AX2061
FRMCLKSRC	7	RW	0	Framing clock source; 0 = divider output, 1 = SYSCLK
DIVCLKSRC	8	RW	0	Divider clock source; 0 = SYSCLK, 1 = internal 32 kHz oscillator
CPENA	9	RW	0	Charge Pump Enable
RST	11	RW	0	Reset chip by writing 1 to RST, and then 0

Table 16. MODES

Bits	Meaning
0000	Off; all LCD COM and SEG pins are driven to GND
0010	Static
1000	Dynamic 1/1
1001	Dynamic 1/2
1010	Dynamic 1/3
1011	Dynamic 1/4
1100	Dynamic 1/5

Table 17. LATCH MODE

Bits	Meaning
00	Latch Opaque
01	Latch Transparent
10	The LATCH pin controls the pixel latch. Pin LATCH = 0: Opaque; pin LATCH = 1: Transparent
11	The LATCH pin controls the pixel latch. Pin LATCH = 0: Transparent; pin LATCH = 1: Opaque

DIVIDER Register

Table 18. DIVIDER REGISTER

Name	Bits	R/W	Reset	Description
DIVIDER	7:0	RW	00000000	Divider; divides the prescaler output by DIVIDER + 1
PRESCALER	11:8	RW	0000	Prescaler; divides the clock input by $2^{PRESCALER}$

The refresh frequency will be

$$f_{REFRESH} = \frac{f_{CLK}}{2^{PRESCALER}\,(\,DIVIDER + 1)}$$

(Note that this is the frequency at which drive signals change. Drive signals will repeat after 2 times the refresh period times the dynamic multiplex ratio.)

CONTRAST Register

Table 19. CONTRAST REGISTER

Name	Bits	R/W	Bits	Description
CONTRAST	3:0	RW	0111	Contrast
REVISION	11:4	R	00000001	Chip revision

For a table containing the contrast encoding see the Specifications section on LCD drive characteristics.

PINCFG Register

Table 20. PINCFG REGISTER

Name	Bits	R/W	Reset	Description
ICLKDRV	2:0	RW	111	ICLK drive mode
ICLKR	3	R	–	ICLK pad observation
SYSCLKDRV	6:4	RW	111	SYSCLK drive mode
SYSCLKR	7	R	–	SYSCLK pad observation
LATCHDRV	10:8	RW	111	LATCH drive mode
LATCHR	11	R	–	LATCH pad observation

Table 21. ICLK DRIVE MODE

Bits	Meaning
000	Drive 0
001	Drive 1
010	Internal 32 kHz oscillator clock
011	Divider output clock
100	Frame sync output
101	Latch output
111	High Impedance / Input

Table 22. SYSCLK DRIVE MODE

Bits	Meaning
000	Drive 0
001	Drive 1
010	Internal 32 kHz oscillator clock
011	Divider output clock
100	Frame sync output
101	Latch output
111	High Impedance / Input

Table 23. LATCH DRIVE MODE

Bits	Meaning
000	Drive 0
001	Drive 1
010	Internal 32 kHz oscillator clock
011	Divider output clock
100	Frame sync output
101	Latch output
111	High Impedance / Input

INT Register

Table 24. INT REGISTER

Name	Bits	R/W	Reset	Description
CONTRAST_OFF[1:0]	9:8	RW	01	Contrast offset adjustment, for Contrast bits see CONTRAST Register
BUF_CUR	3:0	RW	0001	Internal setting of the LCD Drive Voltage Buffers. MUST BE SET TO 1111.

Table 25. CONTRAST OFFSET CODING

Bits	Meaning
00	2 LSB, 40 mV offset
01	Default
10	1 LSB, 20 mV offset
11	−1 LSB, −20 mV offset

OSCILLATOR Register

Table 26. OSCILLATOR REGISTER

Name	Bits	R/W	Reset	Description
CONF	7	RW	0	MUST BE SET TO 1.
EN_OSC_PROG	6	RW	0	Enable oscillator programming. This bit must be set to high for changes of FREQ_OSC to take effect.
FREQ_OSC	5:2	R	–	Internal oscillator frequency programming.

For oscillator frequencies at specific FREQ_OSC settings, see the Specifications section on the Oscillator.

APPLICATION INFORMATION

Application Diagram with External Clocking

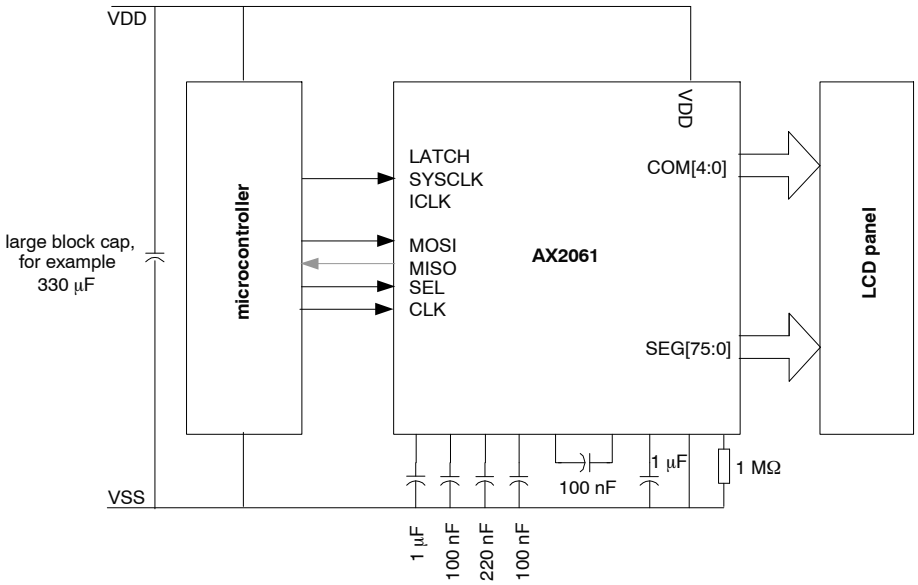


Figure 4. Application Diagram with External Clocking

The unused pins LATCH and ICLK should be either configured to drive 0 or configured to be inputs and tied to VSS.

MISO can optionally be connected to read back register contents from the AX2061. Reading registers is not required for the AX2061 functionality.

Application Diagram with Internal Clocking

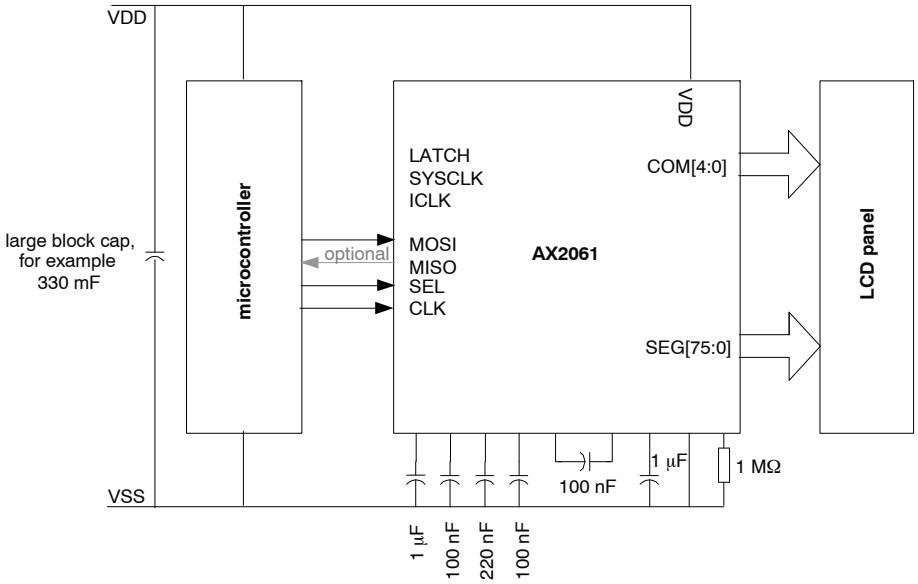


Figure 5. Application Diagram with Internal Clocking

The unused pins LATCH, ICLK and SYSCLK should be either configured to drive 0 or configured to be inputs and tied to VSS.

MISO can optionally be connected to read back register contents from the AX2061. Reading registers is not required for the AX2061 functionality.

DIE OUTLINE, PAD COORDINATES AND WAFER INFORMATION

Table 27.

Pin	X−OUT	X−IN	Y	Symbol		Pin	X−IN	X−OUT	Y	Symbol
1	40		2655	SEG0		59	956 &1126		40	ICLK
2		120 & 290	2609	SEG1		60		1206	85	SYSCLK
3	40		2563	SEG2		61	956 &1126		130	LATCH
4		120 & 290	2517	SEG3		62		1206	175	MOSI
5	40		2470	SEG4		63	956 &1126		220	MISO
6		120 & 290	2424	SEG5		64		1206	265	TST
7	40		2378	SEG6		65	956 &1126		310	VD1
8		120 & 290	2332	SEG7		66		1206	355	VD1
9	40		2285	SEG8		67	956 &1126		400	VSS
10		120 & 290	2239	SEG9		68		1206	445	RREF
11	40		2193	SEG10		69	956 &1126		490	VSS
12		120 & 290	2147	SEG11		70		1206	535	VD2
13	40		2100	SEG12		71	956 &1126		580	VD2
14		120 & 290	2054	SEG13		72		1206	625	VSS
15	40		2008	SEG14		73	956 &1126		670	VSS
16		120 & 290	1962	SEG15		74		1206	715	VD3
17	40		1915	SEG16		75	956 &1126		760	VD3
18		120 & 290	1869	SEG17		76		1206	805	SEG35
19	40		1823	SEG18		77	956 &1126		852	SEG36
20		120 & 290	1777	SEG19		78		1206	898	SEG37
21	40		1730	SEG20		79	956 &1126		944	SEG38
22		120 & 290	1684	SEG21		80		1206	990	SEG39
23	40		1638	SEG22		81	956 &1126		1037	SEG40
24		120 & 290	1592	SEG23		82		1206	1083	SEG41
25	40		1545	SEG24		83	956 &1126		1129	SEG42
26		120 & 290	1499	SEG25		84		1206	1175	SEG43
27	40		1453	SEG26		85	956 &1126		1222	SEG44
28		120 & 290	1407	SEG27		86		1206	1268	SEG45
29	40		1360	SEG28		87	956 &1126		1314	SEG46
30		120 & 290	1314	SEG29		88		1206	1360	SEG47
31	40		1268	SEG30		89	956 &1126		1407	SEG48
32		120 & 290	1222	SEG31		90		1206	1453	SEG49
33	40		1175	SEG32		91	956 &1126		1499	SEG50
34		120 & 290	1129	SEG33		92		1206	1545	SEG51
35	40		1083	SEG34		93	956 &1126		1592	SEG52
36		120 & 290	1037	COM0		94		1206	1638	SEG53
37	40		990	COM1		95	956 &1126		1684	SEG54
38		120 & 290	944	COM2		96		1206	1730	SEG55
39	40		898	COM3		97	956 &1126		1777	SEG56
40		120 & 290	852	COM4		98		1206	1823	SEG57
41	40		805	VDD		99	956 &1126		1869	SEG58
42		120 & 290	760	VDD		100		1206	1915	SEG59
43	40		715	VSS		101	956 &1126		1962	SEG60
44		120 & 290	670	VSS		102		1206	2008	SEG61
45	40		625	VDDCORE		103	956 &1126		2054	SEG62
46		120 & 290	580	VDDCORE		104		1206	2100	SEG63
47	40		535	VSS		105	956 &1126		2147	SEG64

Table 27.

Pin	X−OUT	X−IN	Y	Symbol		Pin	X−IN	X−OUT	Y	Symbol
48		120 & 290	490	VSS		106		1206	2193	SEG65
49	40		445	VI		107	956 &1126		2239	SEG66
50		120 & 290	400	VI		108		1206	2285	SEG67
51	40		355	VSS		109	956 &1126		2332	SEG68
52		120 & 290	310	VSS		110		1206	2378	SEG69
53	40		265	CAPN		111	956 &1126		2424	SEG70
54		120 & 290	220	CAPN		112		1206	2470	SEG71
55	40		175	CAPP		113	956 &1126		2517	SEG72
56		120 & 290	130	CAPP		114		1206	2563	SEG73
57	40		85	SEL		115	956 &1126		2609	SEG74
58		120 & 290	40	CLK		116		1206	2655	SEG75

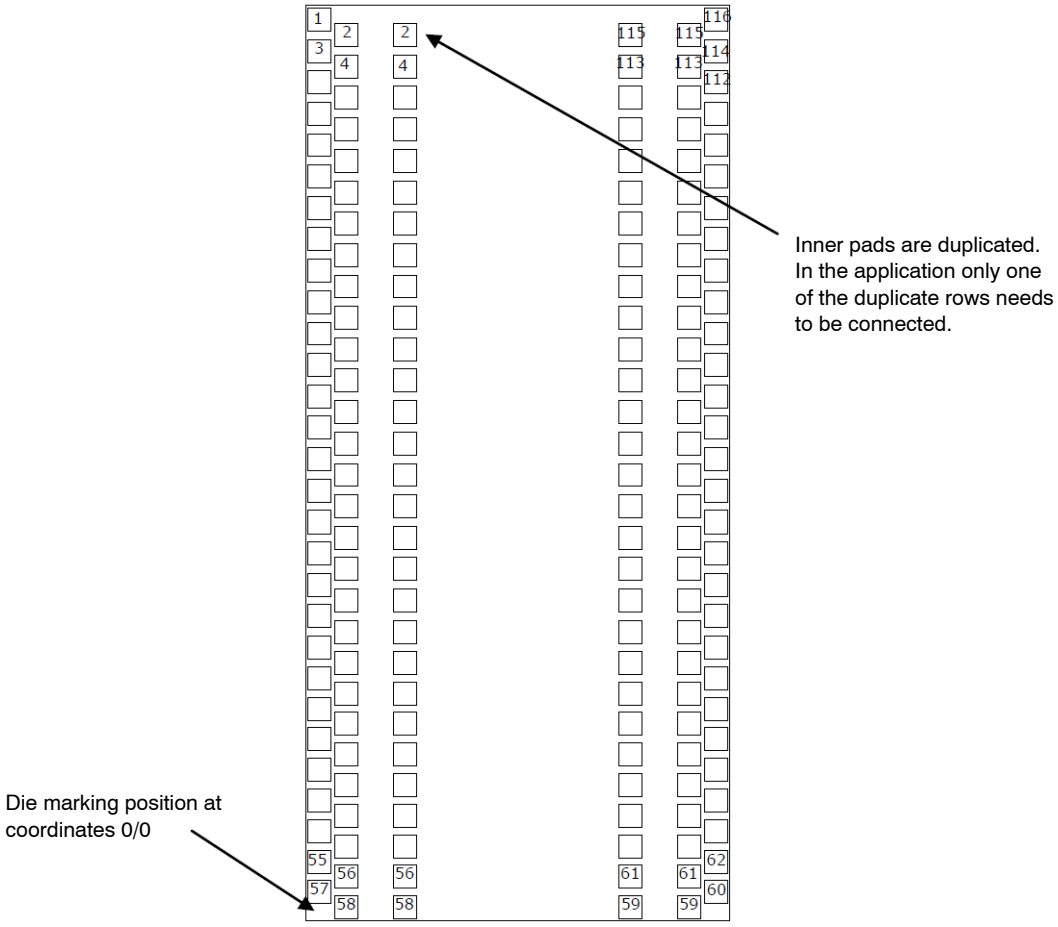


Figure 6. Pad Layout and Marking Position of the Die

Table 28.

Item	Dimension
Die pad openings	70 μm x 70 μm
Minimal pad pitch in y dimension	90 μm
Minimal pad pitch in x dimension	250 μm

Die size	1.4 mm x 2.8 mm
Wafer size	8”
Wafer thickness	19 mil
GDPW	7370
Saw lane width	100 μm

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