Rev: 102108

DS33M30 Demo Kit

General Description

The DS33M30 demo kit (DK) is an easy-to-use evaluation board for the DS33M30 Ethernet-over-SONET/SDH devices. Maxim's ChipView software is provided with the demo kit, giving point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal, queue overflow, Ethernet link, Tx/Rx, and interrupt status.

Windows is a registered trademark of Microsoft Corp.

Demo Kit Contents

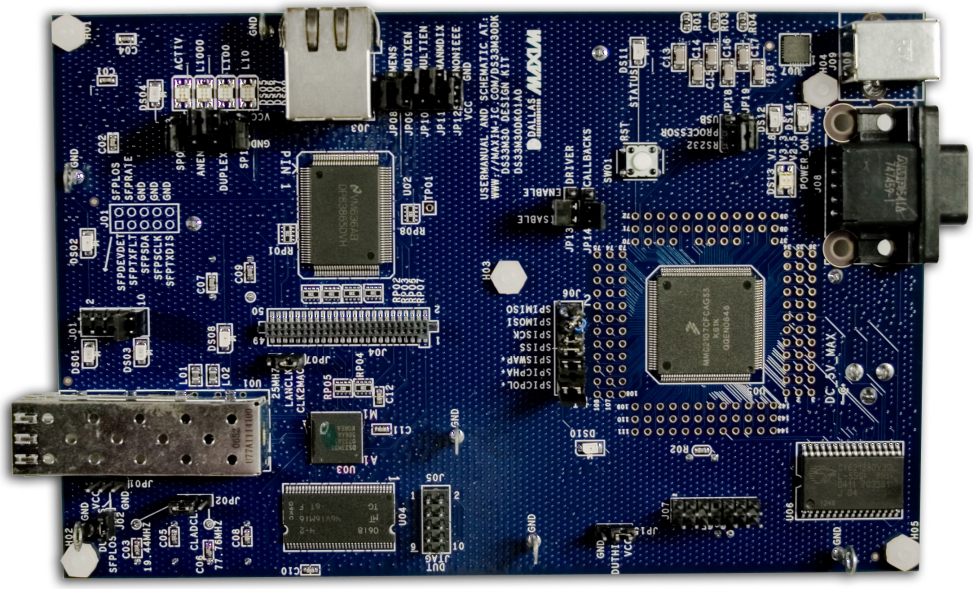
DS33M30DK Board
CD Including:
- ChipView Software
- DS33M30 Definition Files
- DS33M30DK Data Sheet
- DS33M30 Data Sheet

Features

- **Demonstrates Key Functions of DS33M30 Ethernet Transport Chipset**
- **Includes Ethernet PHY Supporting Gigabit Mode**
- **Includes Optical SFP Module for SONET/SDH Interface**
- **Network Connectors, Transformers, and Termination Ease Connectivity**
- **Careful Layout Provides Signal Integrity**
- **On-Board Processor and ChipView Software Provide Point-and-Click Access to the DS33M30 Register Set**
- **All System Side and Overhead Pins are Easily Accessible for External Data Source/Sink**
- **Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs**

Ordering Information

PART	TYPE
DS33M30DK	Demo Kit for DS33M30



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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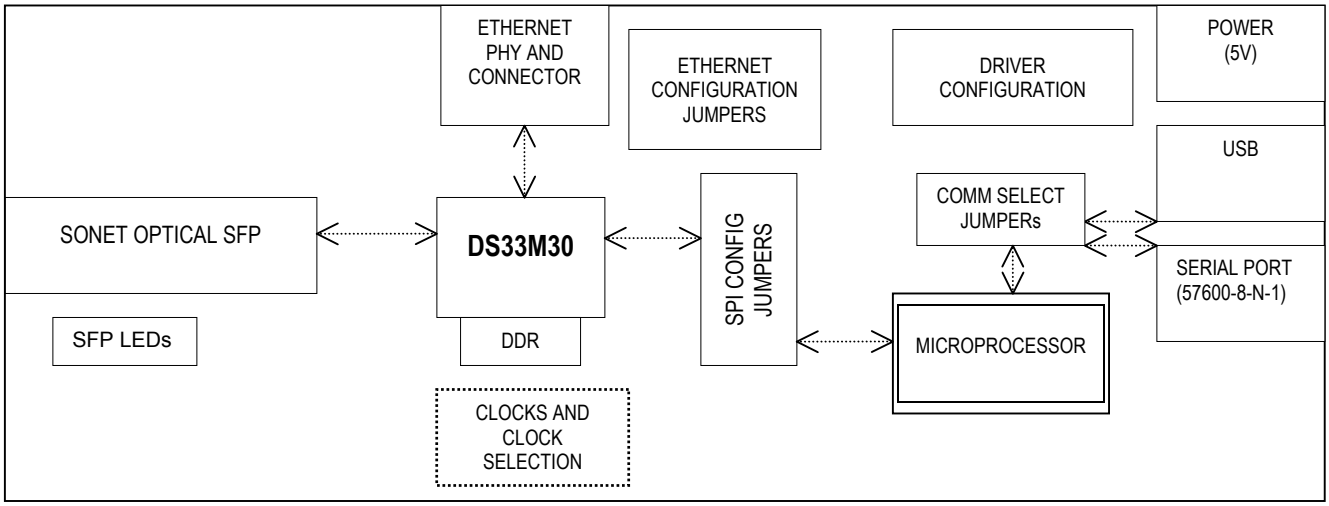
1. Board Floorplan

Figure 1-1. DS33M30DK Board Floorplan



2. PCB Errata

DS33M30DK02A0 errata:

- Silkscreen for JP08 should designate the jumper function as Mac clock enable. Instead it designates the function as MDIX enable
- Silkscreen for JP09 should designate the jumper function as MDIX enable. Instead it designates the function as Mac clock enable.
- SRAM devices U06 and UB09 have been reworked to connect pin 1 and pin 2. On the PCB this appears as a solder bridge between pin 1 and pin 2. This has been done to allow either a 128K*8 or a 512k*8 SDRAM to be installed and used as a 128K*8 device.

3. File Locations

This demo kit relies upon several supporting files, which are provided on the CD and are available as a zip file from the Maxim website www.maxim-ic.com/DS33M30DK. All locations are given relative to the directory in the CD/zip file called "_def_ini_DS33M30".

Table 3-1. Definition and Configuration Files

FILE NAME	FILE USAGE
. \ _DS33M_GlobalSonet.def	Top level definition file to select in ChipView's register mode. This file will autoload the remaining definition files for the DS33M30 when parallel mode is used.
.\ds33M_BufferMan.def .\ds33M_EncapDecap.def .\ds33M_GlobalEth.def .\ds33M_group.def .\ds33M_LanSubscriber.def .\DS33M_serial_1234.def	DS33M30 dependent files. These are called by _DS33M_GlobalSonet.def file, which is listed above.
.\m30_rx_tx_simulation 19mhz.mfg .\m30_STS3c_bert_LoopTime.mfg .\m30_STS3c_SONET_Loopback.mfg ._m30_STS3c_Ethernet_Loopback.mfg ._m30_STS3c_GFPNull_NoScramble.mfg	Files for manually configuring the DS33M30.

4. Basic Operation

Note: In the following sections, software-related items are identified by bolding. Text in **bold** refers to items directly from the EV kit software. Text in **bold and underlined** refers to items from the Windows operating system.

4.1 Powering Up the Demo Kit

- Connect PCB power jack to the wall adapter.
- Connect RS-232 serial cable, or USB cable between the host PC and demo kit.
- Verify that the jumpers are configured as described in Table 5-1.

4.1.1 General

- Upon power-up the power LEDs (DS13, DS12, DS14 green) will be lit.
- PHY LINK LED should be lit if an Ethernet cable is connected. Note that there are three link LEDs, as the DS33M30 is a Gigabit mode device. The L1000 LED should be litl the L100 and L10 LEDs should not be lit.

Following are several basic system initializations.

4.2 Basic DS33M30 Initialization

This section covers two basic methods for configuring the DS33M30.

1. Device Driver-Based Configuration: (Note: The DS33M3001A0 board revision does not come loaded with device drivers.) If the pins J20.1+J20.2 are jumpered, the device driver autoconfigures the DS33M30 upon power-up. This enables traffic to pass from the Ethernet port to the serial port. Consult the device driver documentation for further details. To load the GUI interface for the device drivers, go to the ChipView register mode **Tools** menu and select **Tools→Plugins→DS33M30/M33 Device Driver Demo**.
2. Register-Based Configuration: EoS VC3 with two ports assigned to VCG1.
    a. Remove jumper J20.1+J20.2 to disable device drivers and reset the board.
    b. Launch ChipView.exe and select **Register View**.

c. When prompted for a definition file, pick the file named **_DS33M30_GlobalMicroport.def**. Several additional definition files will load.
d. Go to the **File** menu and select **File→Memory Config File→Load .MFG file**. When prompted, select the file named **_m30_STS3c_GFPNull_NoScramble.mfg**.

4.2.1 Additional Configuration for DS33M30

- Using either a patch or crossover cable, connect the Ethernet connector to an ordinary PC or network test equipment. This should cause the link LED to turn on.
- Place a loopback connector at the SONET network side; the optical LOS LEDs should go out.
- At this point any packets sent to the DS33M30 are echoed back. Incoming packets (i.e., ping) should cause the Activity LED to blink.
- Note that ChipView.exe display settings can be changed using the **Options→Settings** menu.

4.3 Monitor and Capture Ethernet Traffic

- Although ping is mentioned, it is **not** the recommended frame source for testing. The ping command goes through the computer's TCPIP stack and sometimes is not sent out the PC's network connector (i.e., if the PC's ARP cache is out of date). Additionally, ping requires two PCs, as a Windows PC with only one adapter cannot ping itself (i.e., a local ping gets sent to 'local host' instead of out the connector). With that said, ping is still a valuable test once the prototyping stage is complete.
- Generation and capture of arbitrary (raw) packets can be accomplished using **CommView**. A full-featured demo is available at www.tamos.com/products/commview.
- Wireshark (formerly Ethereal) is a free packet capture utility. Download is available at www.wireshark.org.
- Adding additional Ethernet ports to a PC is rather simple when a USB-to-Ethernet adapter is used. This allows for end-to-end testing using a single PC. When using two adapters, the PC has a different IP address for each adapter. Test equipment allows selection of either adapter. Operating system-based network traffic is sent out the default adapter, which usually is the adapter that has recently had connection to a live network.

5. Jumpers and Connectors

Jumpers and connectors are listed in Table 5-1. They are listed in order of appearance on the PCB from left to right, top to bottom (as viewed with SONET connector on the left side of the board).

Table 5-1. Jumpers and Connectors

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING	SCHEMATIC PAGE	DESCRIPTION
J03	Ethernet Connection	Connected	14	Connect to Gigabit Ethernet source.
JP06 + JP03	Bias PHY Speed1 + Speed0	Jumper P2+3(high) P2+1 (low)	14	If auto negotiation is enabled this setting advertises capability for 1000 speeds. If auto negotiation is disabled then this setting forces 1000Mb mode.
JP04	Bias PHY ANEN	Jumper P2+3 (high)	14	Jumper P2+3 to enable auto negotiation.
JP05	Bias PHY Duplex	Jumper P2+3 (high)	14	Jumper P2+3 to enable full duplex, Jumper P1.2 to force half duplex.
JP09	Bias PHY MdixEn	Jumper P2+1 (high)	14	P2+3 disables pair swap mode, P2+1 enables pair swap mode.
JP08	Bias PHY MacClkEn	Jumper P2+3 (low)	14	P2+3 PHY clock to mac output is disabled, P1+2 PHY clock to mac output is enabled. Mac clock only needs to be enabled in Gigabit mode.

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING	SCHEMATIC PAGE	DESCRIPTION
DS05	LED activity	--	14	Flashes for PHY Tx-Rx activity.
DS06 DS07 DS09	LED link speed	DS06 shold be lit (when linked)	14	LED to indicate link speed: 1000, 100, or 10Mbps. Only DS06 should be lit since the DS33M30 is GMII only.
J04	PHY test points	--	12	PHY test points. The connector pinout is compatible with existing PHY cards, but cannot be used with U04 on the board.
JP13 JP14	Runtime options	NA	11	Currently the device drivers do not fit in flash, and are not loaded to the DK.
DS11	Status	—	11	LED kit status, not lit.
J03	USB	—	11	USB interface. See folder marked USBdrivers_CP210x for drivers.
J04	RS232 DB9 connector	—	11	RS-232 DB-9 connector, operates in ASCII mode at 57.6K,8,N,1.
JP18 JP19	Comm Port	Jumper P1+2 P1+2	11	Jumper pins 1+2 to select the RS232 transceiver. Jumper pins 2+3 to select the USB to serial converter.
SW01	Reset	—	7	System Reset button.
J06	SPI	All jumpered	6	SPI™ bias and data pins. Control by external processor is possible after removing CS, MISO, MOSI, and SCK
JP15	HIZ	Jumper P2+3	6	Dut three-state control.
J07	Software Debug	—	11	ONcE EBDI.
JP07	Clock select	Jumper P2+1	4	Clock selection for PHY and Ethernet side of DS33M30.
JP02	Clock select	Jumper P1+2	4	Clad clock selection, Jumper P1+2 to drive with 19.44MHz. Jumper P2+3 to drive with 77.76MHz clock.
DS08	DS33M30 Int	—	9	LED, lit when DS33M30 Interrupt is asserted.
J01	SFP test points	Jumper P9+10		Test points for SFP module.
DS01	SFP MOD0	—	2	Lit when a SFP module is installed.
DS03	SFP TXDISABLE	—	2	Lit when Tx is enabled.
DS02	SFP LOS	—	2	Lit when fiber optic cable is removed.
J02 JP01	SFP LOS/M33 LOS	Jumper	2	Jumper J02 to connect SFP LOS to DS33M30 LOS. If J02 is removed, then JP01 can be used to pull DS33M30 LOS high or low.
U01	SFP	Installed	2	SFP module.
J05	JTAG	—	6	DS33M30 JTAG.

SPI is a trademark of Motorola, Inc.

6. Line-Side Connections

The DS33M30DK has one optical port and one Ethernet port.

7. Microcontroller

The microcontroller has factory-installed firmware in on-chip nonvolatile memory. This firmware translates memory access requests from the RS-232 serial port into register accesses on the DS33M30 and the FPGAs.

8. Power-Supply Connectors

Connect a 5.0V wall adapter to the PCB power jack. LED DS1 provides indications that a 5.0V supply is connected properly. The board power supplies (3.3V, 2.5V, and 1.8V) are regulated to supply proper voltages to various circuits on the board.

9. Connecting to a Computer

Both USB and serial modes are supported.

To connect through a RS-232 serial port, set jumpers JP25 and JP26 jumpers to pins 1+2, identified in the silkscreen as RS232,PROCESSOR. Connect a standard DB-9 serial cable between the serial port on the DS33M30DK and an available serial port on the host computer. The host computer must be a Windows-based PC. Be sure the cable is a standard straight-through cable rather than a null-modem cable. Null-modem cables prevent proper operation.

To connect through USB, set jumpers JP25 and JP26 jumpers to pins 3+2, identified in the silkscreen as USB, PROCESSOR. Connect a USB cable between the DS33M30DK USB connector and the PC. The host computer must be a Windows-based PC, which should automatically recognize the device as a virtual com port and assign the device drivers. If drivers are not automatically assigned, direct the **New Hardware** wizard to the driver files on the CD in the folder marked **USBdrivers_CP210x**.

10. Installing and Running the Software

ChipView is a general-purpose program that supports a number of Maxim demo kits. To install the ChipView software, run Chipview.msi from the disk included in the DS33M30DK box or from the zip file downloadable on our website at www.maxim-ic.com/DS33M30DK.

After installation, run the ChipView program with the DS33M30DK board powered up and connected to the PC. If the default installation options were used, one easy way to run ChipView is to click the **Start** button on the Windows toolbar and select **Programs→ChipView→ChipView**. In the opening screen, click the **Register View** button. Select the correct serial port in the **Port Selection** dialog box, then click **OK**.

Next, the **Definition File Assignment** window appears. This window has subwindows to select definition files for up to four separate boards on other Maxim evaluation platforms. In the active subwindow, select the _DS33M_GlobalSonet.def definition file from the list shown, or browse to find it in another directory. Press the **Continue** button.

After selecting the definition file, the main part of the ChipView window displays the DS33M30's register map. To select a register, click on it in the register map. When a register is selected, the full name of the register and its bit map are displayed at the bottom of the ChipView window. Bits that are logic 0 are displayed in white, while bits that are logic 1 are displayed in green.

The ChipView software supports the following actions:

- **Toggle a bit.** Select the register in the register map and then click the bit in the bit map.
- **Write a register.** Select the register, click the **Write** button, and enter the value to be written.
- **Write all registers.** Click the **Write All** button and enter the value to be written.
- **Read a register.** Select the register in the register map and click the **Read** button.
- **Read all registers.** Click the **Read All** button.

11. Address Map

SPI mode address space begins at 0x0.

Table 11-1. Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000	DS33M30	DS33M30 registers

12. Additional Information/Resources

12.1 DS33M30 Information

For more information about the DS33M30, refer to the DS33M30 data sheet at www.maxim-ic.com/DS33M30.

12.2 DS33M30DK Information

For more information about the DS33M30DK, refer to the DS33M30DK Quick View page at www.maxim-ic.com/DS33M30DK.

12.3 Technical Support

For additional technical support, submit your questions at www.maxim-ic.com/support.

13. Component List

DESIGNATION	DESCRIPTION	SUPPLIER	PART
C01, C03, C05, C06, C09, C11, CB11, CB12, CB15, CB16, CB17, CB19, CB20, CB24, CB39, CB44, CB45, CB48, CB56, CB57, CB60, CB66, CB71, CB74, CB75, CB88, CB97, CB101, CB112	L_0603 CERAM .1uF 16V 20% X7R	AVX	0603YC104MAT
Component listing on next line, begins with C02	0603 CERAM 4.7uF 6.3V MULTILAYER	Digi-Key	ECJ-1VB0J475M
C02, C04, C07, CB05, CB07, CB18, CB21, CB22, CB25, CB31, CB32, CB33, CB35, CB38, CB42, CB43, CB46, CB47, CB49, CB50, CB51, CB53, CB55, CB61, CB62, CB63, CB64, CB67, CB68, CB70, CB72, CB73, CB76, CB77, CB78, CB79, CB80, CB81, CB83, CB84, CB86, CB89, CB90, CB94, CB95, CB103, CB105, CB109, CB110, CB116, CB121			
C08, C10, C12, CB04, CB08, CB09, CB10, CB14, CB30, CB40, CB65, CB85, CB107	L_0603 CERAM .01uF 50V 10% X7R	AVX	06035C103KAT
C1, C13, C14, C15, C16, C17, C18, CB120 , CB23, CB27, CB28, CB29, CB41, CB87, CB98, CB106	1206 CERAM 10uF 10V 20%	Panasonic	ECJ-3YB1A106M
CB01, CB02, CB03, CB13, CB111	D CASE TANT 470uF 6.3V 20%	KEM	T491D477M006AS
CB06, CB26, CB34, CB36, CB37, CB52, CB54, CB58, CB59, CB69, CB82, CB91, CB92, CB93, CB96, CB102, CB108, CB114, CB115	0603 CERAM .1uF 16V 10%	Panasonic	ECJ-1VB1C104K
CB104, CB117	L_1206 CERAM 1uF 16V 10%	Panasonic	ECJ-3YB1C105K
CB113	1206 CERAM 4.7uF 25V 10% X5R	Panasonic	ECJ-3YB1E475K
CB99, CB100, CB118, CB119	L_D CASE TANT 68uF 16V 20%	Panasonic	ECS-T1CD686R
DB01	SCHOTTKY DIODE, 1 AMP 40 VOLT	Internatioanl Rectifier	10BQ040
DS01, DS03, DS11 , DS04, DS12, DS14	L_LED, GREEN, SMD	Panasonic	LN1351C
DS02, DS08, DS10	L_LED, RED, SMD	Panasonic	LN1251C
DS05, DS06, DS07, DS09	LED, GREEN/GREEN, SMD	LUMEX	67-1362-1-ND
DS13	LED, RED/GREEN, SMD	LITEON	160-1172-1-ND
GND_TP01, GND_TP02, GND_TP03, GND_TP04, GND_TP05, GND_TP06, GND_TPB01, GND_TPB02, GND_TPB03	STANDARD GROUND CLIP	KEYSTONE	4954
H01, H02, H03, H04, H05, H08	KIT, 4-40 HARDWARE, .50 NYLON STANDOFF AND NYLON HEX-NUT	Labstock	4-40KIT4
J01	TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	Digi-Key	S2012-05-ND
J02, JB01	100 MIL 2 POS JUMPER	Labstock	NA
J03	CONNECTOR, SINGLE LEVEL, GIGABIT RJ-45, 10 PIN	Halo Electronics	HFJ11-1G02E

J04	PLUG, SMD, 50 PIN, 2 ROW VERTICAL	Samtec	SFM-125-L2-S-D-LC
J05	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	Samtec	TSW-105-07-T-D
J06	HEADER, 14 PIN, DUAL ROW, VERT	Samtec	HDR-TSW-107-14-T-D
J07	100 MIL 2*7 POS JUMPER	Labstock	NA
J08	L_CONN, DB9 RA, LONG CASE	AMP	747459-1
J09	TYPE B SINGLE RT ANGLE, BLACK	Digi-Key	WM17108-ND
JB02	CONN 2.1MM/5.5MM PWRJACK RT ANGLE PCB, closed frame, high current 24VDC@5A also requires 5V ACDC adapter INPUT 100-240VAC 50-60HZ 0.6A OUTPUT DC 5V 2.6A. PN DMS050260-P5P-SZ. MODEL 3Z-161WP05	CUI, INC	PJ-002AH
JP01, JP02, JP03, JP04, JP05, JP06, JP07, JP08, JP09, JP13, JP14, JP15, JP18, JP19	100 MIL 3 POS JUMPER	Labstock	NA
L01, L02	1uH ±10% 0805 Multilayer Ceramic 400 mA	TDK	GLF2012T1R0M
L1	FERRITE 3A 100 OHM AT 100 MHZ 1206 SMD	Steward	HI1206N101R-10
R01, R03, R04, RB19	RES 0603 0.0 Ohm 1/16W 5%	Panasonic	ERJ-3GEY0R00V
R02	RES 0603 1.0M Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ105V
RB01, RB18 , RB03, RB20, RB22	RES 0603 330 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ331V
RB02, RB04, RB12, RB13, RB14	RES 0603 30 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ300V
RB05	RES 0603 2.2K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ222V
RB06, RB07, RB16	RES 0603 2.0K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ202V
RB08	RES 0603 100 Ohm 1/16W 1%	Panasonic	ERJ-3EKF1000V
RB09, RB11	RES 0603 1.00K Ohm 1/16W 1%	Panasonic	ERJ-3EKF1001V
RB15	RES 0603 9.76K Ohm 1/16W 1%	Panasonic	ERJ-3EKF9761V
RB17, RB21	L_RES 0603 10K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ103V
RP01, RP02, RP03, RP04, RP05, RP06, RP07, RP08, RPB12	RESISTOR, 4 PACK, 30 OHM 5PCT QUAD 0603	Panasonic	EXB-V8V300JX
RPB01, RPB07, RPB20, RPB24	RESISTOR, 4 PACK, 330 OHM 5PCT QUAD 0603	Panasonic	EXB-V8V331JX

RPB02, RPB08, RPB11, RPB17, RPB19	RESISTOR, 4 PACK, 1K OHM 5PCT QUAD 0603	Panasonic	EXB-V8V102JX
RPB03, RPB04, RPB13, RPB15, RPB18, RPB21, RPB22, RPB23, RPB25, RPB26, RPB27, RPB28, RPB29	RESISTOR, 4 PACK, 10K OHM 5PCT QUAD 0603	Panasonic	EXB-V8V103JX
RPB05, RPB06, RPB14	RESISTOR, 4 PACK, 2.2K OHM 5PCT QUAD 0603	Panasonic	EXB-V8V222JX
RPB09, RPB10	RESISTOR, 4 PACK, 50 OHM 2PCT QUAD 0603	KOA	CN1J4TTD500G
SW01	SWITCH MOM 4PIN SINGLE POLE	Panasonic	EVQPAE04M
TP01	TEST POINT, 1 PLATED HOLE, DO NOT STUFF	Labstock	NA
U01	SFP host / receptacle	PARTS_KIT	SFP_HOST-TYCO
U02	GIG PHYTER V, 10/100/1000 ETHERNET PHYSICAL LAYER, 128 PIN QFP	National Semiconductor	DP83865DVH
U03	ETHERNET EXTENSION DEVICE	Dallas Semiconductor	DS33M30
U04	DOUBLE DATA RATE (DDR) SDRAM 2-2-2 TIMING 256MBITX16 TSSOP	MICRON	MT46V16M16TG-75E
U05	MMC2107 PROCESSOR	Motorola	MMC2107
U06, UB09	CYPRESS SRAM, LAB STOCK	Labstock	NA
U07	IC, SINGLE-CHIP USB TO UART BRIDGE, 28 PIN QFN	SIL	CP2101
U1	SPI SERIAL EEPROM 8M 8 PIN SOIC 3.3V	Atmel	AT26DF081A
UB01	IC, LINEAR REG 1.5W, 2.5V or Adj, 1A, 16TSSOP-EP	Maxim	MAX1793EUE-25
UB02	IC, LINEAR REG 1.5W, 1.8V or Adj, 1A, 16TSSOP-EP	Maxim	MAX1793EUE-18
UB03	MICROPROCESSOR VOLTAGE MONITOR, 3.08V RESET, 4PIN SOT143	Maxim	MAX811TEUS-T
UB04, UB05, UB07	IC, LINEAR REG 1.5W, 3.3V or Adj, 1A, 16TSSOP-EP	Maxim	MAX1793EUE-33
UB06	HIGH SPEED BUFFER	FAIRCHILD	NC7SZ86
UB08	Dual RS-232 transceivers with 3.3V/5V internal capacitors	MAXIM	MAX3233E
XB01	XTAL LOW PROFILE 8.0MHZ	ECL	EC1-8.000M
YB01	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 19.44 MHZ	SaRonix	SOCKET+NTH089A3-19.44

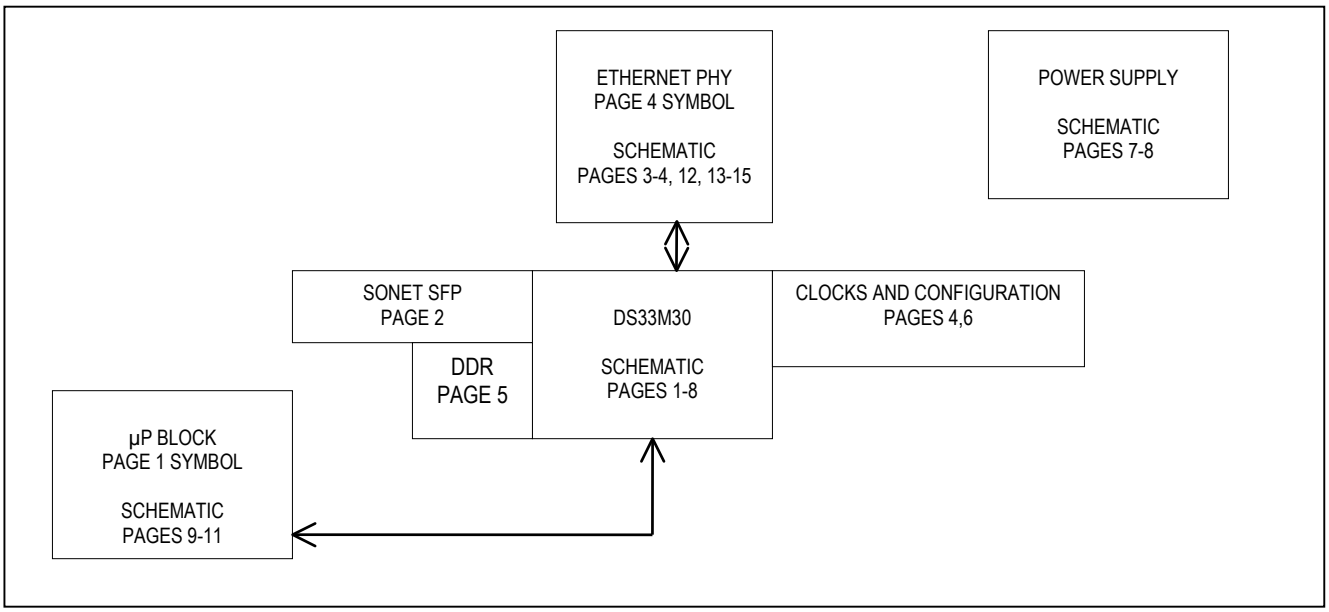
YB02	SOCKETED OSCILLATOR, CRYSTAL CLOCK, 3.3V - 25.000 MHZ	SaRonix	NTH089AA3-25.000+SOCKET
YB03	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 77.76 MHZ	SaRonix	SOCKET+NTH089A3-77.7600

14. Schematics

The DS33M30DK schematics are featured in the following pages. The schematic contains three hierarchal blocks: Microcontroller, Ethernet PHY, and Ethernet Test Points.

All signals inside a hierarchy block are local, with exception for V_{CC} and ground. In-port and out-port connectors are used to allow signals inside a hierarchy block to become accessible as pins on the hierarchy blocks symbol. From here blocks are wired together as if they were ordinary components. Figure 14-1 shows the system diagram in terms of hierarchal blocks with schematic page numbers given for each functional block.

Figure 14-1. DS33M30 PCB Layout and Schematic Hierarchy Block Page Listing



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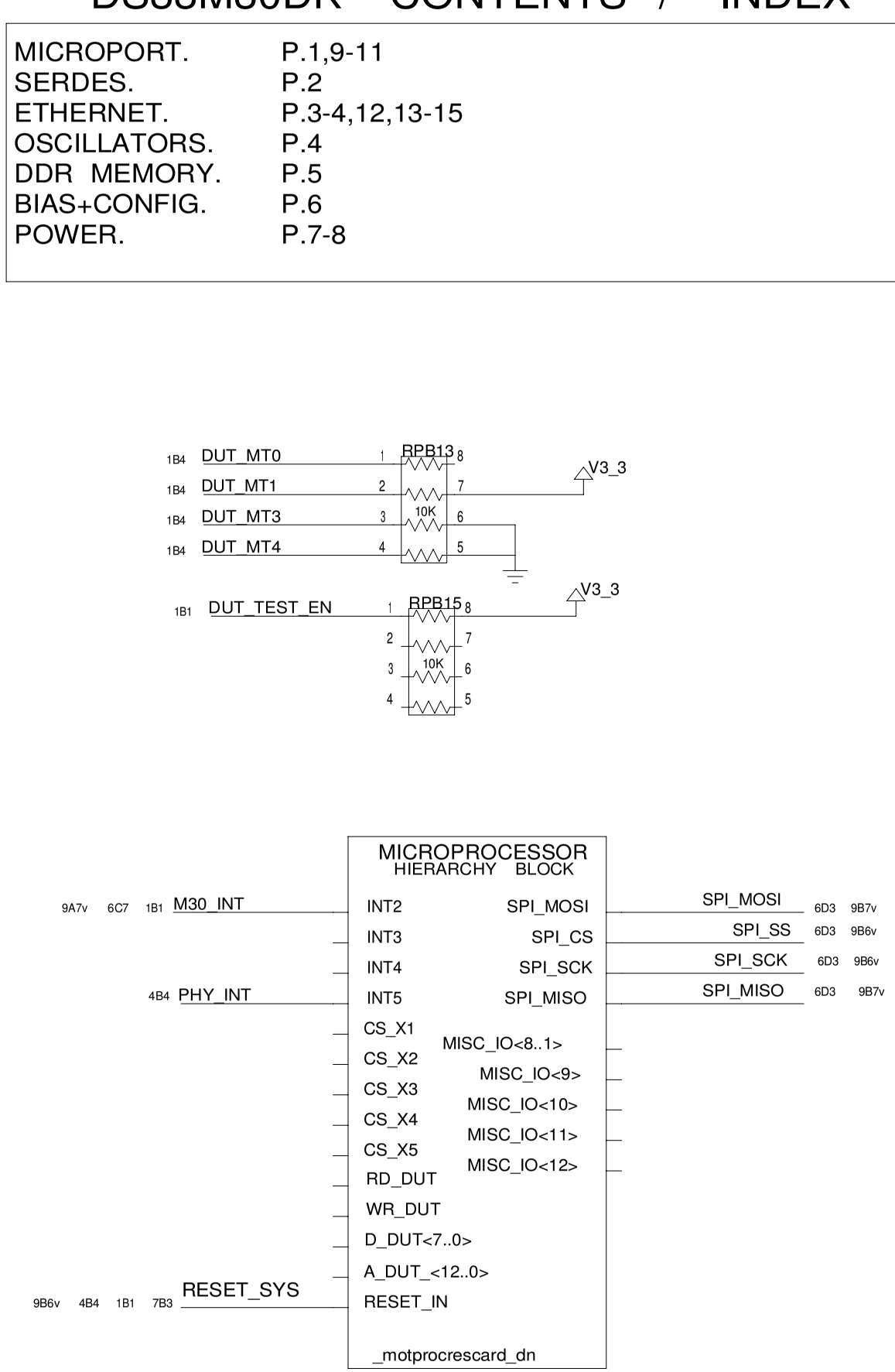
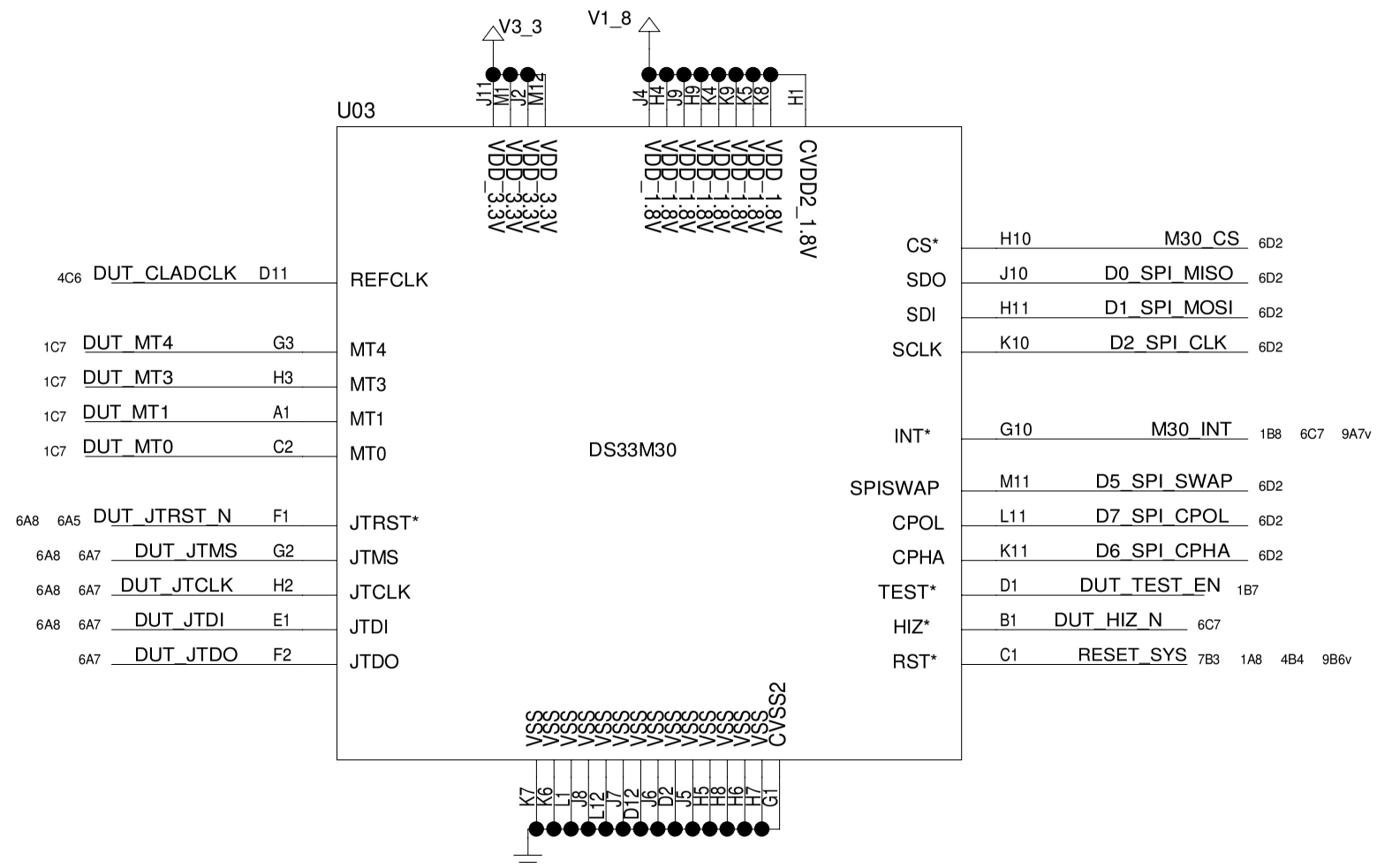
BIAS+CONFIG.	P.6
POWER.	P.7-8

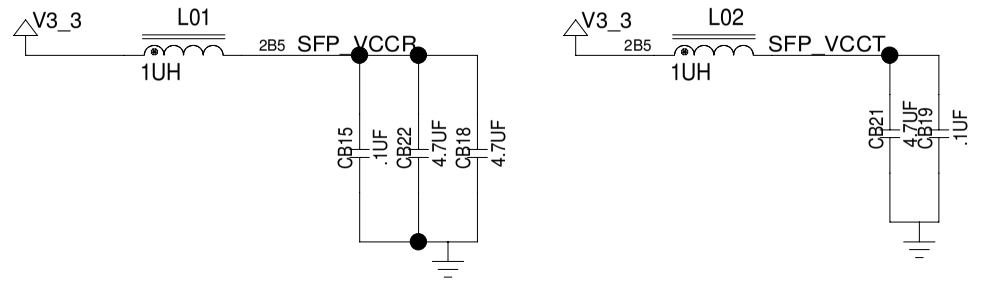


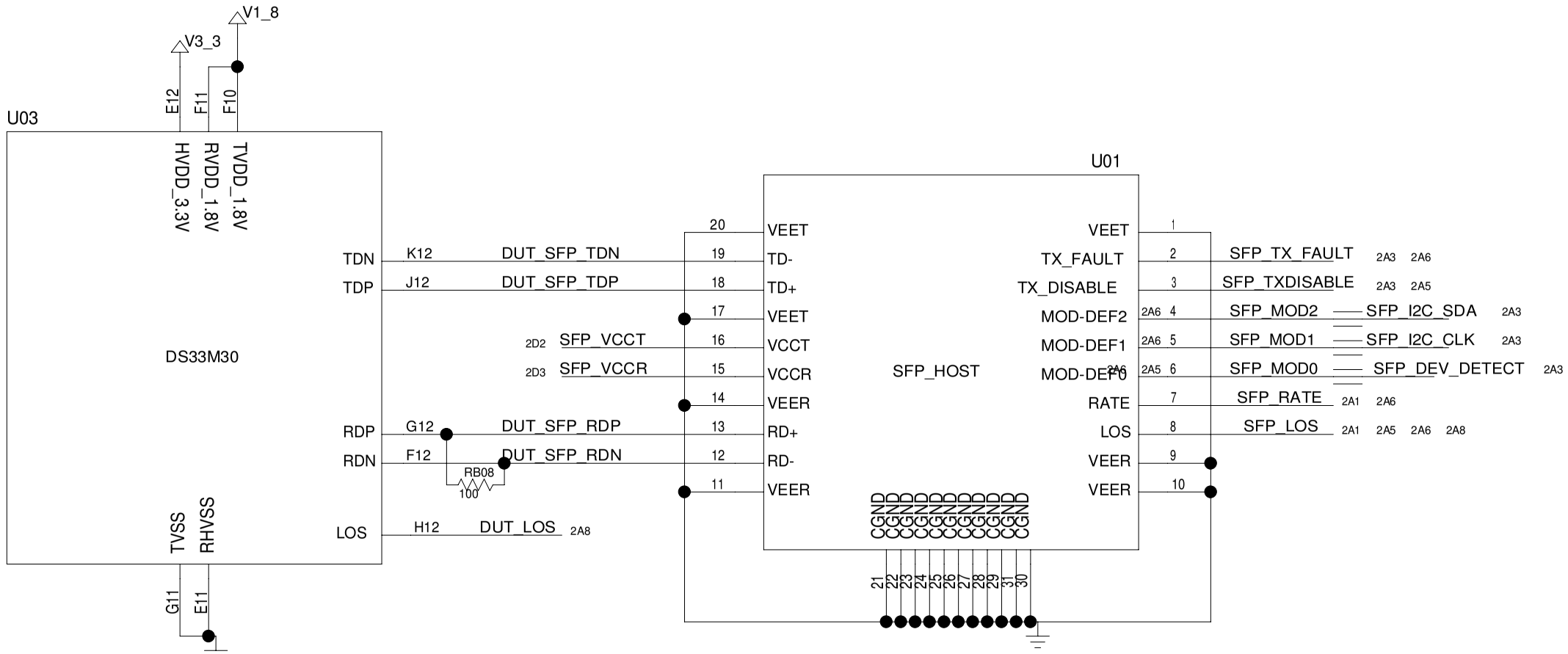


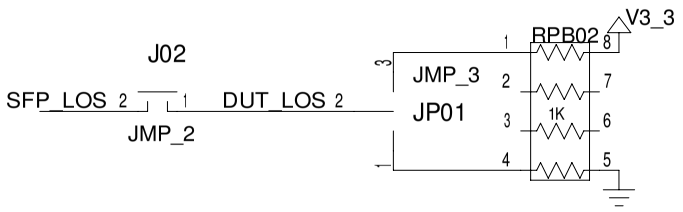
BEGINNING OF DS33M30DK

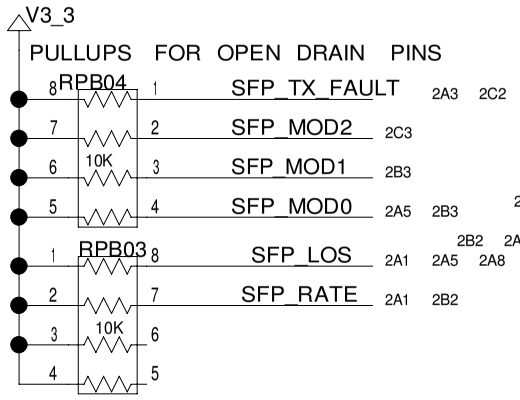
TITLE: DS33M30DK02A0 MICROPORT. P.1,9-11	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 1/8(BLOCK) 1/14(TOTAL)

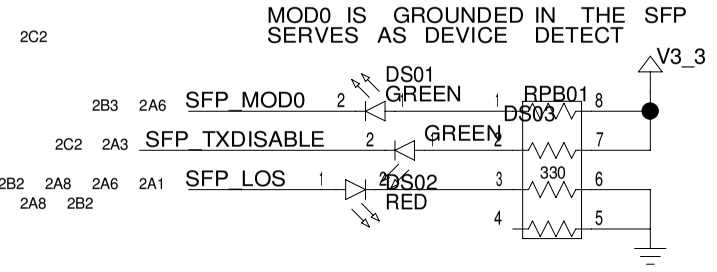
BLOCK NAME: _rc_top_dn_.

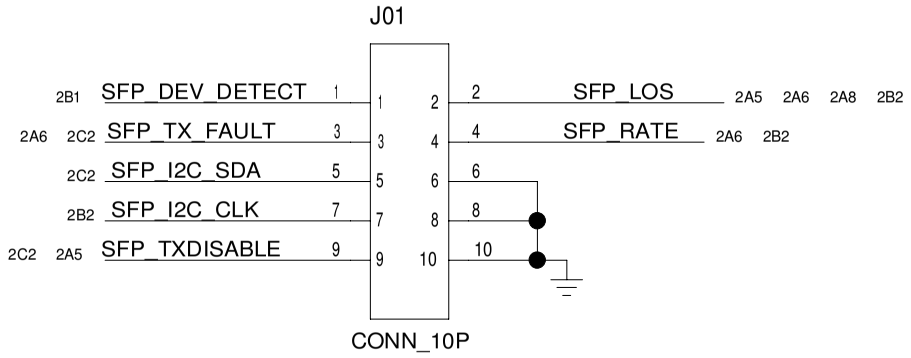






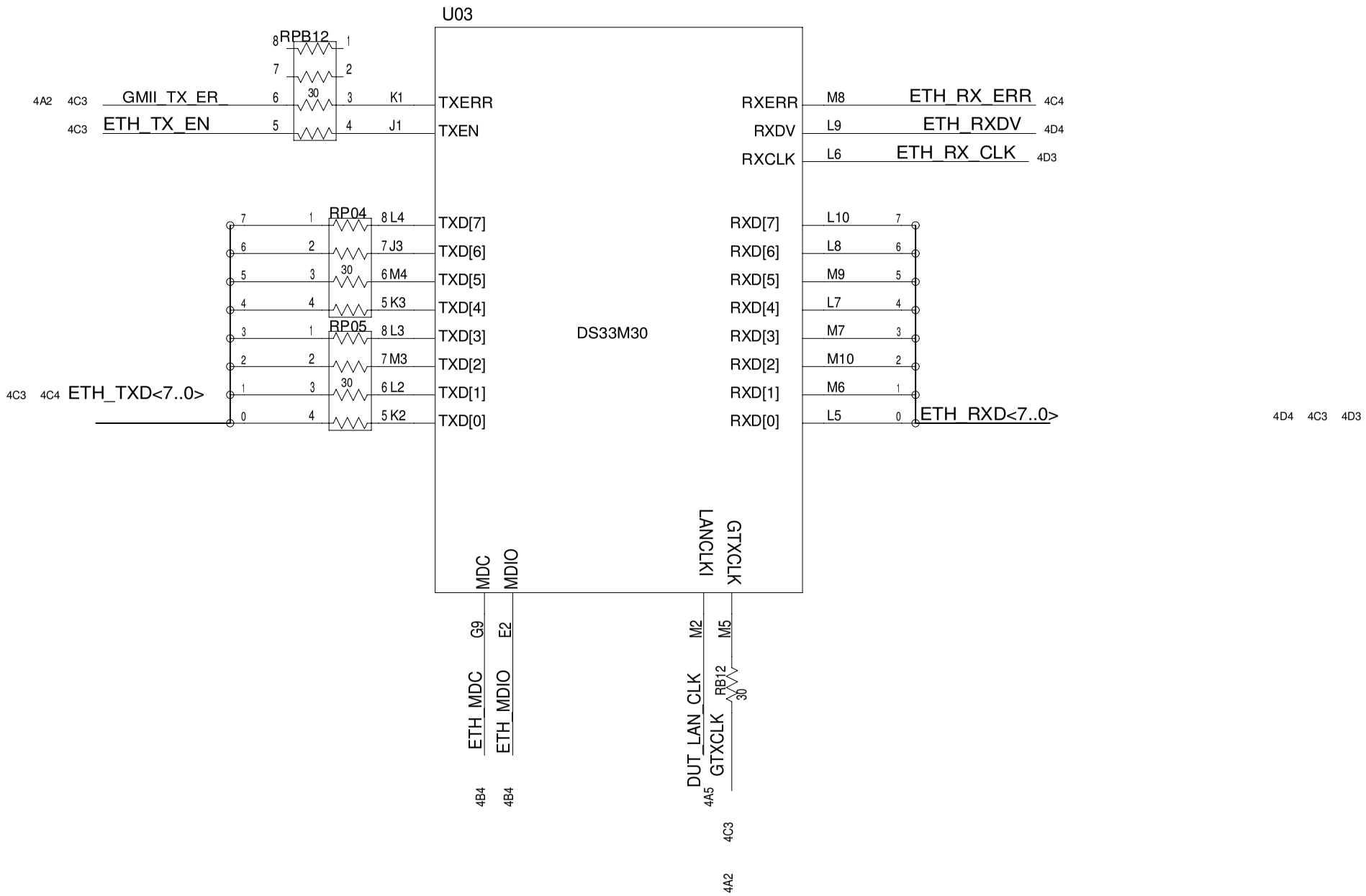






TITLE: DS33M30DK02A0 SERDES. P.2	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 2/8(BLOCK) 2/14(TOTAL)

BLOCK NAME: _rc_top_dn_.



TITLE: DS33M30DK02A0 ETHERNET. P.3-4,12,13-15	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 3/8(BLOCK) 3/14(TOTAL)

BLOCK NAME: _rc_top_dn_.

YB03
OSC
V3_3
VCC
GND
OUT
77.76MHZ_3.3V_SOCKET

YB01
OSC
V3_3
VCC
GND
OUT
19.44MHZ_3.3V_SOCKET

JMP_3
JP02
RB02
30
DUT_CLADCLK 1C4

YB02
25.000MHZ_3.3V_SOCKET
OSC
V3_3
VCC
GND
OUT
REFC_25M
JMP_3
RB04
30
PY25MHZOSC 4B4 12B5v 13B4v

JP07
RB14
30
DUT_LAN_CLK 3A4
RB13
30
AV_LAN_CLK 4B4 12B5v
ETH_REF_CLK IS ONLY USED IN RMII MODE (50 MHZ)
CLK_TO_MAC
13B1v 12B5v 4B1 4C3

V3_3
RB05
2.2k

_phy_dp83865bvh_dn

COL_DET 13A1v 12C5v ETH_COL_DET
RXD<7..0> ETH_RXD<7..0> 3B2 4C3 4D3 12B5v 12C5v 13A7v 13B7v
13B7v 4D4 3B2 ETH_RXD<3..0>
RXDV 13A1v 3C3 12C5v ETH_RXDV
RX_CLK ETH_RX_CLK
RX_CRS 12C5v 13A1v ETH_RX_CRS
RX_ERR 13A1v 3C3 12B5v ETH_RX_ERR
TXD<7..0> ETH_TXD<7..0> 3B6 4C3 12B5v 12C5v 13B7v
13B7v 12C5v 3B6 4C4 ETH_TXD<3..0>
TX_CLK ETH_TX_CLK
TX_EN ETH_TX_EN
GMII ONLY
TX_ER_ GMII_TX_ER 3C6 4A2 12B5v 13A7v
CLKTOMAC CLK_TO_MAC 4A7 4B1 12B5v 13B1v
CLKTOMAC_TESTPNT 13A7v 12B5v 4D4 3B2 ETH_RXD<7..4>
GMII_CLKFROM_MAC GTXCLK 3A4 4A2 12B5v 13B7v
13B7v 12B5v 3B6 4C4 ETH_TXD<7..4>
LAN_CLK AV_LAN_CLK
PHYOSC25M PY25MHZOSC
MDC ETH_MDC
MDIO ETH_MDIO
RESET_B RESET_SYS
PHY_INT PHY_INT
SPARE<4..1>

SINGLE 50 PIN
I.M. CARD PLUG-CONNECTORS
USED ON BOTTOM OF MOTHERBOARD
FOR CONNECTION TO ETHERNET CARD

_phy_imbus_mb_dn

PT1_COL_DET
PT1_RXD<3..0>
PT1_RXDV
PT1_RX_CLK
PT1_RX_CRS
PT1_RX_ERR
PT1_TXD<3..0>
PT1_TX_CLK
PT1_TX_EN
PT2_COL_DET
PT2_RXD<3..0>
PT2_RXDV
PT2_RX_CLK
PT2_RX_CRS
PT2_RX_ERR
PT2_TXD<3..0>
PT2_TX_CLK
PT2_TX_EN
LAN_CLK
OSC25M
MDC
MDIO
RESET_B
PHY_INT
SPARE
GMII_CLKFROM_MAC
GMII_TX_ER
GMII_CLKTOMAC_BUF

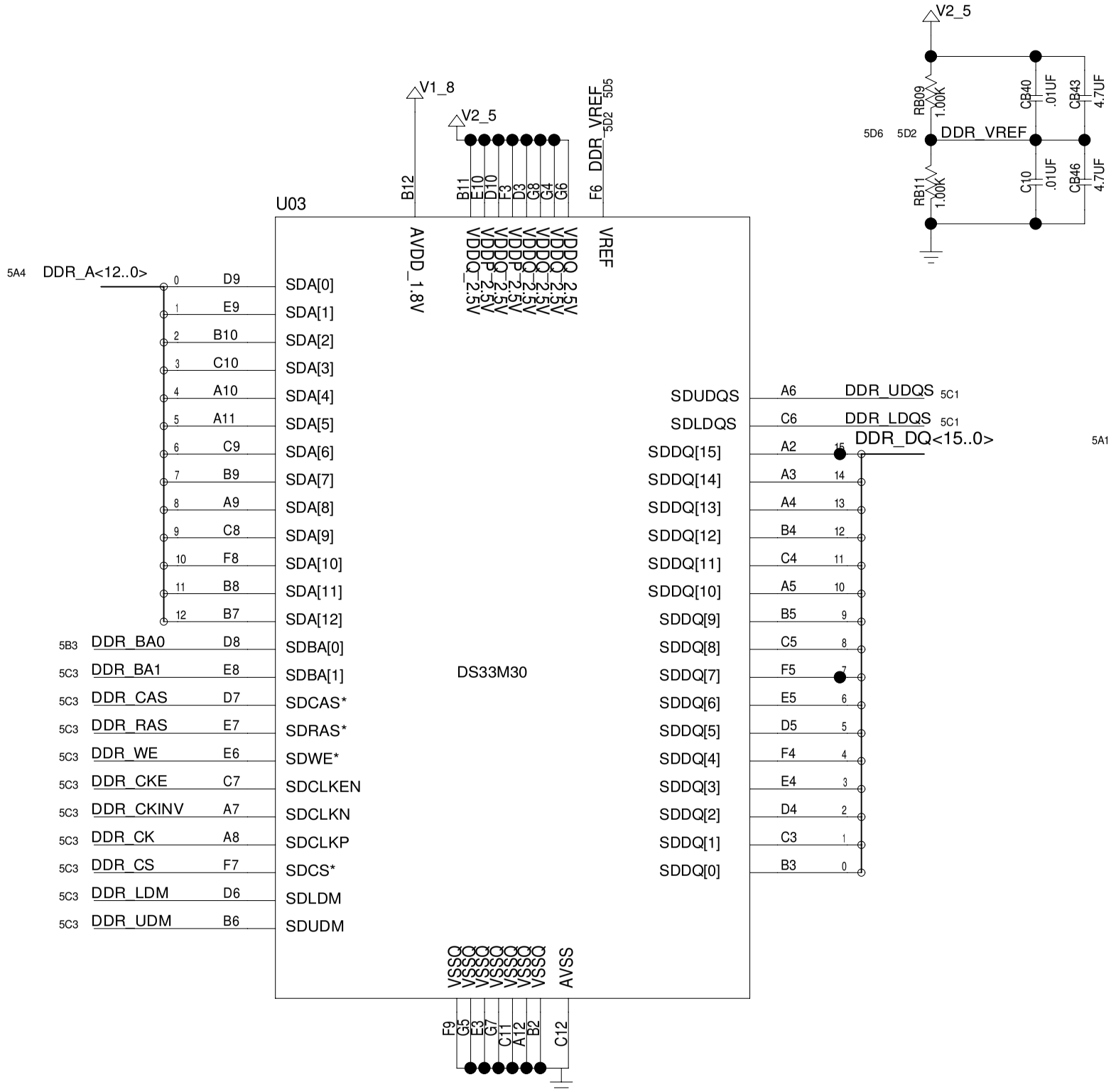
ETHERNET (LAN) CONNECTORS

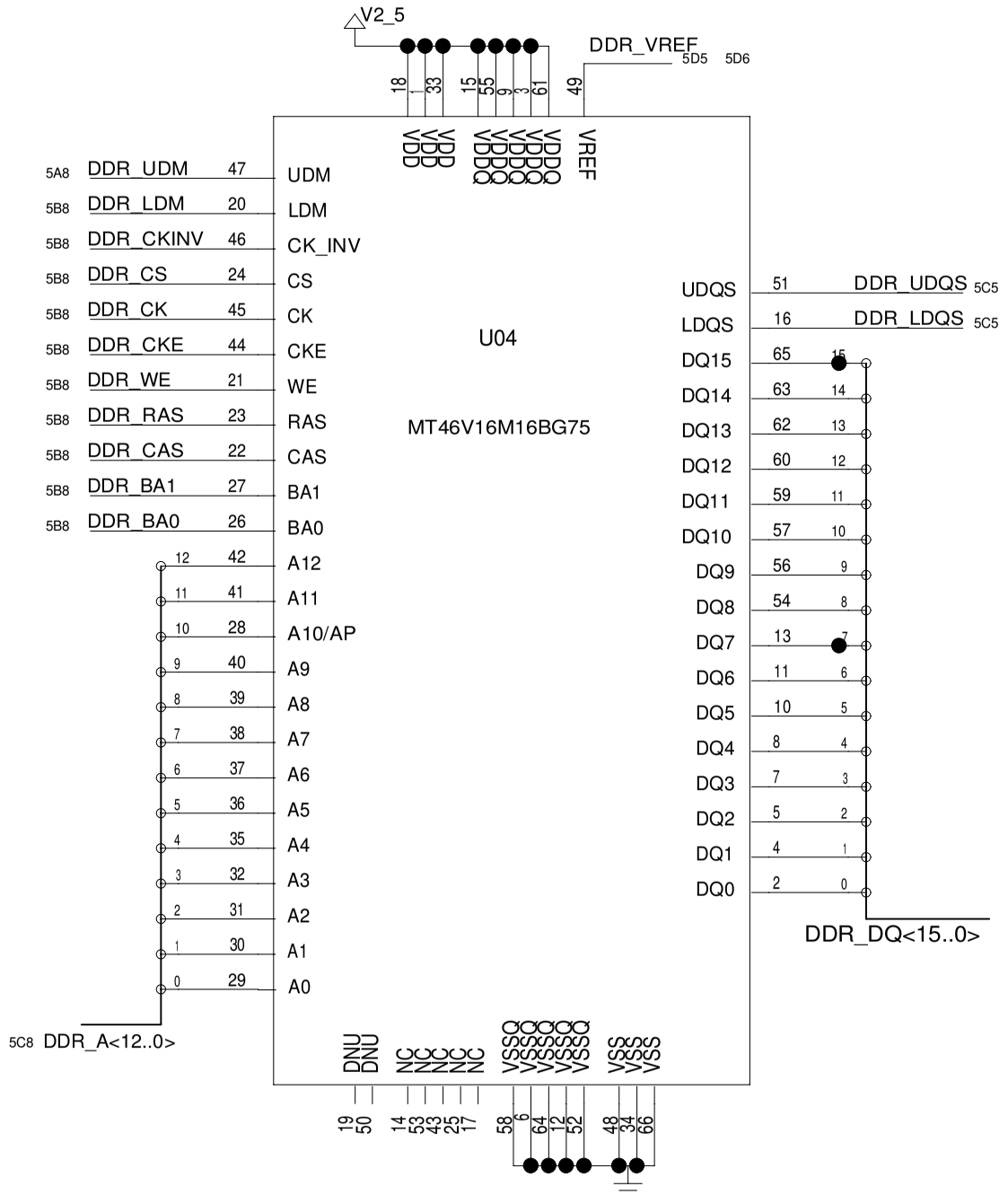
13B1v 12B5v 4C3 4A7 CLK_TO_MAC
13A7v 12B5v 4C3 3C6 GMII_TX_ER_
13B7v 12B5v 3A4 4C3 GTXCLK

ETHERNET CONNECTOR (I.M. BUS)
IS INTENDED FOR USE AS TESTPOINTS
NOT CONNECTION TO A RESOURCE CARD

TITLE: DS33M30DK02A0 ETHERNET. P.3-4,12,13-15	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 4/8(BLOCK) 4/14(TOTAL)

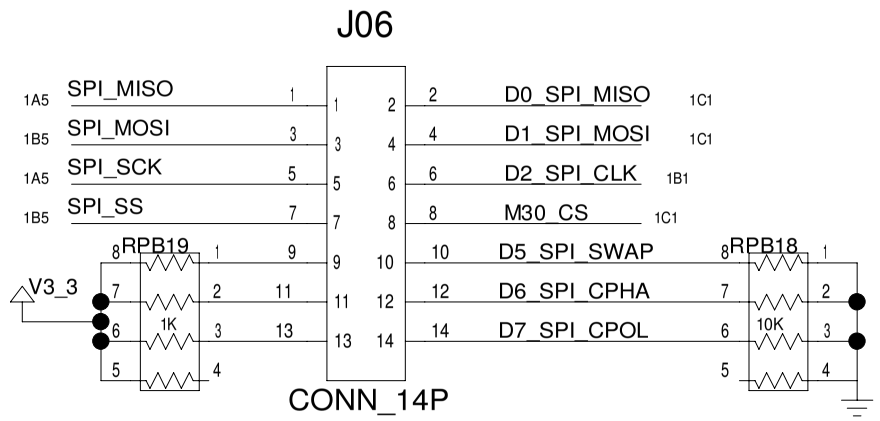
BLOCK NAME: _rc_top_dn_.

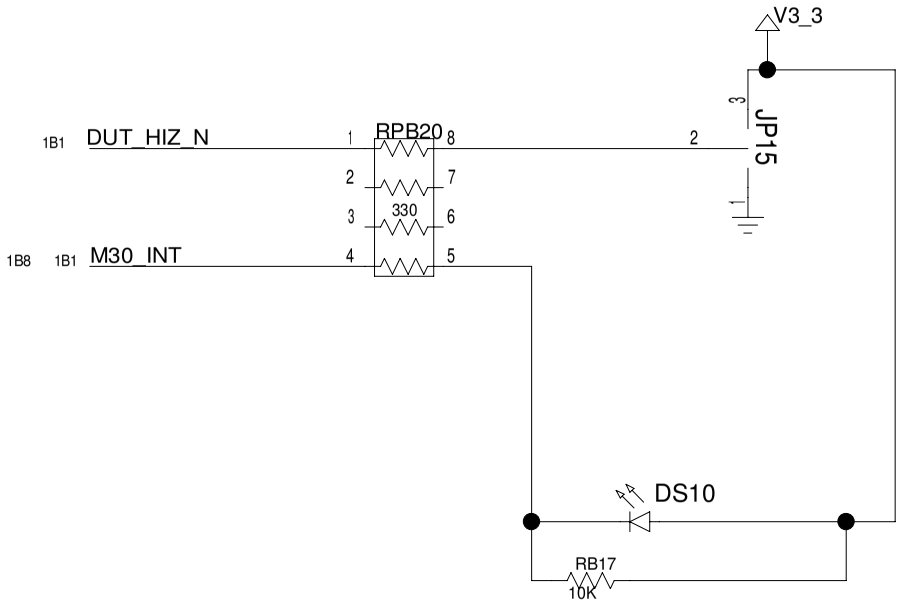


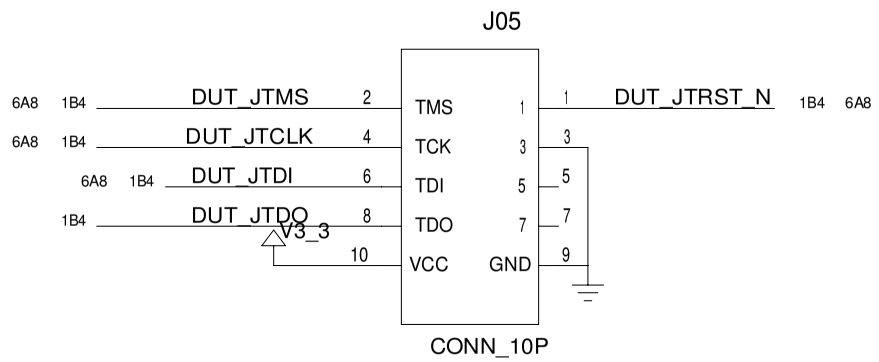


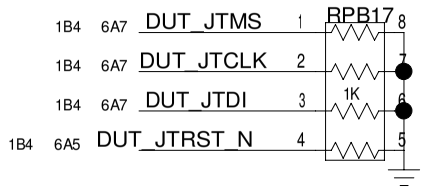
TITLE: DS33M30DK02A0 DDR MEMORY. P.5	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 5/8(BLOCK) 5/14(TOTAL)

BLOCK NAME: _rc_top_dn_.



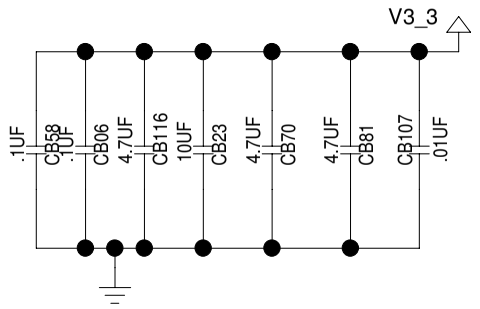


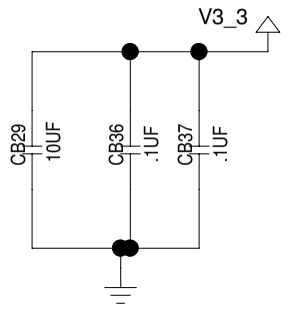


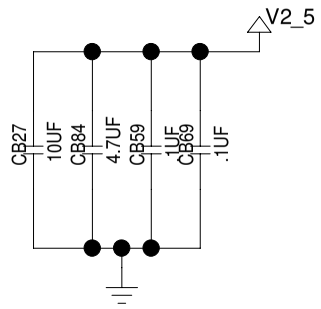


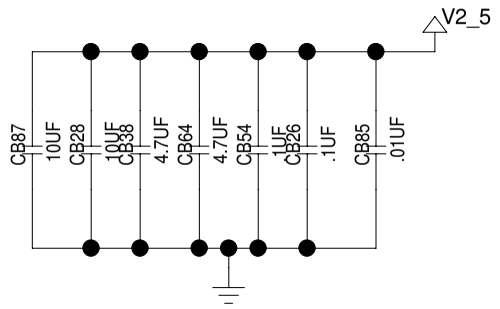
TITLE: DS33M30DK02A0 BIAS+CONFIG. P.6	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 6/8(BLOCK) 6/14(TOTAL)

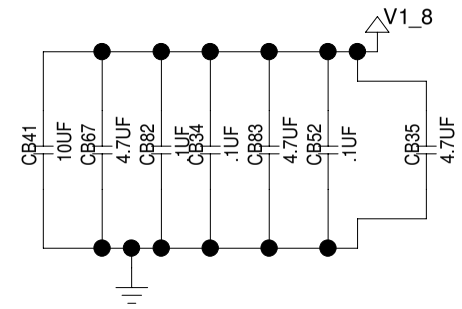
BLOCK NAME: _rc_top_dn_.

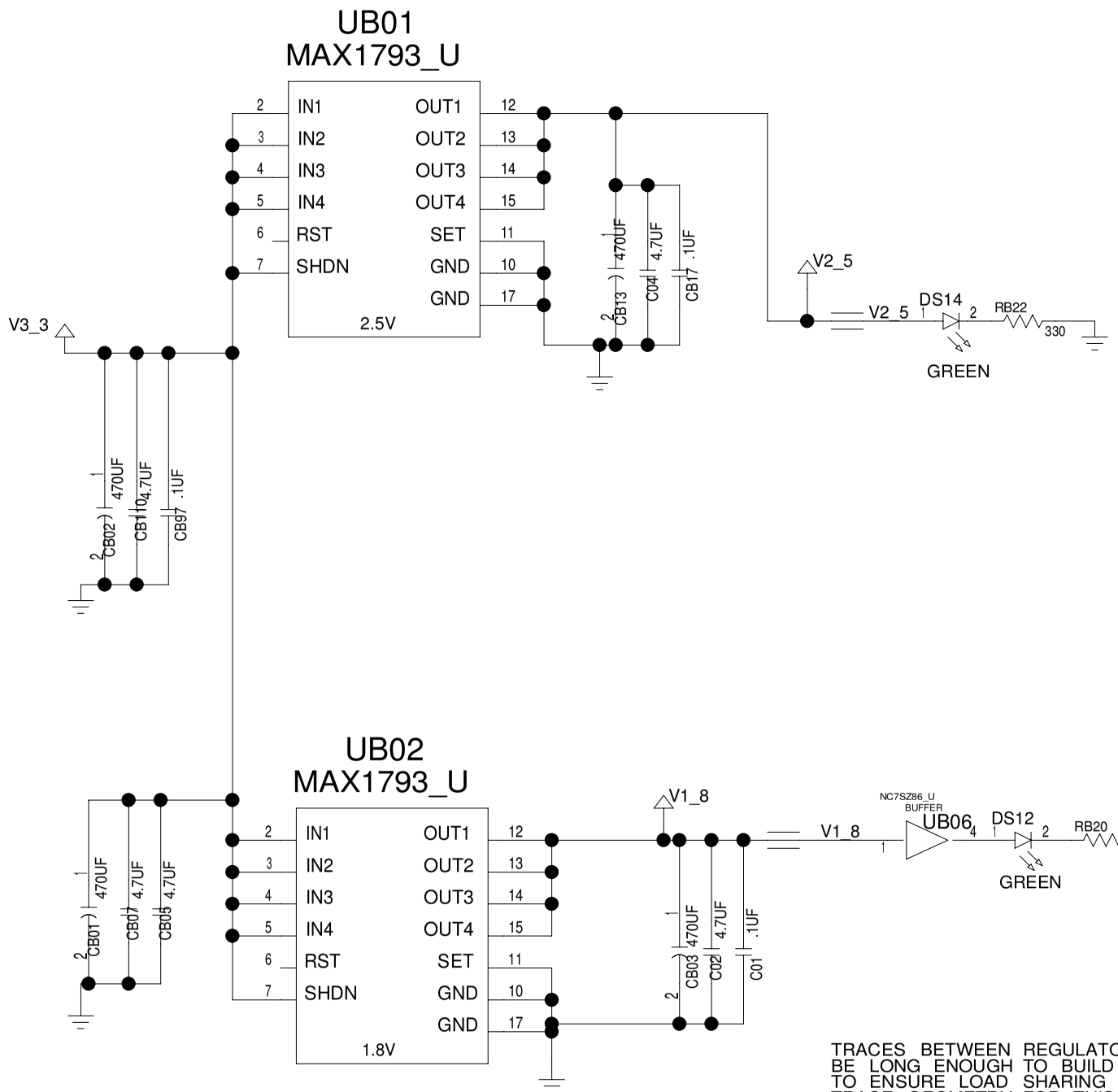


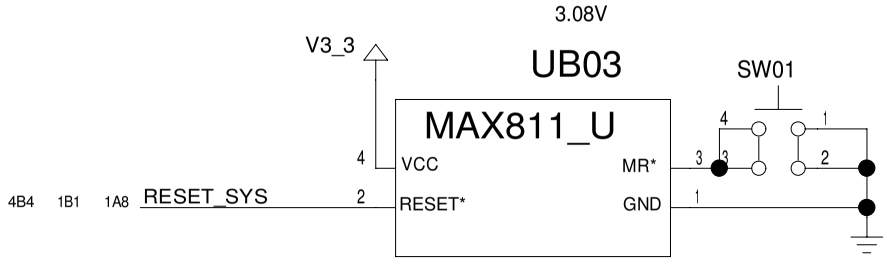












TRACES BETWEEN REGULATOR OUTPUT AND V2.5 SHOULD BE LONG ENOUGH TO BUILD 0.05 OHM OF RESISTANCE TO ENSURE LOAD SHARING BETWEEN THE 2.5V 1% REGULATORS TRACE GEOMETRY FOR THIS IS: 1 INCH LONG, 10 MIL WIDE, 1 OZ COPPER

TITLE: DS33M30DK02A0 POWER. P.7-8	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 7/8(BLOCK) 7/14(TOTAL)

BLOCK NAME: _rc_top_dn_.

V3_3

CB98 10UF CB109 4.7UF CB108 .1UF CB114 .1UF CB121 4.7UF CB115 .1UF CB91 .1UF

CB106 10UF CB103 4.7UF CB92 .1UF CB93 .1UF CB105 4.7UF CB102 .1UF CB96 .1UF

3.3V

UB05

MAX1793_U

V5_0

IN1 IN2 IN3 IN4 RST SHDN — OUT1 OUT2 OUT3 OUT4 SET GND GND

68UF CB100 C16 10UF R03 0.0

R01 0.0

3.3V

UB04

MAX1793_U

V5_0

IN1 IN2 IN3 IN4 RST SHDN — OUT1 OUT2 OUT3 OUT4 SET GND GND

8A4 POWEROK

C14 10UF

3.3V 1% REGULATOR

V3_3

R04 0.0

CB111 470UF CB94 4.7UF CB95 4.7UF

LED1 GREEN RED

RPB24 330

POWEROK 8A8

UB07

MAX1793_U

V5_0

OUT1 OUT2 OUT3 OUT4 SET GND GND — IN1 IN2 IN3 IN4 RST SHDN

10UF C18 68UF CB99

3.3V

100O100MZHPBF

JB02 L1

C1 10UF

V5_0

68UF CB119 68UF CB118 C13 10UF CB120 10UF C15 10UF C17 10UF

DB01 1 AMP

GND_TP04 GND_TP01 GND_TP03 GND_TPB01 GND_TP05 GND_TP06 GND_TPB03 GND_TPB02 GND_TP02

H01 H05 H04 H08 H03 H02

.50STANDOFF_NUT

TITLE: DS33M30DK02A0 POWER. P.7-8	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 8/8(BLOCK) 8/14(TOTAL)

BLOCK NAME: _rc_top_dn_.

U05 TIM_16H_8L

INT6* 88 · EB3* 96 · EB2* 98 · EB1* 100 · EB0* 101 · PQB3 104 · PQB2 105 · PQB1 106 · PQB0 107 · PQA4 108 · PQA3 109 · PQA1 110 · PQA0 111 · TDI 133 · TDO 135

EB3 10B4 · EB2 10B7 · ONCE_TDI 11D5 · 2107_TDO 11D5

MMC2107 CONTROL

ICOC23 52 · ICOC22 53 · ICOC21 54 · ICOC20 55 · ICOC13 56 · ICOC12 57 · ICOC11 58 · ICOC10 61 · GND —TEST 63 · SCI2_OUT 66 · SCI2_IN 68 · PROCSER_OUT 69 · PROCSER_IN 70

CSE1 60 · CSE0 62 · TC2 67 · TC1 78 · CS3* 81 · CS2* 83 · CS1* 85 · CS0* 86 · RESET* 118 · CLKOUT 128 · RSTOUT* 120 · SCK 93 · DE* 143 · SS* 94

CS3 · CS2 · CS1 · CS0 10B3 10B7 · RESET_IN 10D1 11D5 1A7^ · CPUCLK_OUT · PROC_RESET_OUT · SPI_SCK OUT 10C4 1A6^ · ONCE_DE_B 11D4 · SPI_CS OUT 1B6^

INT7* 89 · INT5* 84 · INT4 82 · INT3* 79 · INT2* 75 · INT1* 72 · INT0* 71 · YC0 80 · MOSI 90 · MISO 91 · XTAL 124 · EXTAL 125 · TCLK 130 · TRST* 142 · TMS 138

CS_SPI_FLASH 10C4 · USER_LED2 · ENABLE_DRIVER_H 9A6 · ENABLE_CALLBACKS_H 9A6 · RUN_KIT_USR · KIT_STATUS 11C8 · INT2 9A7 · YC0 · SPI_MOSI OUT 10D4 · SPI_MISO IN · XTAL 11D6 · OSC_MCU 11D6 · ONCE_TCLK 11D5 · ONCE_TRST_B 11D4 · ONCE_TMS 11D3

DS08 1B6^ 10D2 9A6 1B7^

1B7^ 10D2 9A6 9A7 INT2 · 2 · 1 · RB03 330 · V3_3

9A7 ENABLE_DRIVER_H · 9A7 ENABLE_CALLBACKS_H · 10D2 9A7 INT2 1B7^ · RPB21 10K · V3_3 · JMP_3 JP13 · JMP_3 JP14

U05

RW 59 · OE* 95 · SHS* 97 · TA* 99 · TEA* 102 · VSTBY 92 · VRH 113 · VRL 112 · VPP 87 · VDDA 115 · VDDF 74 · VDDH 103 · VDDSYN 123 · VDD8 141 · VDD7 129 · VDD6 77 · VDD5 65 · VDD4 45 · VDD3 33 · VDD2 19 · VDD1 9

RW · OE 10B4 · RCON 10C7 · TA · TEA · VRH · FLASH_VPP 11D3 · VDDSYN · RB19 0.0 · CB101 .1UF · CB104 1UF · V3_3

MMC2107 PORT

D31 31 144 · D30 30 1 · D29 29 2 · D28 28 3 · D27 27 4 · D26 26 5 · D25 25 7 · D24 24 10 · D23 23 12 · D22 22 15 · D21 21 16 · D20 20 17 · D19 19 20 · D18 18 21 · D17 17 22 · D16 16 25 · D15 15 27 · D14 14 30 · D13 13 31 · D12 12 34 · D11 11 35

D10 36 10 · D9 37 9 · D8 38 8 · D7 39 7 · D6 40 6 · D5 41 5 · D4 42 4 · D3 43 3 · D2 46 2 · D1 48 1 · D0 51 0

VSSA 114 · VSSF 73 · VSSSYN 126 · VSS8 140 · VSS7 127 · VSS6 76 · VSS5 64 · VSS4 44 · VSS3 32 · VSS2 18 · VSS1 8

PD<31..0> 10A2 10A6 10C7 10D7

A22 116 22 · A21 117 21 · A20 119 20 · A19 121 19 · A18 122 18 · A17 131 17 · A16 132 16 · A15 134 15 · A14 136 14 · A13 137 13 · A12 139 12 · A11 6 11 · A10 11 10 · A9 13 9 · A8 14 8 · A7 23 7 · A6 24 6 · A5 26 5 · A4 28 4 · A3 29 3 · A2 47 2 · A1 49 1 · A0 50 0

PA<22..0>

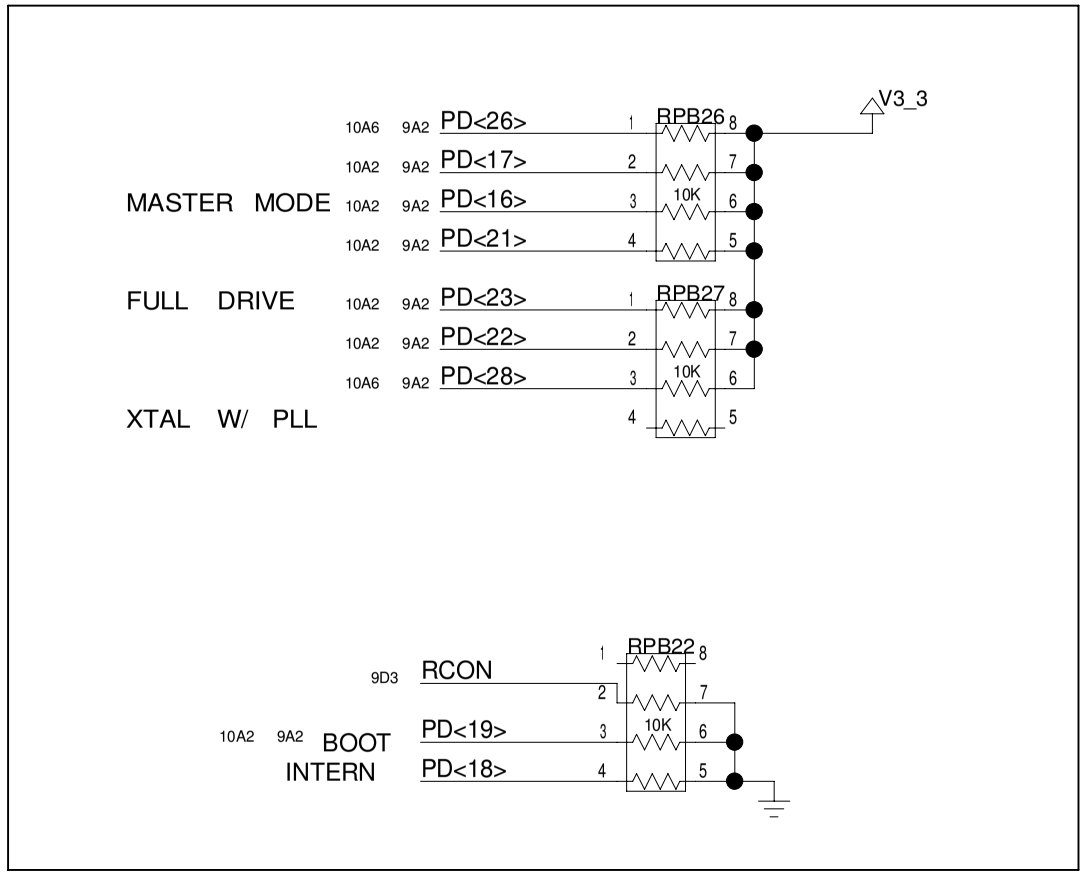
BEGINNING OF PROCESSOR HIERARCHY BLOCK

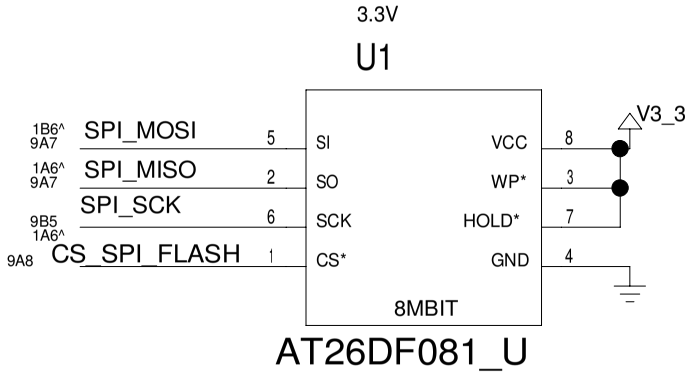
TITLE: DS33M30DK02A0	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 1/3(BLOCK) 9/14(TOTAL)

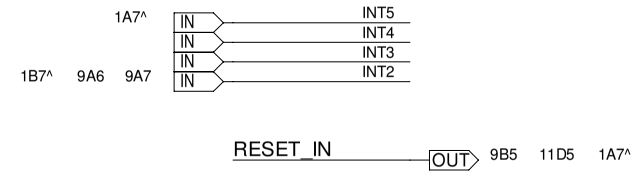
BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _rc_top_dn_\

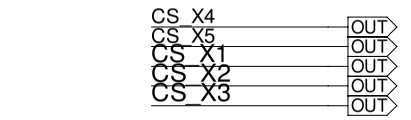
PRINTED Mon Mar 10 14:11:38 2008

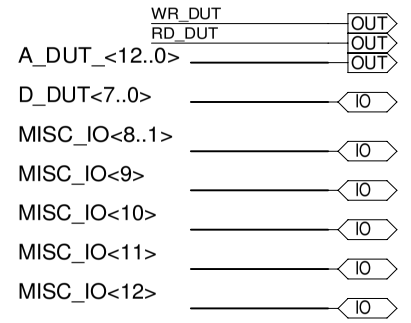
RESET CONFIGURATION

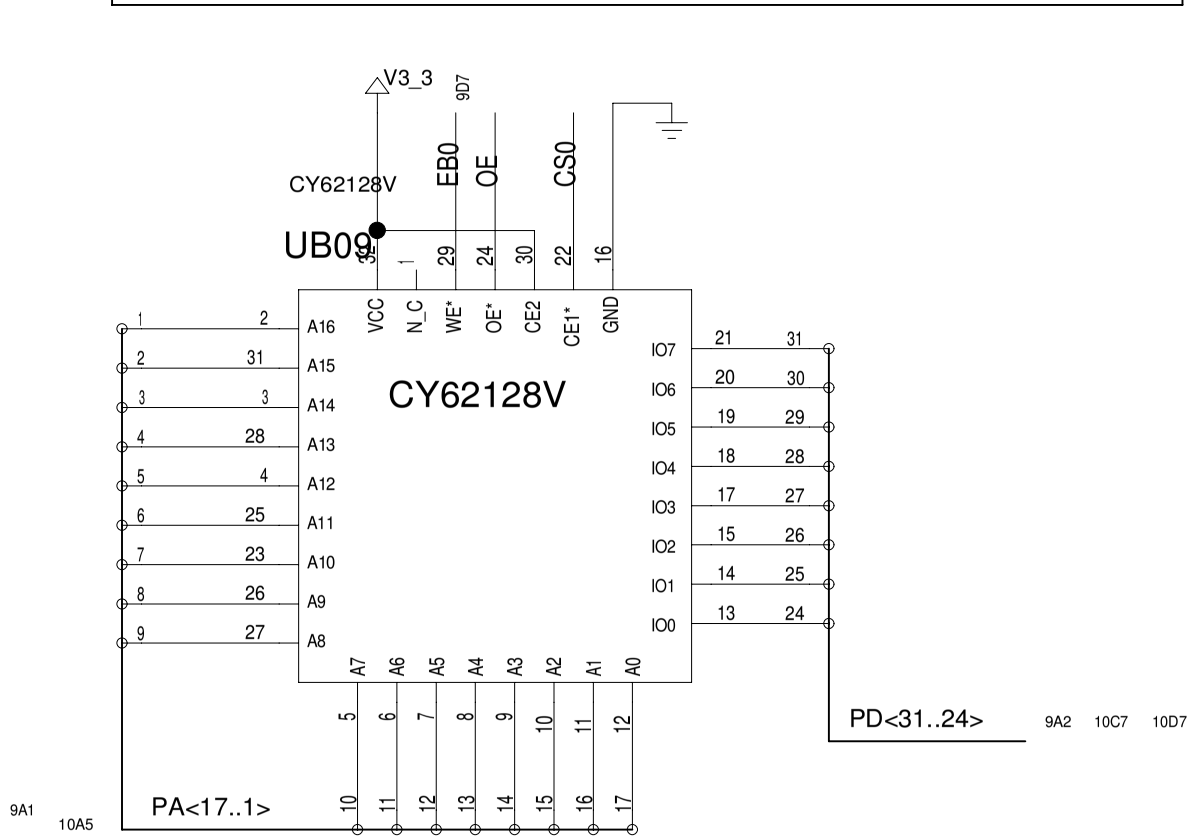


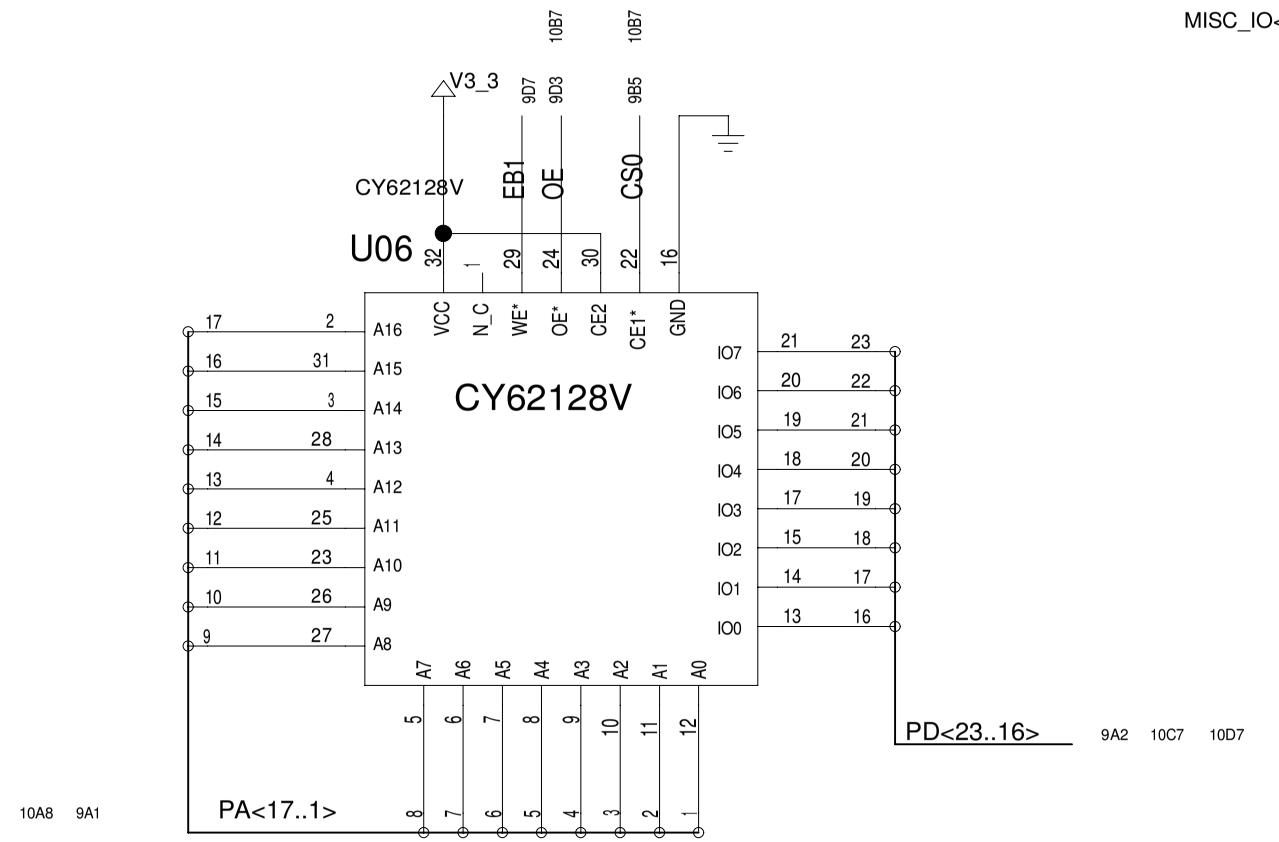












TITLE: DS33M30DK02A0	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 2/3(BLOCK) 10/14(TOTAL)

XB01
8.0MHZ
OSC_MCU 9A6
R02
1.0M
PLACE PADS FOR CAP
BUT DO NOT POPULATE
XTAL 9A7

DS11
GREEN
KIT_STATUS 9A7
RB18
330

J07
CON14P
9D6 ONCE_TDI
9D6 2107_TDO
9A6 ONCE_TCLK
RESET_IN
1A7^ 10D1 9B5 V3_3
ALIGN KEY
ONCE_TMS 9A6
ONCE_DE_B 9B5
ONCE_TRST_B 9A6
V5_0
FLASH_VPP 9D3
JB01
RPB29
10K
V3_3

V3_3
UB08
MAX3233E
11A5 UART_DIGIN
11A5 UART_DIGOUT
11A8 PRT1_OUT
11A8 PRT1_IN
R2OUT R2IN
INVALID* T2OUT
T2IN GND
T1IN V-
FORCEON C2-
R1OUT C2+
T1OUT C1-
R1IN C1+
VCC V+2
FORCEOFF* V+1

USB
J09
VDD
DAT-
DAT+
GND
RB21
CB113
CB112
.1UF

VDD IS A (UNUSED) OUTPUT ON CP2101 CHIP
U07
CP2101
USBDM
USBDP
VBUS
RST*
REGIN
SSPL 11 SUSPEND_LOW*
SUSPEND_HIGH
TXD 26 USB_DOUT 11A5
RXD 25 USB_DIN 11B5
RTS* 24
CTS* 23
DTR* 28
DSR* 27
DCD* 1
RI* 2
11B4 NC7 18
NC8 19
NC9 20
NC10 21
NC11 22
RPB23
RPB25
10K
SSPL
DTR AND RTS USE RPACK CONNECTION AS TESTPOINTS

9B8 PROCSER_OUT
JMP_3 JP18
USB_DIN 11B2
UART_DIGIN 11B8
9B8 PROCSER_IN
JMP_3 JP19
USB_DOUT 11B2
UART_DIGOUT 11B8

J08
CONN_DB9P
PRT1_OUT 11B8
PRT1_IN 11B8
RPB28
10K
V3_3

CB117 1UF
GND NC1 NC2 NC3 NC4 NC5 NC6

TITLE: DS33M30DK02A0	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 3/3(BLOCK) 11/14(TOTAL)

BLOCK NAME: motprocrescard_dn PARENT BLOCK: \ rc_top_dn \

V3_3 I67 V3_3

I68 GND

J04
SMT
SFM-125-L2-S-D-LC
NA
I78

4B3^	12A8	RESET_B	1	1	2	2 0	PT1_RXD<3..0>	12C1	4D3^		
			3	3	4	4 1	V1_8				
4C3^	12D1	PT1_TXD<3..0> 0	5	5	6	6					
		1	7	7	8	8 2					
			9	9	10	10 3					
		2	11	11	12	12	PT1_RX_CRS	12D1	4D3^		
		3	13	13	14	14	PT1_RXDV	12C1	4D3^		
4C3^	12D1	PT1_TX_EN	15	15	16	16	V3_3				
4C3^	12D1	PT1_TX_CLK	17	17	18	18	PT1_RX_CLK	12D1	4D3^		
			19	19	20	20	PT1_COL_DET	12D1	4D3^		
4B1^	12A4	GMII_CLKFROM_MAC	21	21	22	22	PT1_RX_ERR	12D1	4C3^		
4B1^	12A4	GMII_TX_ER_	23	23	24	24					
4B1^	12A4	GMII_CLKTOMAC_BUF	25	25	26	26	PHY_INT	12A8	4B3^		
4B3^	IO	OSC25M	27	27	28	28	SPARE	12A7			
4B3^	12A8	LAN_CLK	29	29	30	30 0	PT2_RXD<3..0>	12B1	4C3^		
			31	31	32	32 1					
4C3^	12C1	PT2_TXD<3..0> 0	33	33	34	34					
		1	35	35	36	36 2					
			37	37	38	38 3					
		2	39	39	40	40	PT2_RX_CRS	12C1			
		3	41	41	42	42	PT2_RXDV	12C1			
12C1		PT2_TX_EN	43	43	44	44	V2_5				
12C1		PT2_TX_CLK	45	45	46	46	PT2_RX_CLK	12C1			
4B3^	12A8	MDIO	47	47	48	48	PT2_COL_DET	12C1			
4B3^	12A8	MDC	49	49	50	50	PT2_RX_ERR	12C1			

PT1_TXD<3..0> IO
PT1_TX_EN IO
PT1_TX_CLK IO
PT1_RX_CLK IO
PT1_COL_DET IO
PT1_RX_ERR IO
PT1_RX_CRS IO
PT1_RXDV IO
PT1_RXD<3..0> IO

PT2_TXD<3..0> IO
PT2_TX_EN IO
PT2_TX_CLK IO
PT2_RX_CLK IO
PT2_COL_DET IO
PT2_RX_ERR IO
PT2_RX_CRS IO
PT2_RXDV IO
PT2_RXD<3..0> IO

CONNECTORS FOR LAN MOTHERBOARD TO RESOURCE CARD

LAN_CLK IO
MDC IO
MDIO IO
RESET_B IO
PHY_INT IO

12B4 SPARE IO

GMII_CLKFROM_MAC IO 12B6 4B1^
GMII_TX_ER_ IO 12B6 4B1^
GMII_CLKTOMAC_BUF IO 12B6 4B1^

TITLE: DS33M30DK02A0	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 1/1(BLOCK) 12/14(TOTAL)

BLOCK NAME: _phy_imbus_mb_dn. PARENT BLOCK: _rc_top_dn_\

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<TXT_GIGABITPHYMOTHERBRDCONNECTOR>. SCHEMATIC ON <PGNM_GIGABITPHYMOTHERBRDCONNECTOR>

PLACE 9.76K RES CLOSE TO BG_REF

RESET_B — RB15 9.76K

U02

DP83865_U

OUTPUT

COL	PIN39
CRS	PIN40
RXER	PIN41
RXDV	PIN44
RXD[0:7]	[PIN56:PIN45]
RXCLK	PIN57
TXCLK	PIN60
CLKTOMAC	PIN85
CLKOUT	PIN87

INPUT

TXERR	PIN61
TXEN	PIN62
TXD[0:7]	[PIN76:PIN65]
GTXCLK	PIN79
MDC	PIN81
CLKIN	PIN86

33	RESET*		
102	BG_REF		
34	VDD_SEL_STRAP	V3_3	
90	IO_VDD<1..12>	V1_8	
92	CORE_VDD<1..8>	V1_8	
96	2V5_AVDD<1..2>	V2_5	
123	1V8_AVDD1_<1..5>	V1_8	
98	1V8_AVDD2	V1_8	
100	1V8_AVDD3	V1_8	
128	VSS<1..35>		

32	TRST*	RB06 2.0K	
31	TDI	RP01	
28	TDO	RP01	
27	TMS	RP01	
24	TCK	RP01	
40	CRS/RGMII_SEL1	13A2	RX_CRS_BUF
39	COL	13B2	COL_DET_BUF
60	TX_CLK/RGMII_SEL0	13B2	TX_CLK_BUF
76	TXD<0>/TX0	TXD<7..0>	4C4^ 13C1
75	TXD<1>/TX1	TXD<7..0>	4C4^ 13C1
72	TXD<2>/TX2	TXD<7..0>	4C4^ 13C1
71	TXD<3>/TX3	TXD<7..0>	4C4^ 13C1
68	TXD<4>	TXD<7..0>	4C4^ 13C1
67	TXD<5>	TXD<7..0>	4C4^ 13C1
66	TXD<6>	TXD<7..0>	4C4^ 13C1
65	TXD<7>	TXD<7..0>	4C4^ 13C1
62	TX_EN/TXEN_ER	4C4^ 13C1	TX_EN
79	GTX_CLK/TCK	4C4^ 13D1	GMII_CLKFROM_MAC
61	TX_ER	4C4^ 13A7 13C1	TX_ER_
57	RX_CLK	13B2	RX_CLK_BUF
56	RXD<0>/RX0	RP06	
55	RXD<1>/RX1	RP06	
52	RXD<2>/RX2	RP06	
51	RXD<3>/RX3	RP06	
50	RXD<4>	RP03	
47	RXD<5>	RP03	
46	RXD<6>	RP03	
45	RXD<7>	RP03	
41	RX_ER/RXDV_ER	13A2	RX_ER_BUF
44	RX_DV/RCK	13A2	RXDV_BUF

81	MDC	MDC	13D2 4B4^
80	MDIO	MDIO	13D2 14B5 4B4^
3	INTERRUPT*	PHY_INT	0603_2PCT_50
108	MDIA_P	14C3 MDIA_P1	RPB10
109	MDIA_N	14C3 MDIA_N2	RPB10
114	MDIB_P	14C3 MDIB_P3	RPB10
115	MDIB_N	14C3 MDIB_N4	RPB10
120	MDIC_P	14C3 MDIC_P1	RPB09
121	MDIC_N	14B3 MDIC_N2	RPB09
126	MDID_P	14B3 MDID_P3	RPB09
127	MDID_N	14B3 MDID_N4	RPB09
86	CLK_IN	PHYOSC25M	0603_2PCT_50
87	CLK_OUT	CLKOUT_BUF	13B2
85	CLK_TO_MAC	CLKTOMAC_BUF	13B2
1	NON_IEEE_STRAP	NON_IEEE_STRAP	14D4
6	MAN_MDIX_STRAP/TX_TCLK	MAN_MDIX_STRAP__TX_TCLK	14D4
7	ACTIVITY_LED/SPEED0_STRAP	ACTIVITYLED_SPEED0	14B6
8	LINK10_LED/SPEED1_STRAP	LINK10LED_SPEED1	14B6
9	LINK100_LED/DUPLEX_STRAP	LINK100LED_DUPLEX	14B6
10	LINK1000_LED/AN_EN_STRAP	LINK1000LED_ANEN	14B6
13	DUPLEX_LED/PHYADDR<0>_STRAP	A0_DUPLEX	13A4
14	PHYADDR<1>_STRAP	RPB08	
17	PHYADDR<2>_STRAP	RPB08	
18	PHYADDR<3>_STRAP	RPB08	
95	PHYADDR<4>_STRAP	RPB08	
94	MULTI_EN_STRAP/TX_TRIGGER	MULTI_EN_STRAP__TX_TRIGGER	14C4
89	MDIX_EN_STRAP	MDIX_EN_STRAP	14C4
88	MAC_CLK_EN_STRAP/TX_SYN_CLK	MAC_CLK_EN_STRAP__TX_SYN_CLK	14C4

PLACE MDI RESISTORS CLOSE TO PHY

MAINTAIN 50OHM STIPLINE TO V2_5PHY

PHYOSC25M	IN 13B3 4B4^
LAN_CLK	4B4^ IO
MDC	4B4^ 13C3 IO
MDIO	4B4^ 14B5 13C3 IO
RESET_B	4B4^ 14B5 13D6 IO
PHY_INT	4B4^ 14B5 13C3 IO
SPARE<4..1>	IO
GMII_CLKFROM_MAC	IO 13B7 4C4^
TX_ER_	IO 13A7 13B7 4C4^
CLKTOMAC_TESTPNT	IO 13B1
CLKTOMAC	IO 13B1 4C4^
TXD<7..0>	IO 13B7 4C4^
TX_EN	IO 13B7 4C4^
TX_CLK	IO 13B1 4C4^
RX_CLK	IO 13B1 4D4^
COL_DET	IO 13B1 4D4^
RX_ERR	IO 13A1 4C4^
RX_CRS	IO 13A1 4D4^
RXDV	IO 13A1 4D4^
RXD<7..0>	IO 13A8 4D4^

RXD<7..0>	RP07		
RX_CLK_BUF	RP07	RX_CLK	13C1 4D4^
TX_CLK_BUF	RP07	TX_CLK	13C1 4C4^
CLKTOMAC_BUF	RP08	CLKTOMAC	13C1 4C4^
	RP08	CLKTOMAC_TESTPNT	
CLKOUT_BUF	RP08	CLKOUT	TP01
COL_DET_BUF	RP02	COL_DET	13C1 4D4^
RX_CRS_BUF	RP02	RX_CRS	13C1 4D4^
RX_ERR_BUF	RP02	RX_ERR	13C1 4C4^
RXDV_BUF	RP02	RXDV	13C1 4D4^

V3_3 — V3_3 — GND

4C4^ 13B7 13C1 TX_ER_ — RPB11 1K

13A3 A0_DUPLEX — RB01 330 — DS04 GREEN — RB07 2.0K — V3_3

TITLE:	DS33M30DK02A0
DATE:	03/10/2008
ENGINEER:	STEVE SCULLY
PAGE:	1/2(BLOCK) 13/14(TOTAL)

BLOCK NAME: _phy_dp83865bvh_dn. PARENT BLOCK: _rc_top_dn_\

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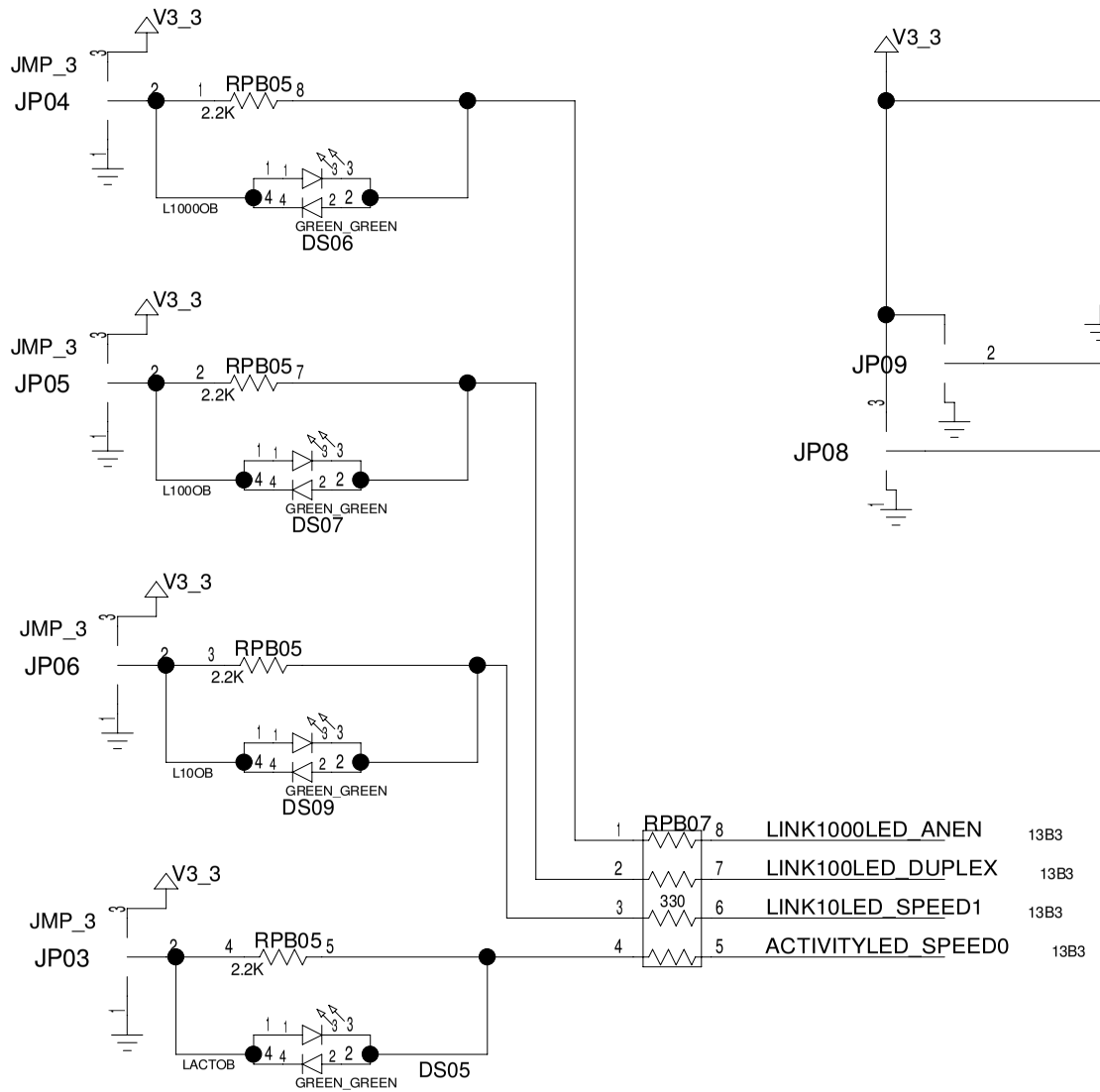
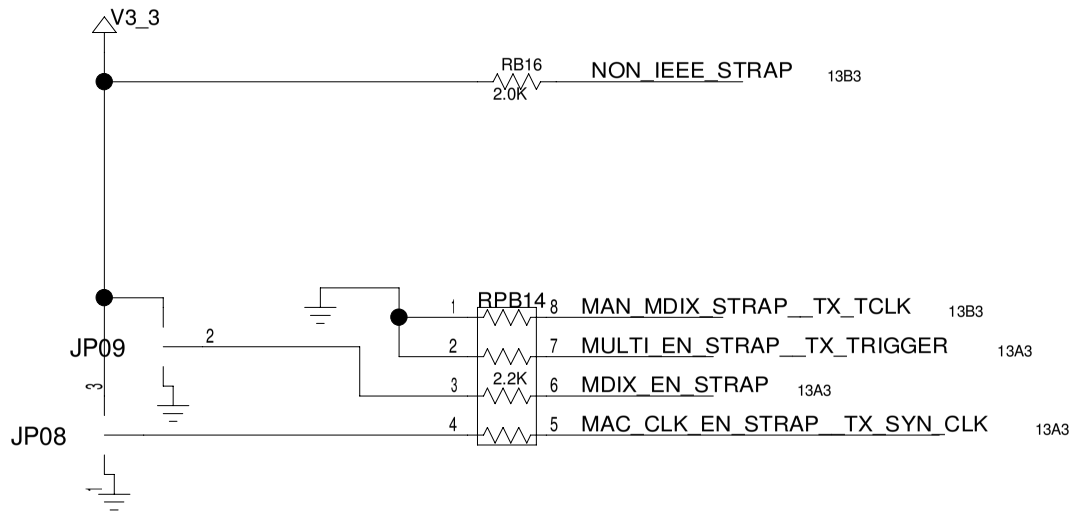
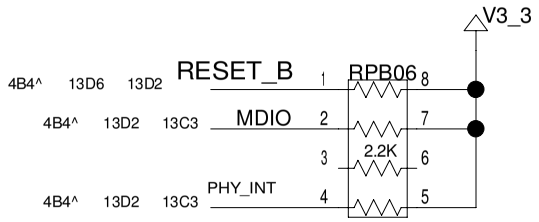
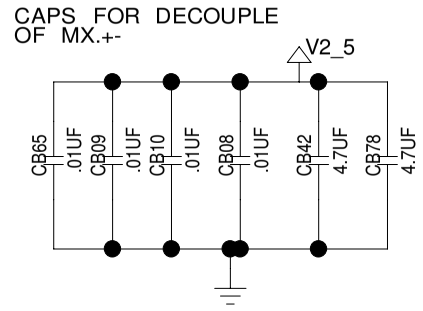
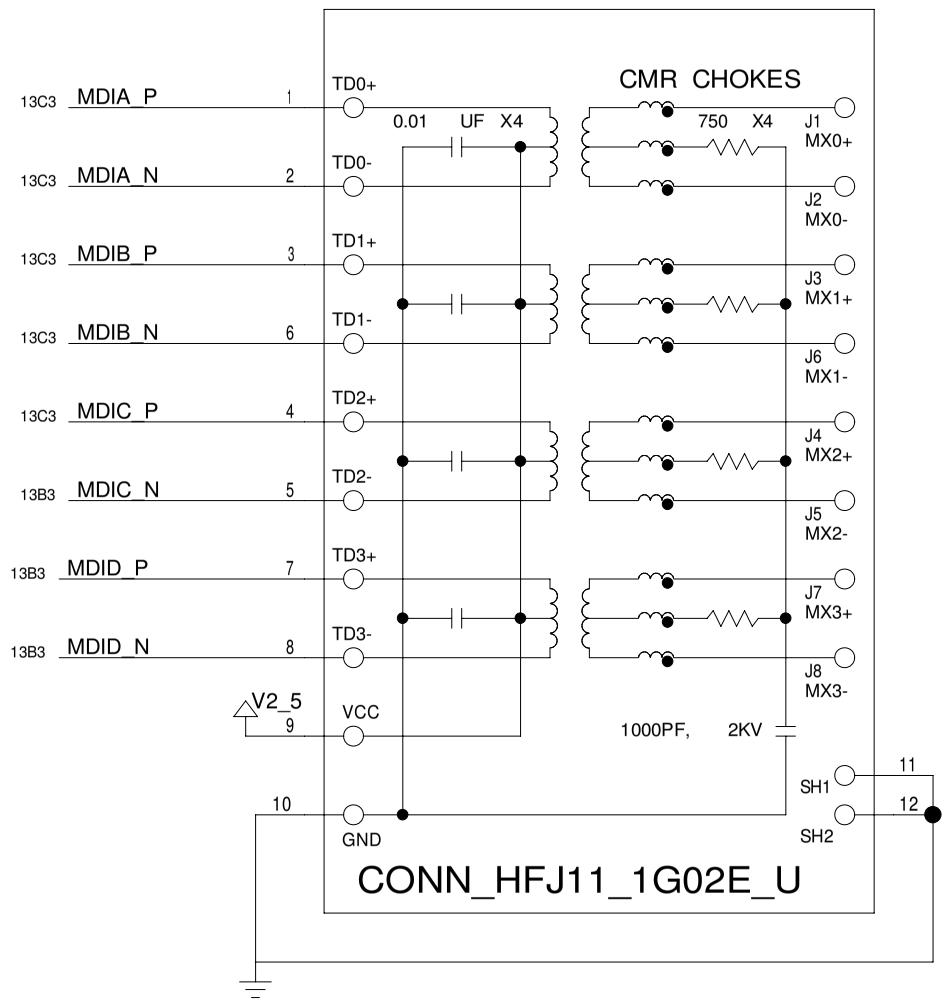


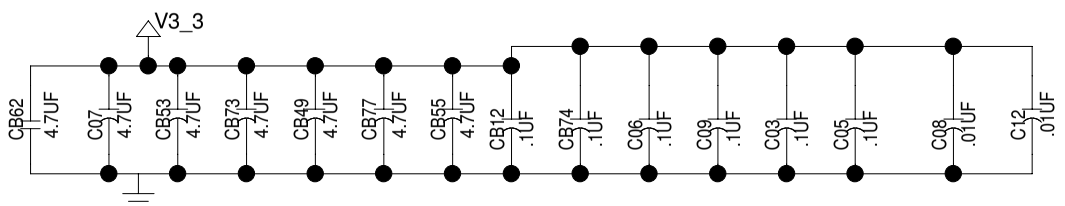


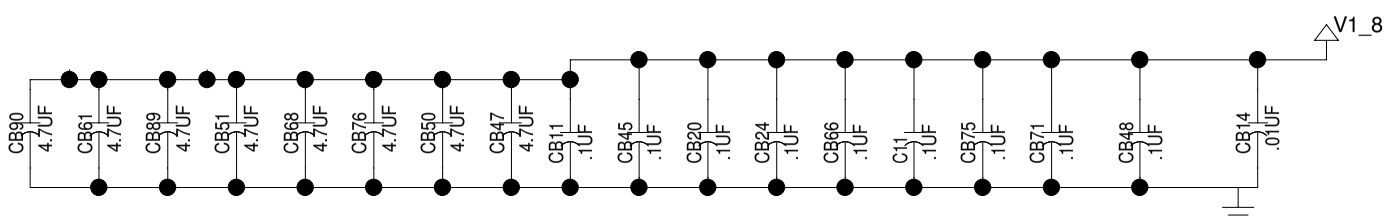


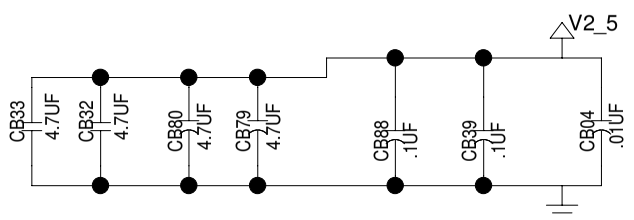




CHECK THAT 2.2K RES USE THE SAME RPACK
STRAP OPTIONS HERE DO NOT FOLLOW DATASHEET







TITLE: DS33M30DK02A0	DATE: 03/10/2008
ENGINEER: STEVE SCULLY	PAGE: 2/2(BLOCK) 14/14(TOTAL)

BLOCK NAME: _phy_dp83865bvh_dn. PARENT BLOCK: _rc_top_dn_\