MCF51JG256DS
Rev.1.1, 07/2013

MCF51JG256 Data Sheet

This is the MCF51JG256 Data Sheet set consisting of the following files:

- MCF51JG256 Data Sheet Addendum, Rev 1
- MCF51JG256 Data Sheet, Rev 1

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Data Sheet Addendum

MCF51JG256DSAD
Rev.1, 07/2013

MCF51JG256 Data Sheet Addendum

This errata document describes corrections to the *MCF51JG256 Microcontroller Data Sheet*, order number MCF51JG256DS. For convenience, the addenda items are grouped by revision. Please check our website at http://www.freescale.com for the latest updates.

The current version available of the *MCF51JG256 Microcontroller Data Sheet* is Revision 1.0.

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1 Addendum for Revision 1.0

Table 1. MCF51JG256DS Rev 1.0 addendum

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Table 5, “Power mode transition operating behaviors”/Page 12</td><td>Updated the numbers in “Power Mode Transition Operating Behaviors” table.
<table>
<tr><th>Symbol</th><th>Description</th><th>Min</th><th>Max</th><th>Unit</th><th>Note</th></tr>
<tr><td>t_{POR}</td><td>After a POR event, amount of time from the point V_{DD} reaches 1.85 V to execution of the first instruction across the operating temperature range of the chip.
• V_{DD} slew rate ≥ 6.2 kV/s
• V_{DD} slew rate < 6.2 kV/s</td><td>–</td><td>

300
1.85 V/(V_{DD} slew rate in Volts per µs)</td><td>µs</td><td>1</td></tr>
<tr><td></td><td>VLLS1 → RUN</td><td>–</td><td>165</td><td>µs</td><td>1,2</td></tr>
<tr><td></td><td>VLLS2 → RUN</td><td>–</td><td>123</td><td>µs</td><td>1,2</td></tr>
<tr><td></td><td>VLLS3 → RUN</td><td>–</td><td>123</td><td>µs</td><td>1,2</td></tr>
<tr><td></td><td>VLLPS → RUN</td><td>–</td><td>6.5</td><td>µs</td><td>2</td></tr>
<tr><td></td><td>STOP → RUN</td><td>–</td><td>6.5</td><td>µs</td><td>2</td></tr>
</table>
NOTES:
1 Normal boot (FTFL_FOPT[LPBOOT] is 1).
2 The wake-up time includes the execution time for small amount of firmware used to produce a GPIO clear. Wake-up time is measured from from falling edge of wake-up event to falling-edge of GPIO clear performed by software.</td></tr>
</table>

2 Revision history

Table 2 provides a revision history for this addendum.

Table 2. Revision history table

Revision	Substantive changes	Date of release
1.0	• Initial release. Updated the numbers in “Power Mode Transition Operating Behaviors” table.	07/2013

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MCF51JG256

MCF51JG256 Microcontroller

Features

- Operating characteristics
  - Voltage range 1.85 V to 3.6 V
  - Flash write voltage 1.85 V to 3.6 V
  - Temperature range (ambient) -40 °C to 85 °C
- Core features
  - Up to 50 MHz Version 1 (V1) ColdFire CPU
  - Provides 1.10 DMIPS(2.1) per MHz performance when running from internal RAM, 0.99 DMIPS per MHz when running from flash
  - Enhanced Multiply-Accumulate Unit (EMAC)
  - Hardware divide
- Clocks
  - 1 MHz to 32 MHz crystal oscillator
  - 32 kHz crystal oscillator
  - Multi-purpose clock generator(MCG)
- System debug, protection, and power management
  - Various stop, wait, and run modes to provide low power based on application needs
  - Illegal opcode and illegal address detection with programmable reset or processor exception response
  - Hardware CRC module to support fast cyclic redundancy checks
  - Cryptographic Acceleration Unit (CAU)
  - Random Number Generator Accelerator (RNGA)
- Debug
  - Integrated ColdFire DEBUG_Rev_B+ interface with single wire BDM connection
  - EzPort support flash In-System Programming
- DMA controller
  - Four independently programmable DMA controller channels for directly transferring data between system memory and I/O peripherals
- Timers
  - Motor control/general purpose timer (FTM)
  - 16-bit modulo timer (MTIM)
  - Low-power timer/pulse counter (LPTMR0)
- Communications
  - Universal asynchronous receivers/transmitters (UART)/Serial communications interface (SCI) with Smart Card support and FIFO
  - Serial peripheral interface (SPI) with FIFO
  - Inter-Integrated Circuit (I2C)
  - USB Full Speed/Low Speed OTG/Host/Device
  - Serial Audio Interface (SAI), to support Full Duplex Serial Interfaces with Frame Sync I2S, TDM, AC97, and CODEC, on MCF51Jx families only
- Input/output
  - All pins with interrupt with selectable polarity
  - Up to 14 pins with programmable glitch filter
  - Up to 14 rapid general purpose I/O (RGPIO) pins
- On-Chip Memory
  - Flash FlexMemory for additional program space or EEPROM
  - Flash security features and block protection
- System RAM
  - Protected from single-bit errors by nibble parity checking
  - Ability for software to insert single-bit errors to "check the checkers"

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1 Part identification

1.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

1.2 Format

Part numbers for this device have the following format:

Q CCCC DD MMM T PP

1.2.1 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• P = Prequalification • M = Fully qualified, general market flow
CCCC	Core code	CF51 = ColdFire V1
DD	Device number	JG
MMM	Memory size	256 = 256K Flash
T	Temperature range (°C)	C = –40 to 85
PP	Package identifier	• HS = 44 pin Laminate QFN (lead-free)

1.2.2 Example

MCF51JG256CHS

2 Terminology and guidelines

2.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

2.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

2.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

2.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

2.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

2.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

2.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

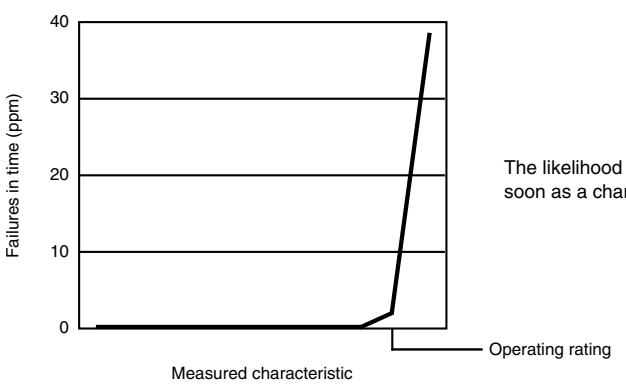
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

2.4.1 Example

This is an example of an operating rating:

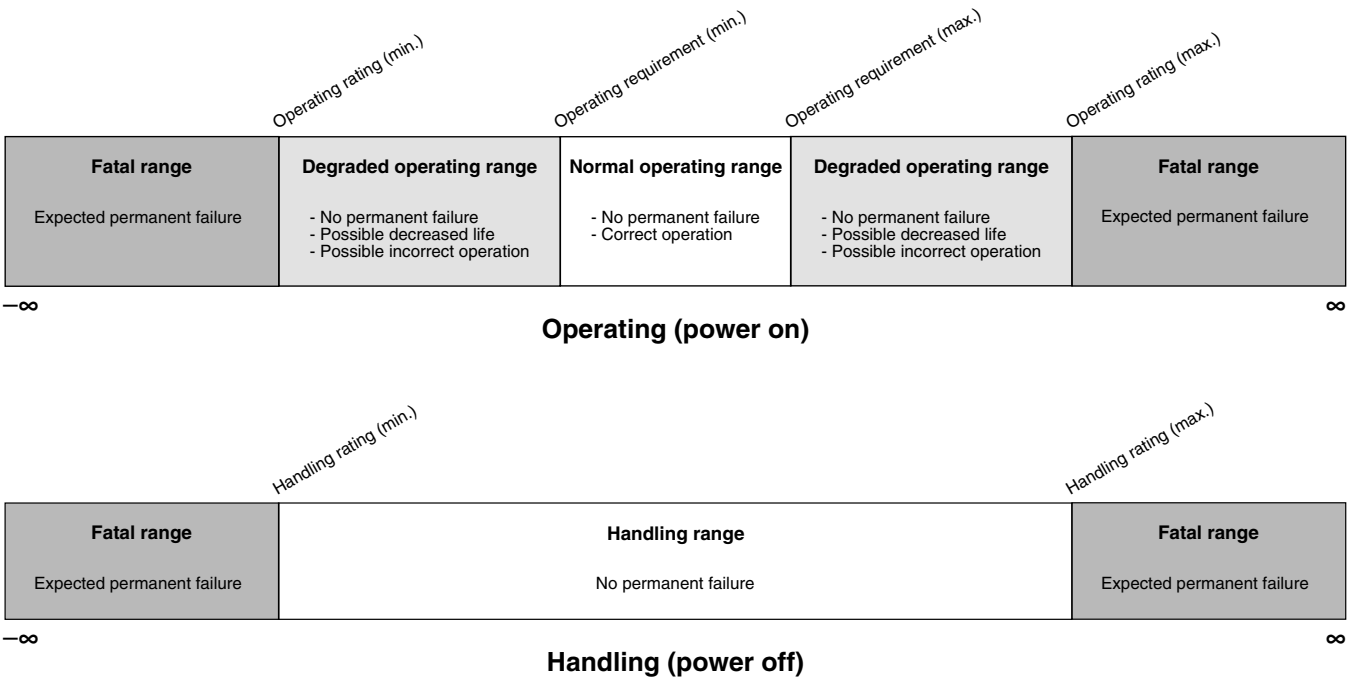
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

2.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

2.6 Relationship between ratings and operating requirements



2.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

2.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

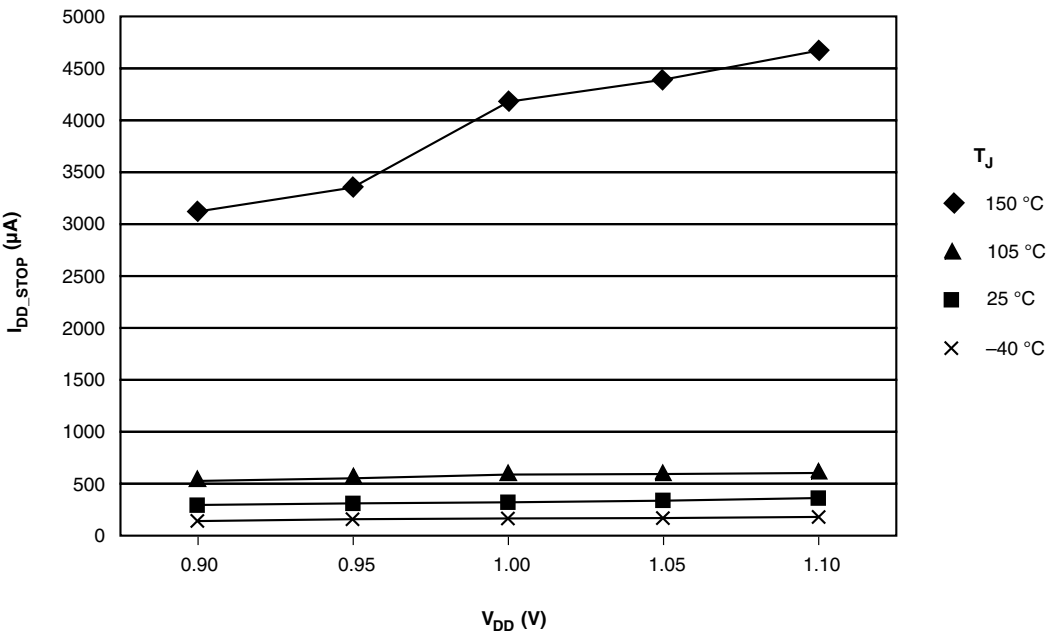
2.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

2.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



2.9 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

3 Ratings

3.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

3.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

3.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	500	V	2
V_{MM}	Electrostatic discharge voltage, machine model	-200	200	V	3
I_{LAT}	Latch-up Current at ambient temperature of 85 °C	-100	100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD22-A115, *Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)*.

3.4 Voltage and current operating ratings

Table 1. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	Input voltage	-0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
V_{USB_DP}	USB_DP input voltage	–0.3	3.63	V
V_{USB_DM}	USB_DM input voltage	–0.3	3.63	V
VREGIN	USB regulator input	–0.3	6.0	V

4 General

4.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

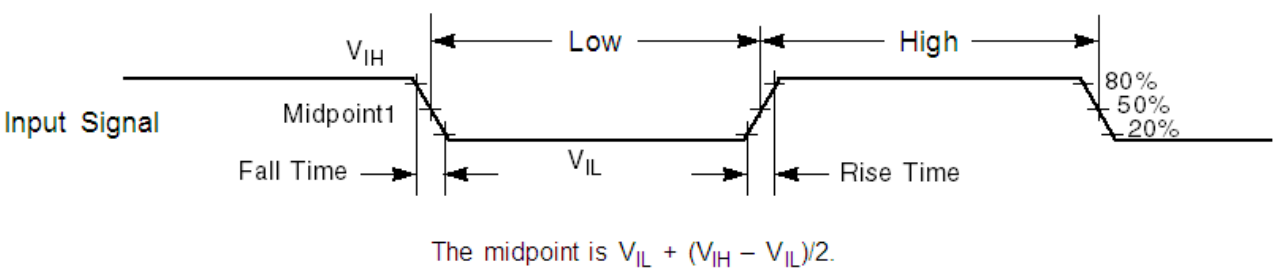


Figure 1. Input signal measurement reference

4.2 Nonswitching electrical specifications

4.2.1 Voltage and current operating requirements

Table 2. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.85	3.6	V	
V_{IH}	Input high voltage				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V	0.7 × V_{DD}	—	V	
	• 1.85 V ≤ V_{DD} ≤ 2.7 V	0.75 × V_{DD}	—	V	
V_{IL}	Input low voltage				2
	• 2.7 V ≤ V_{DD} ≤ 3.6 V	—	0.35 × V_{DD}	V	
	• 1.85 V ≤ V_{DD} ≤ 2.7 V	—	0.3 × V_{DD}	V	
I_{IC}	DC injection current — single pin				3
	• V_{IN} > V_{DD}	0	2	mA	
	• V_{IN} < V_{SS}	0	–0.2	mA	
	DC injection current — total MCU limit, includes sum of all stressed pins				
	• V_{IN} > V_{DD}	0	25	mA	
	• V_{IN} < V_{SS}	0	–5	mA	
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	--	V	

1. The device always interprets an input as a 1 when the input is greater than or equal to V_{IH} (min.) and less than or equal to V_{IH} (max.), regardless of whether input hysteresis is turned on.
2. The device always interprets an input as a 0 when the input is less than or equal to V_{IL} (max.) and greater than or equal to V_{IL} (min.), regardless of whether input hysteresis is turned on.
3. All functional non-supply pins (except RESET) are internally clamped to V_{SS} and V_{DD}. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{IN} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

4.2.2 LVD and POR operating requirements

Table 3. LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	

Table continues on the next page...

Table 3. LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.46	2.56	2.66	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.6	2.70	2.8	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.7	2.80	2.9	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.8	2.90	3.0	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.9	3.00	3.1	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	+/-80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.7	1.80	1.9	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.8	1.90	2.0	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.9	2.00	2.1	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.0	2.10	2.2	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	+/-60	—	mV	
t_{LPO}	Internal low power oscillator period factory trimmed	900	1000	1100	µs	

1. Rising thresholds are falling threshold + hysteresis voltage

4.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max	Unit	Notes
V_{OH}	Output high voltage — high drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -9 mA	V_{DD} – 0.5	—	V	
	• 1.85 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -3 mA	V_{DD} – 0.5	—	V	
	Output high voltage — low drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -2 mA	V_{DD} – 0.5	—	V	
	• 1.85 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -0.6 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max	Unit	Notes
V_{OL}	Output low voltage — high drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 9 mA	—	0.5	V	
	• 1.85 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 3 mA	—	0.5	V	
	Output low voltage — low drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 2 mA	—	0.5	V	
	• 1.85 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 0.6 mA	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin)				1
	• @ full temperature range	—	1.0	µA	
	• @ 25 °C	—	0.1	µA	
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	
R_{PU}	Internal pullup resistors	20	50	kΩ	2
R_{PD}	Internal pulldown resistors	20	50	kΩ	3

1. Tested by ganged leakage method
2. Measured at Vinput = V_{SS}
3. Measured at Vinput = V_{DD}

4.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx-RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock (and flash and FlexBus clocks) = 25 MHz

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.85 V to execution of the first instruction across the operating temperature range of the chip.	—	300	µs	1
	RUN → VLLS1 → RUN				1
	• RUN → VLLS1	—	4.4	µs	
	• VLLS1 → RUN	—	124	µs	
	RUN → VLLS2 → RUN				1
	• RUN → VLLS2	—	4.6	µs	
	• VLLS2 → RUN	—	83.6	µs	

Table continues on the next page...

Table 5. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	RUN → VLLS3 → RUN				1
	• RUN → VLLS3	—	4.4	µs	
	• VLLS3 → RUN	—	83.6	µs	
	RUN → VLPS → RUN				
	• RUN → VLPS	—	4.4	µs	
	• VLPS → RUN	—	4.6	µs	
	RUN → STOP → RUN				
	• RUN → STOP	—	4.4	µs	
	• STOP → RUN	—	4.6	µs	

1. Normal boot (FTFL_FOPT[LPBOOT] is 1)

4.2.5 Current consumption operating behaviors

Table 6. Current consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					1
	• @ 1.85 V	—	16	24	mA	
	• @ 3.0 V	—	16	24	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					2
	• @ 1.85 V	—	19.5	25.5	mA	
	• @ 3.0 V	—	20	26	mA	
I_{DD_WAIT}	Wait mode current at V_{DD} = 3.0 V	—	13	19	mA	3
I_{DD_STOP}	Stop mode current at V_{DD} = 3.0 V	—	0.4	1.8	mA	--
I_{DD_VLPR}	Very-low-power run mode current at V_{DD} = 3.0 V. All peripheral clocks disabled.	—	1.8	3.6	mA	4
I_{DD_VLPR}	Very-low-power run mode current at V_{DD} = 3.0 V. All peripheral clocks enabled.	—	1.8	3.6	mA	5
I_{DD_VLPW}	Very-low-power wait mode current at V_{DD} = 3 V	—	0.3	1.7	mA	6
I_{DD_VLPS}	Very-low-power stop mode current at V_{DD} = 3.0 V	—	50	900	µA	7
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at V_{DD} = 3.0 V	—	3.5	200	µA	7
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at V_{DD} = 3.0 V	—	2.8	110	µA	7
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at V_{DD} = 3.0 V	—	2.3	63	µA	7

1. 50 MHz CPU clock not including peripherals or external loads. 25 MHz bus clock. MCG configured for FEI mode. All peripheral clocks disabled.
2. 50 MHz CPU clock not including peripherals or external loads. 25 MHz bus clock. MCG configured for FEI mode. All peripheral clocks enabled.
3. 50 MHz CPU clock. 25 MHz bus clock. MCG configured for FEI mode.
4. 2 MHz CPU clock and 1 MHz bus clock. MCG configured for fast IRCLK mode. All peripheral clocks disabled. Code executing from flash.
5. 2 MHz CPU clock and 1 MHz bus clock. MCG configured for fast IRCLK mode. All peripheral clocks enabled, but peripherals are not in active operation. Code executing from flash.
6. 2 MHz CPU clock and 1 MHz bus clock. MCG configured for fast IRCLK mode. All peripheral clocks disabled.
7. OSC clocks disabled.

4.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode, except for 50 MHz core (FEI mode)
- For the All Peripheral Clocks Disabled curve, all peripheral clocks are disabled except flash
- For the All Peripheral Clocks Enabled curve, all peripheral clocks are enabled but peripherals are not in active operation
- No GPIOs toggled
- Code execution from flash memory

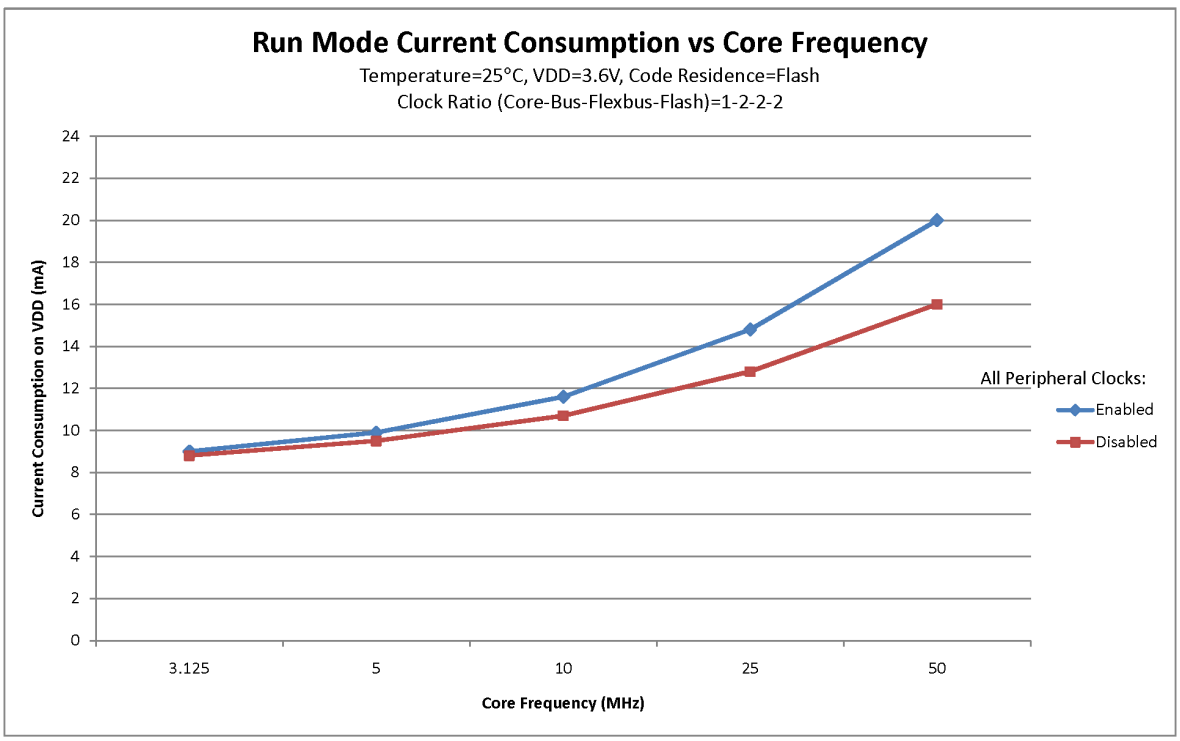


Figure 2. Run mode supply current vs. core frequency

4.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	12	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	14		
V_{RE3}	Radiated emissions voltage, band 3	150–500	11		
V_{RE4}	Radiated emissions voltage, band 4	500–1000	12		
V_{RE_IEC}	IEC level	0.15–1000	M	—	1, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions, IEC Standard 61967-2, Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported

emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. V_{DD} = 3 V, T_A = 25 °C, f_{OSC} = 16 MHz (crystal), f_{BUS} = 25 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*.

4.2.6.1 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

4.2.7 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

4.3 Switching electrical specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	50	MHz	
f_{SYS_USB}	System and core clock when USB in operation	20	—	MHz	
f_{BUS}	Bus clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode					
f_{SYS}	System and core clock	—	1.2	MHz	
f_{BUS}	Bus clock	—	0.6	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	

4.3.1 General Switching Specifications

These general purpose specifications apply to all signals configured for GPIO, MTIM, IRQ, and I^2C signals. The conditions are 50 pF load, V_{DD} = 1.85 V to 3.6 V and full temperature range. The GPIO are set for high drive, no slew rate control and no input filter, digital or analog, unless otherwise specified.

Table 10. General control timing

Num	Characteristic	Min	Max	Unit
G1	Bus clock from CLK_OUT pin high to GPIO output valid	—	32	ns
G2	Bus clock from CLK_OUT pin high to GPIO output invalid (output hold)	4	—	ns
G3	GPIO input valid to bus clock high	28	—	ns
G4	Bus clock from CLK_OUT pin high to GPIO input invalid	—	4	ns
G5	GPIO pin interrupt pulse width (digital glitch filter disabled) Synchronous path[1]	1.5	—	Bus clock cycles
G6	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) Asynchronous path[2]	100	—	ns
G7	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) Asynchronous path[2]	50	—	ns
G8	External reset pulse width (digital glitch filter disabled)	100	—	ns
G9	Mode select (MS) hold time after reset deassertion	2	—	Bus clock cycles

1. The greater synchronous or asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.

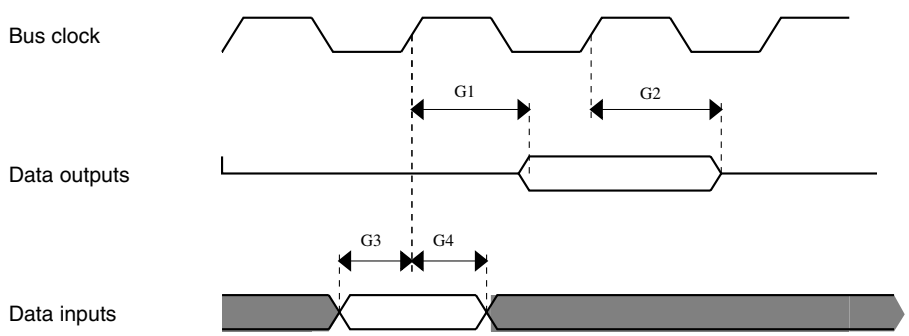


Figure 3. GPIO timing diagram

These general purpose specifications apply to all signals configured for RGPIO, FTM, and UART/SCI. The conditions are 25 pF load, V_{DD} = 1.85 V to 3.6 V, and full temperature range. The GPIO are set for high drive, no slew rate control and no input filter, digital or analog, unless otherwise specified.

Table 11. RGPIO/SCI general control timing

Num	Characteristic	Min	Max	Unit
R1	CPUCLK from CLK_OUT pin high to GPIO output valid	—	16	ns
R2	CPUCLK from CLK_OUT pin high to GPIO output invalid (output hold)	2	—	ns
R3	GPIO input valid to bus clock high	14	—	ns
R4	CPUCLK from CLK_OUT pin high to GPIO input invalid	—	2	ns
R5	GPIO pin interrupt pulse width (digital glitch filter disabled) Synchronous path[1]	1.5	—	CPU clock cycles

1. The greater synchronous or asynchronous timing must be met.

4.4 Thermal specifications

4.4.1 Thermal operating requirements

Table 12. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	105	°C
T_A	Ambient temperature	–40	85	°C

4.4.2 Thermal attributes

Board type	Symbol	Description	44 MAPLGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	94	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	47	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	78	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	43	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	25	°C/W	2

Table continues on the next page...

Board type	Symbol	Description	44 MAPLGA	Unit	Notes
—	$R_{\theta JC}$	Thermal resistance, junction to case	30	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	4	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions —Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions —Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions —Natural Convection (Still Air)*.

5 Peripheral specifications

5.1 Core modules

5.1.1 Debug specifications

Table 13. Background debug mode (BDM) timing

Number	Symbol	Description	Min.	Max.	Unit
1	t_{MSSU}	BKGD/MS setup time after issuing background debug force reset to enter user mode or BDM	500	—	ns
2	t_{MSH}	BKGD/MS hold time after issuing background debug force reset to enter user mode or BDM[1]	100	—	µs

1. To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

5.2 System modules

5.2.1 EzPort switching specifications

Table 14. EzPort signal timing

Num	Description	Min.	Max.	Unit
—	Operating voltage	1.85	3.6	V

Table continues on the next page...

Table 14. EzPort signal timing (continued)

Num	Description	Min.	Max.	Unit
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{SYS}/8$	MHz
EP2	$\overline{\text{EZP\_CS}}$ negation to next $\overline{\text{EZP\_CS}}$ assertion	2 x t_{EZP_CK}	—	ns
EP3	$\overline{\text{EZP\_CS}}$ input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to $\overline{\text{EZP\_CS}}$ input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	5	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output setup	—	12	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	$\overline{\text{EZP\_CS}}$ negation to EZP_Q tri-state	—	12	ns

NOTE

Input slew rate of 2 ns and output load of 35 pF.

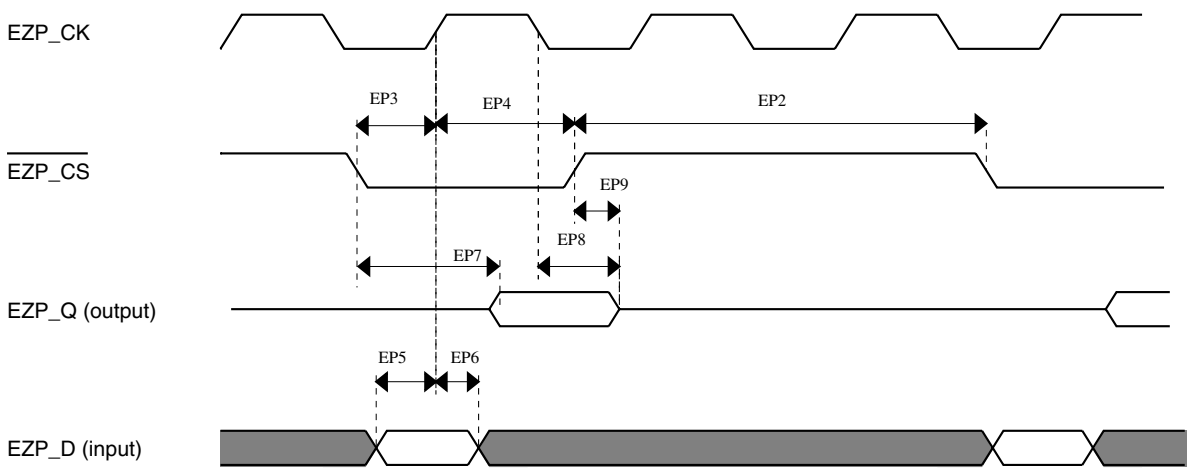


Figure 4. EzPort timing diagram

5.3 Memories and memory interfaces

5.3.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

5.3.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 15. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversblk32k}$	Erase Block high-voltage time for 32 KB	—	52	452	ms	1
$t_{hversblk128k}$	Erase Block high-voltage time for 128 KB	—	208	1808	ms	1

1. Maximum time based on expectations at cycling end-of-life.

5.3.1.2 Flash timing specifications — commands

Table 16. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					
$t_{rd1blk32k}$	• 32 KB data flash	—	—	0.5	ms	
$t_{rd1blk128k}$	• 128 KB program flash	—	—	1.7	ms	
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	
	Erase Flash Block execution time					2
$t_{ersblk32k}$	• 32 KB data flash	—	55	465	ms	
$t_{ersblk128k}$	• 128 KB program flash	—	220	1850	ms	
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
	Program Section execution time					
$t_{pgmsec512}$	• 512 bytes flash	—	4.7	—	ms	
$t_{pgmsec1k}$	• 1 KB flash	—	9.3	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	
t_{ersall}	Erase All Blocks execution time	—	490	4200	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

Table continues on the next page...

Table 16. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Swap Control execution time					
$t_{swapx01}$	• control code 0x01	—	200	—	µs	
$t_{swapx02}$	• control code 0x02	—	70	150	µs	
$t_{swapx04}$	• control code 0x04	—	70	150	µs	
$t_{swapx08}$	• control code 0x08	—	—	30	µs	
	Program Partition for EEPROM execution time					
$t_{pgmpart32k}$	• 32 KB FlexNVM	—	70	—	ms	
	Set FlexRAM Function execution time:					
$t_{setramff}$	• Control Code 0xFF	—	50	—	µs	
$t_{setram8k}$	• 8 KB EEPROM backup	—	0.3	0.5	ms	
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.7	1.0	ms	
	Byte-write to FlexRAM for EEPROM operation					
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	175	260	µs	3
	Byte-write to FlexRAM execution time:					
$t_{eewr8b8k}$	• 8 KB EEPROM backup	—	340	1700	µs	
$t_{eewr8b16k}$	• 16 KB EEPROM backup	—	385	1800	µs	
$t_{eewr8b32k}$	• 32 KB EEPROM backup	—	475	2000	µs	
	Word-write to FlexRAM for EEPROM operation					
$t_{eewr16bers}$	Word-write to erased FlexRAM location execution time	—	175	260	µs	
	Word-write to FlexRAM execution time:					
$t_{eewr16b8k}$	• 8 KB EEPROM backup	—	340	1700	µs	
$t_{eewr16b16k}$	• 16 KB EEPROM backup	—	385	1800	µs	
$t_{eewr16b32k}$	• 32 KB EEPROM backup	—	475	2000	µs	
	Longword-write to FlexRAM for EEPROM operation					
$t_{eewr32bers}$	Longword-write to erased FlexRAM location execution time	—	360	540	µs	
	Longword-write to FlexRAM execution time:					
$t_{eewr32b8k}$	• 8 KB EEPROM backup	—	545	1950	µs	
$t_{eewr32b16k}$	• 16 KB EEPROM backup	—	630	2050	µs	
$t_{eewr32b32k}$	• 32 KB EEPROM backup	—	810	2250	µs	

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

5.3.1.3 Flash high voltage current behaviors

Table 17. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

5.3.1.4 Reliability specifications

Table 18. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	Program Flash					
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2
	Data Flash					
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycd}$	Cycling endurance	10 K	50 K	—	cycles	2
	FlexRAM as EEPROM					
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	50	—	years	
$t_{nvmretee10}$	Data retention up to 10% of write endurance	20	100	—	years	
	Write endurance					3
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	35 K	175 K	—	writes	
$n_{nvmwree128}$	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	—	writes	
$n_{nvmwree512}$	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	—	writes	
$n_{nvmwree4k}$	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	
$n_{nvmwree8k}$	• EEPROM backup to FlexRAM ratio = 8192	20 M	100 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 105°C.
3. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 105°C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup. Minimum and typical values assume all byte-writes to FlexRAM.

5.3.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the flash memory module to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

$$\text{Writes\_FlexRAM} = \frac{\text{EEPROM} - 2 \times \text{EEESIZE}}{\text{EEESIZE}} \times \text{Write\_efficiency} \times n_{nvmcycd}$$

where

- Writes_FlexRAM — minimum number of writes to each FlexRAM location
- EEPROM — allocated FlexNVM based on DEPART; entered with the Program Partition command
- EEESIZE — allocated FlexRAM based on DEPART; entered with the Program Partition command
- Write_efficiency —
  - 0.25 for 8-bit writes to FlexRAM
  - 0.50 for 16-bit or 32-bit writes to FlexRAM
- $n_{nvmcycd}$ — data flash cycling endurance (the following graph assumes 10,000 cycles)

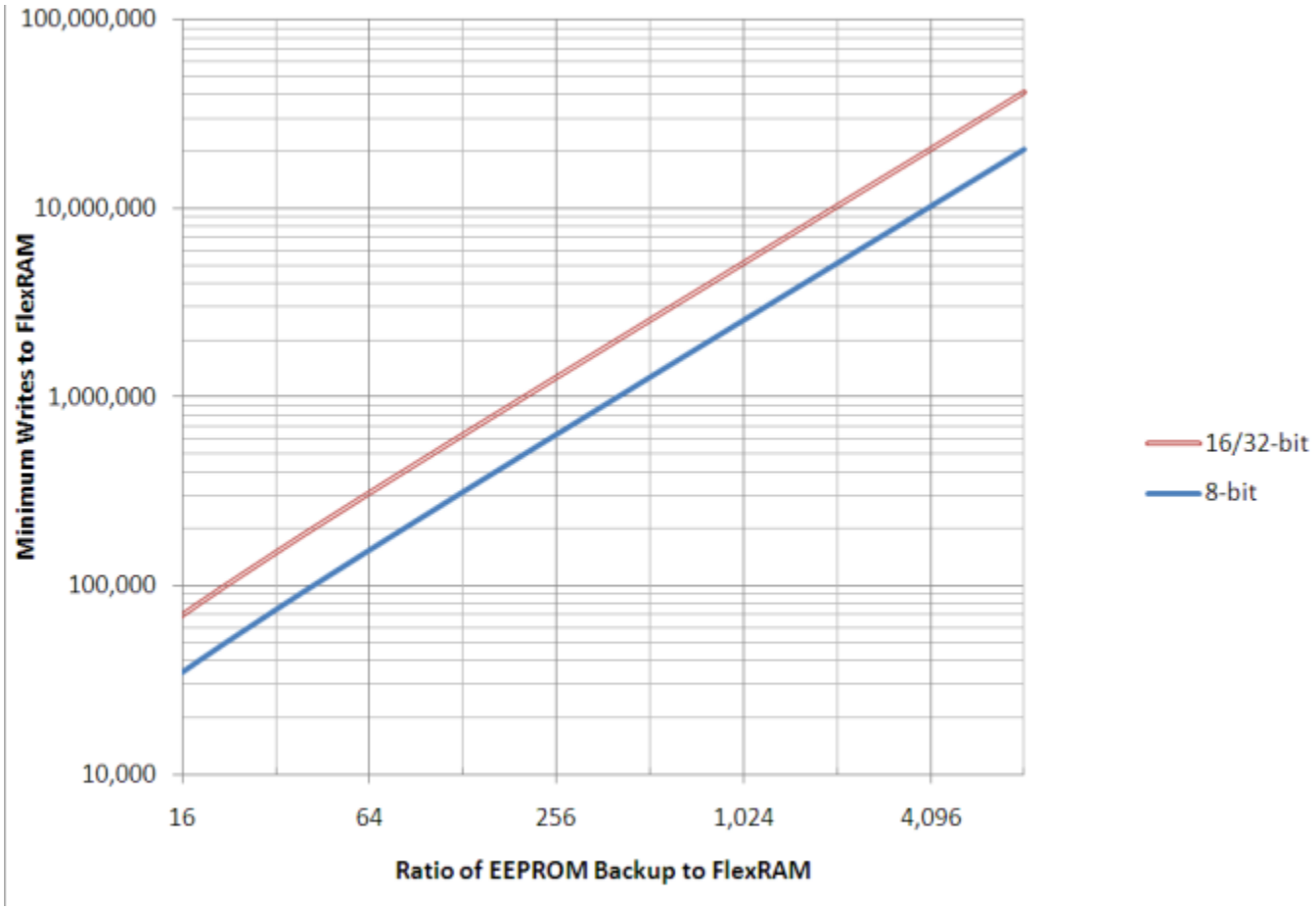


Figure 5. EEPROM backup writes to FlexRAM

5.4 Clock modules

5.4.1 MCG specifications

Table 19. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
Δf_{ints_t}	Total deviation of internal reference frequency (slow clock) over voltage and temperature	—	± 0.5	± 14	%	1, 2
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed	31.0	—	34.0	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.25	± 0.6	$\%f_{dco}$	2
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	± 0.5	± 14	$\%f_{dco}$	1, 2

Table continues on the next page...

Table 19. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—	± 0.5	—	$\%f_{dco}$	1, 2
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		—	4	—	MHz	
Δf_{intf_t}	Total deviation of internal reference frequency (fast clock) over voltage and temperature		—	± 10	± 15	%	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	3
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{ints_t}	19.84	20.97	21.76	MHz	4,
		Mid range (DRS=01) 1280 × f_{ints_t}	39.68	41.94	43.52	MHz	
		Mid-high range (DRS=10) 1920 × f_{ints_t}	59.52	62.91	65.28	MHz	
		High range (DRS=11) 2560 × f_{ints_t}	79.36	83.89	87.04	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{ints_t}	—	23.99	—	MHz	5, 6
		Mid range (DRS=01) 1464 × f_{ints_t}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{ints_t}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f_{ints_t}	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter		—	70	140	ps	7
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	8
PLL							
f_{vco}	VCO operating frequency		48.0	—	100	MHz	
I_{pll}	PLL operating current • PLL @ 96 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 48)		—	1060	—	µA	9
I_{pll}	PLL operating current • PLL @ 48 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 24)		—	600	—	µA	9
f_{pll_ref}	PLL reference frequency range		2.0	—	4.0	MHz	

Table continues on the next page...

Table 19. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 48 MHz • f_{vco} = 100 MHz	 — —	 120 50	 — —	 ps ps	10
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS) • f_{vco} = 48 MHz • f_{vco} = 100 MHz	 — —	 1350 600	 — —	 ps ps	10
D_{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	150×10^{-6} + 1075(1/f_{pll_ref})	s	11

1. Typ. value indicates typical deviation at 25 °C. Max. value indicates maximum deviation from 25 °C to the temperature extreme.
2. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
3. Subject to change after process characterization.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
9. Excludes any oscillator currents that are also consuming power while PLL is in operation.
10. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
11. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

5.4.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

5.4.2.1 Oscillator DC electrical specifications

Table 20. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.85	—	3.6	V	

Table continues on the next page...

Table 20. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 1 MHz	—	200	—	µA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz (RANGE=01)	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	—	µA	
	• 1 MHz	—	300	—	µA	
	• 4 MHz	—	400	—	µA	
	• 8 MHz (RANGE=01)	—	500	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	

Table continues on the next page...

Table 20. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)					
	• 1 MHz resonator	—	6.6	—	kΩ	
	• 2 MHz resonator	—	3.3	—	kΩ	
	• 4 MHz resonator	—	0	—	kΩ	
	• 8 MHz resonator	—	0	—	kΩ	
	• 16 MHz resonator	—	0	—	kΩ	
	• 20 MHz resonator	—	0	—	kΩ	
	• 32 MHz resonator	—	0	—	kΩ	
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x,C_y can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

5.4.2.2 Oscillator frequency specifications

Table 21. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	1	—	8	MHz	

Table continues on the next page...

Table 21. Oscillator frequency specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	1000	—	ms	1, 2
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	500	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Proper PC board layout procedures must be followed to achieve specifications.
2. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

5.4.3 32 kHz Oscillator Electrical Characteristics

This section describes the module electrical characteristics.

5.4.3.1 32 kHz oscillator DC electrical specifications

Table 22. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.85	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

5.4.3.2 32 kHz oscillator frequency specifications

Table 23. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.

2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

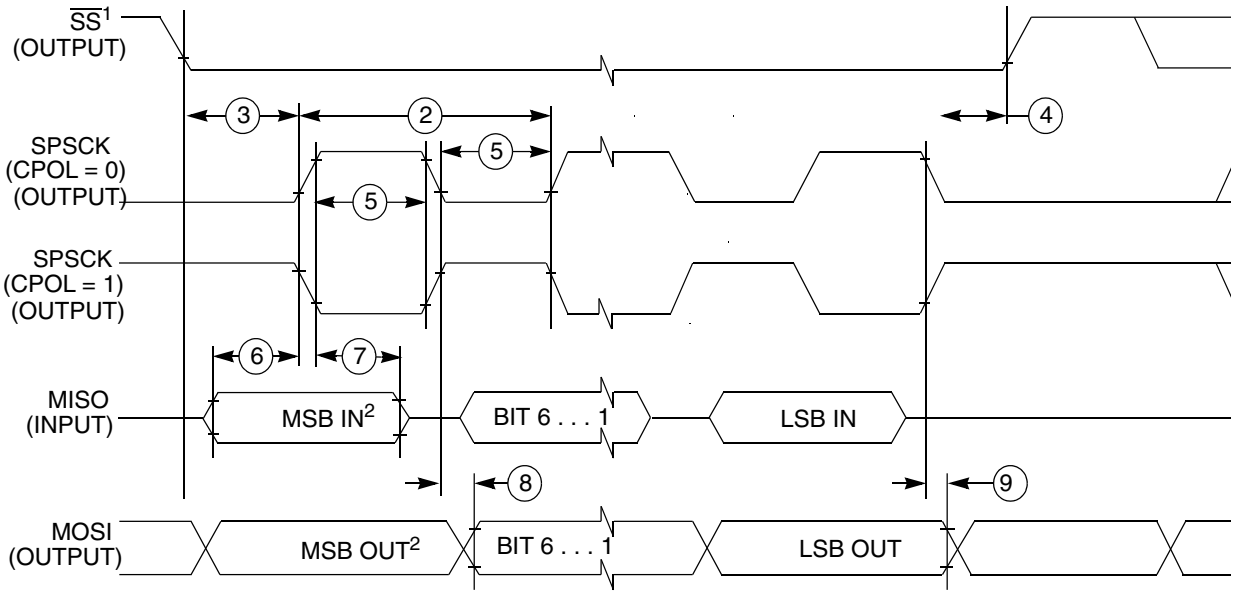
5.5 Communication interfaces

5.5.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted, input slew rate of 2 ns and 35 pF load on all SPI pins. All timing assumes slew rate control is disabled (PCTLx_SRE[PTSRE]=0, fastest slew rate configuration) and high drive strength is enabled for SPI output pins.

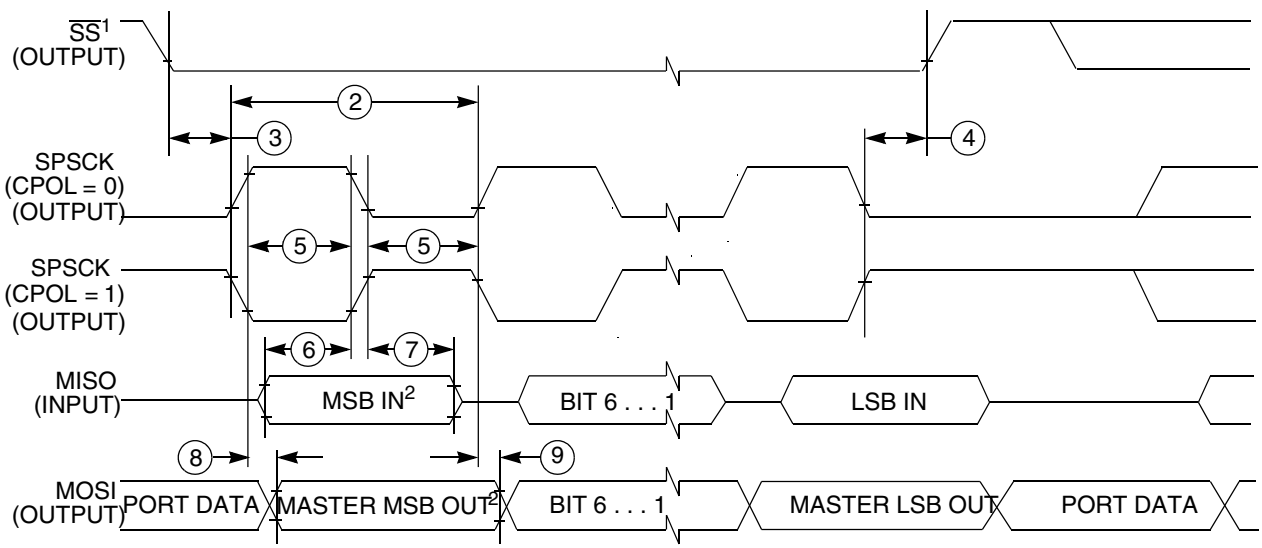
Table 24. SPI master mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	$f_{BUS}/2048$	$f_{BUS}/2$	Hz	f_{BUS} is the bus clock as defined in Table 9.
2	t_{SPSCK}	SPSCK period	2 x t_{BUS}	2048 x t_{BUS}	ns	t_{BUS} = 1/ f_{BUS}
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{BUS} - 30	1024 x t_{BUS}	ns	—
6	t_{SU}	Data setup time (inputs)	21	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	25	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—



1. If configured as an output.
2. LSBF = 0. For LSBF = 1. bit order is LSB. bit 1. .... bit 6. MSB.

Figure 6. SPI master mode timing (CPHA=0)



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 7. SPI master mode timing (CPHA=1)

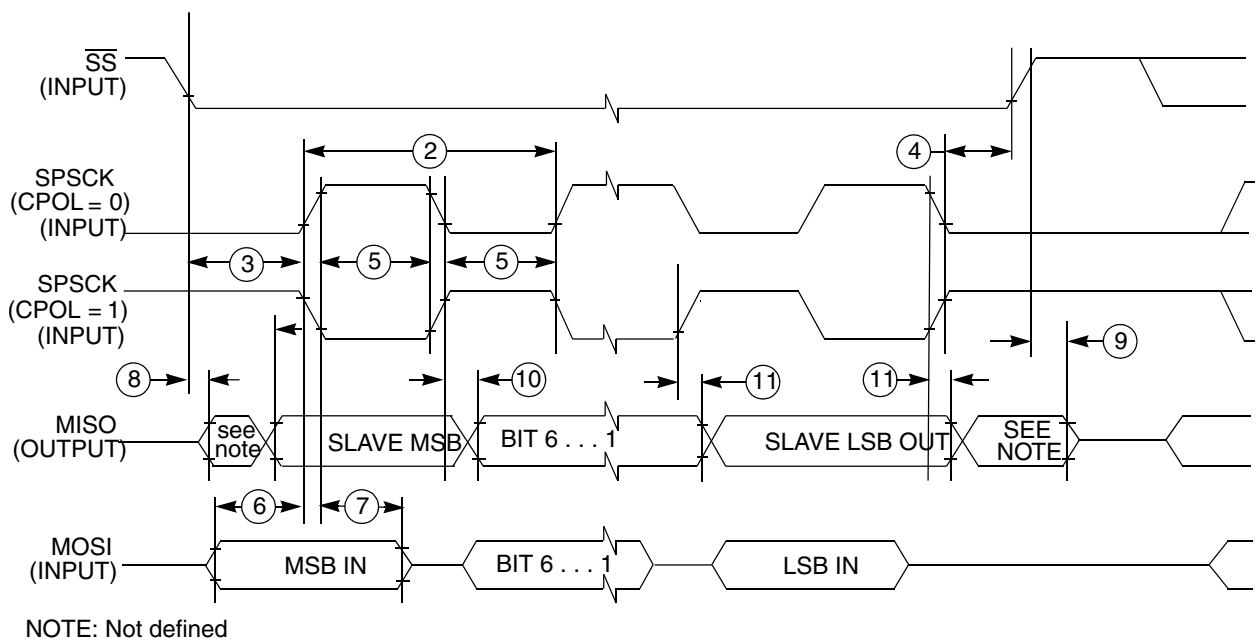
Table 25. SPI slave mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	0	$f_{BUS}/4$	Hz	f_{BUS} is the bus clock as defined in Table 9.
2	t_{SPSCK}	SPSCK period	4 x t_{BUS}	—	ns	t_{BUS} = 1/ f_{BUS}

Table continues on the next page...

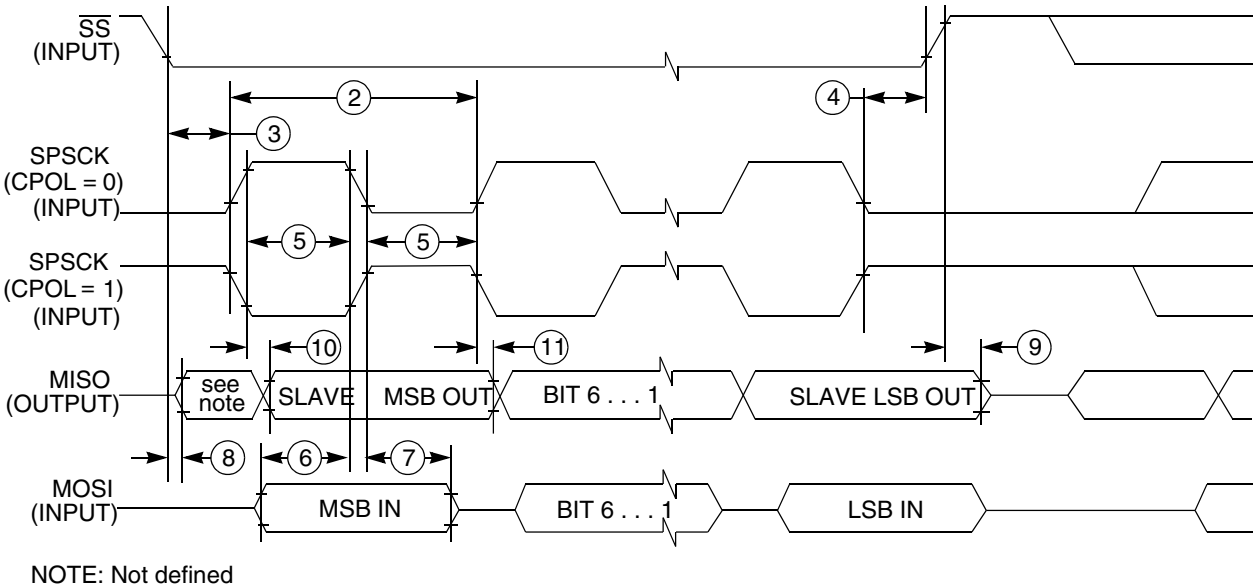
Table 25. SPI slave mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Comment
3	t_{Lead}	Enable lead time	1	—	t_{BUS}	—
4	t_{Lag}	Enable lag time	1	—	t_{BUS}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{BUS} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	19.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_a	Slave access time	—	t_{BUS}	ns	Time to data active from high-impedance state
9	t_{dis}	Slave MISO disable time	—	t_{BUS}	ns	Hold time to high-impedance state
10	t_v	Data valid (after SPSCK edge)	—	27	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—



NOTE: Not defined

Figure 8. SPI slave mode timing (CPHA=0)



NOTE: Not defined

Figure 9. SPI slave mode timing (CPHA=1)

5.5.2 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit **usb.org**.

5.5.3 USB DCD electrical specifications

Table 26. USB DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DP_SRC}	USB_DP source voltage (up to 250 µA)	0.5	—	0.7	V
V_{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I_{DP_SRC}	USB_DP source current	7	10	13	µA
I_{DM_SINK}	USB_DM sink current	50	100	150	µA
R_{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	kΩ
V_{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

5.5.4 VREG electrical specifications

Table 27. VREG electrical specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	

Table continues on the next page...

Table 27. VREG electrical specifications (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
I_{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	120	186	µA	
I_{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	10	µA	
I_{DDoff}	Quiescent current — Shutdown mode • VREGIN = 5.0 V and temperature=25 °C • Across operating voltage and temperature	 — —	 650 —	 — 4	 nA µA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	120	mA	
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) > 3.6 V • Run mode • Standby mode	 3 2.1	 3.3 2.8	 3.6 3.6	 V V	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C_{OUT}	External output capacitor	1.76	2.2	8.16	µF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I_{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

5.5.5 I2S/SAI Switching Specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

Table 28. I2S/SAI master mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time[1]	40		ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK cycle time (output)[1] I2S_RX_BCLK cycle time (output)[1]	80 160	— —	ns

Table continues on the next page...

Table 28. I2S/SAI master mode timing (continued)

Num.	Characteristic	Min.	Max.	Unit
S4	I2S_TX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	25	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns
S11	I2S_TX_FS input assertion to I2S_TXD output valid[2]	—	21	ns

1. This parameter is limited in VLPx modes.
2. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

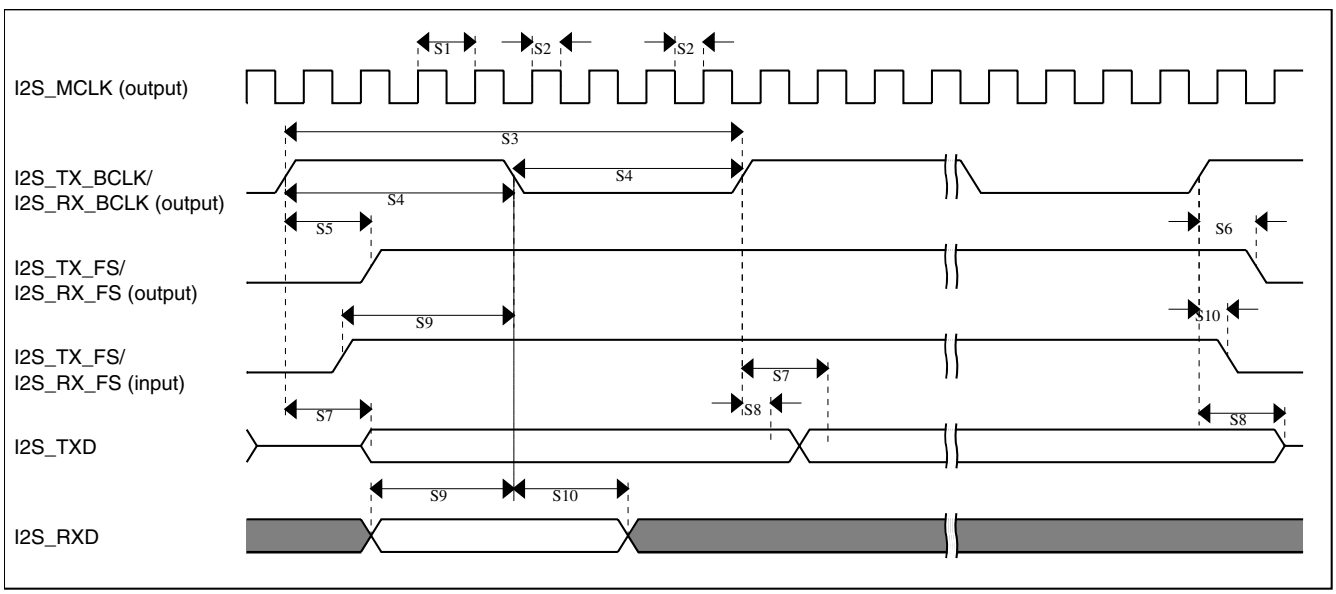


Figure 10. I2S/SAI timing — master modes

Table 29. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_RX_BCLK cycle time (input)	80	—	ns
	I2S_TX_BCLK cycle time (input)	160	—	
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns

Table continues on the next page...

Table 29. I2S/SAI slave mode timing (continued)

Num.	Characteristic	Min.	Max.	Unit
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	29	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	21	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

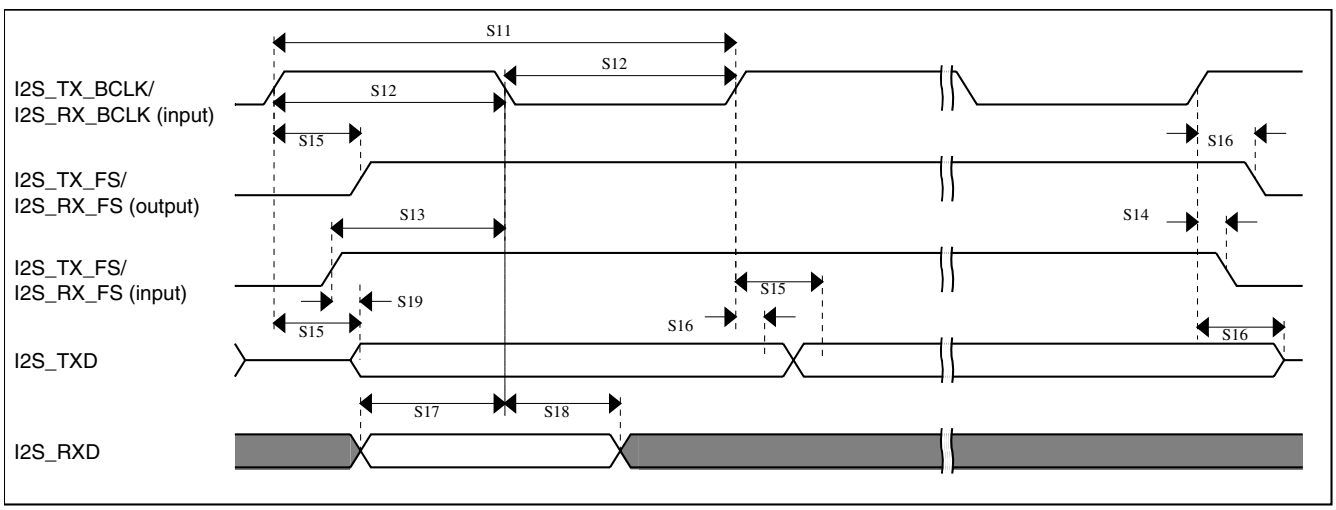


Figure 11. I2S/SAI timing — slave modes

6 Dimensions

6.1 Obtaining package dimensions

Package dimensions are provided in package drawing.

To find a package drawing, go to **freescale.com** and perform a keyword search for the drawing's document number:

Package	Freescale Document Number
44-pin MAPLGA	98ASA00239D

7 Pinout

7.1 Pinout Diagram

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin.

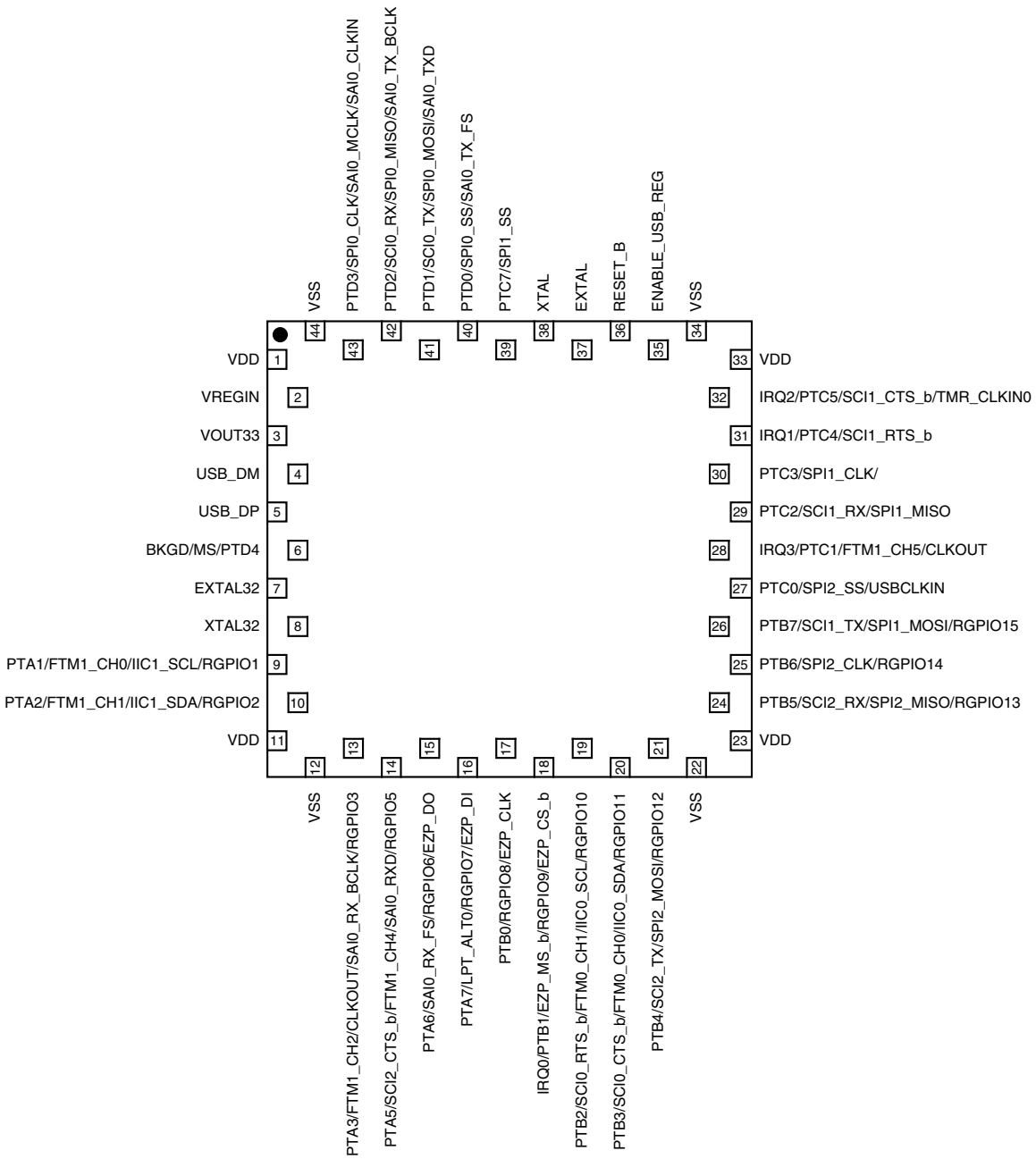


Figure 12. MCF51JG256 44-pin MAPLGA Pinout Diagram

NOTE

PTD4 is adjacent to EXTAL32 and may inject coupling noise on EXTAL32 when both PTD4 as well as EXTAL32 is being used. So it is highly recommended that PTD4 be only used for the cases where EXTAL32 is not used at all and system relies on internal RC clock or external EXTAL clock.

7.2 Signal Multiplexing and Pin Assignments

44 MAPLGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	EZPORT
1	VDD	VDD	VDD						
2	VREGIN	VREGIN	VREGIN						
3	VOUT33	VOUT33	VOUT33						
4	USB_DM	USB_DM	USB_DM						
5	USB_DP	USB_DP	USB_DP						
6	BKGD/ MS/ PTD4	BKGD/ MS	Disabled	PTD4	BKGD	MS			
7	EXTAL32	EXTAL32	EXTAL32						
8	XTAL32	XTAL32	XTAL32						
9	PTA1/ FTM1_CH0/ IIC1_SCL/ RGPIO1	Disabled	Disabled	PTA1	FTM1_CH0		IIC1_SCL	RGPIO1	
10	PTA2/ FTM1_CH1/ IIC1_SDA/ RGPIO2	Disabled	Disabled	PTA2	FTM1_CH1		IIC1_SDA	RGPIO2	
11	VDD	VDD	VDD						
12	VSS	VSS	VSS						
13	PTA3/ FTM1_CH2/ CLKOUT/ SAI0_RX_BCLK/ RGPIO3	Disabled	Disabled	PTA3	FTM1_CH2	CLKOUT	SAI0_RX_BCLK	RGPIO3	
14	PTA5/ SCI2_CTS_b/ FTM1_CH4/ SAI0_RXD/ RGPIO5	Disabled	Disabled	PTA5	SCI2_CTS_b	FTM1_CH4	SAI0_RXD	RGPIO5	
15	PTA6/ SAI0_RX_FS/ RGPIO6/ EZP_DO	Disabled	Disabled	PTA6			SAI0_RX_FS	RGPIO6	EZP_DO
16	PTA7/ LPT_ALT0/	Disabled	Disabled	PTA7	LPT_ALT0			RGPIO7	EZP_DI

44 MAPLGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	EZPORT
	RGPIO7/ EZP_DI								
17	PTB0/ RGPIO8/ EZP_CLK	Disabled	Disabled	PTB0				RGPIO8	EZP_CLK
18	IRQ0/ PTB1/ EZP_MS_b/ RGPIO9/ EZP_CS_b	IRQ0	IRQ0	PTB1	EZP_MS_b			RGPIO9	EZP_CS_b
19	PTB2/ SCI0_RTS_b/ FTM0_CH1/ IIC0_SCL/ RGPIO10	Disabled	Disabled	PTB2	SCI0_RTS_b	FTM0_CH1	IIC0_SCL	RGPIO10	
20	PTB3/ SCI0_CTS_b/ FTM0_CH0/ IIC0_SDA/ RGPIO11	Disabled	Disabled	PTB3	SCI0_CTS_b	FTM0_CH0	IIC0_SDA	RGPIO11	
21	PTB4/ SCI2_TX/ SPI2_MOSI/ RGPIO12	Disabled	Disabled	PTB4	SCI2_TX	SPI2_MOSI		RGPIO12	
22	VSS	VSS	VSS						
23	VDD	VDD	VDD						
24	PTB5/ SCI2_RX/ SPI2_MISO/ RGPIO13	Disabled	Disabled	PTB5	SCI2_RX	SPI2_MISO		RGPIO13	
25	PTB6/ SPI2_CLK/ RGPIO14	Disabled	Disabled	PTB6		SPI2_CLK		RGPIO14	
26	PTB7/ SCI1_TX/ SPI1_MOSI/ RGPIO15	Disabled	Disabled	PTB7	SCI1_TX	SPI1_MOSI		RGPIO15	
27	PTC0/ SPI2_SS/ USBCLKIN	Disabled	Disabled	PTC0		SPI2_SS		USBCLKIN	
28	IRQ3/ PTC1/ FTM1_CH5/ CLKOUT	IRQ3	IRQ3	PTC1	FTM1_CH5	CLKOUT			
29	PTC2/ SCI1_RX/ SPI1_MISO	Disabled	Disabled	PTC2	SCI1_RX	SPI1_MISO			
30	PTC3/ SPI1_CLK/	Disabled	Disabled	PTC3		SPI1_CLK			

44 MAPLGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	EZPORT
31	IRQ1/ PTC4/ SCI1_RTS_b	IRQ1	IRQ1	PTC4	SCI1_RTS_b				
32	IRQ2/ PTC5/ SCI1_CTS_b/ TMR_CLKIN0	IRQ2	IRQ2	PTC5	SCI1_CTS_b	TMR_CLKIN0			
33	VDD	VDD	VDD						
34	VSS	VSS	VSS						
35	ENABLE_USB_ REG	ENABLE_USB_ REG	ENABLE_USB_ REG						
36	RESET_B	RESET_B	RESET_B						
37	EXTAL	EXTAL	EXTAL						
38	XTAL	XTAL	XTAL						
39	PTC7/ SPI1_SS	Disabled	Disabled	PTC7		SPI1_SS			
40	PTD0/ SPI0_SS/ SAI0_TX_FS	Disabled	Disabled	PTD0	SPI0_SS		SAI0_TX_FS		
41	PTD1/ SCI0_TX/ SPI0_MOSI/ SAI0_TXD	Disabled	Disabled	PTD1	SCI0_TX	SPI0_MOSI	SAI0_TXD		
42	PTD2/ SCI0_RX/ SPI0_MISO/ SAI0_TX_BCLK	Disabled	Disabled	PTD2	SCI0_RX	SPI0_MISO	SAI0_TX_BCLK		
43	PTD3/ SPI0_CLK/ SAI0_MCLK/ SAI0_CLKIN	Disabled	Disabled	PTD3		SPI0_CLK	SAI0_MCLK/ SAI0_CLKIN		
44	VSS	VSS	VSS						

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