EVBUM2280/D

KAI-11002 Evaluation Timing Specification

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EVAL BOARD USER'S MANUAL

Altera Code Version Description

The Altera code described in this document is intended for use in the AD984X Timing Board. The code is written specifically for use with the following system configuration:

Table 1. SYSTEM CONFIGURATION

Evaluation Board Kit:	PN
Timing Generator Board	Board Model 3E8180 (AD9845 30 MHz)
KAI−11002 CCD Imager Board	Board Model 3E8187
Framegrabber Board	National Instruments model PCI−1424

ALTERA CODE FEATURES / FUNCTIONS

The Altera Programmable Logic Device (PLD) has three major functions:

Timing Generator

The PLD serves as a state machine based timing generator whose outputs interface to the KAI−11002, the AD9845 Analog Front End (AFE), and the PCI−1424 Framegrabber. The behavior of these output signals is dependent upon the current state of the state machine. External digital inputs, as well as jumpers on the board can be used to set the conditions of certain state transitions (See Table 2). In this manner, the board may be run in any of the following operating modes:

- Single Capture Mode Operation (Trigger, Electronic shutter, Integrate, Fast Dump Vertical CCD's, Diode Transfer, CCD Readout)
- Continuous Free−running Mode Operation (Diode Transfer, CCD Readout, Diode Transfer, CCD Readout)
- Single Output or Dual Output Mode Operation
- 2 x 2 Binning Mode Operation
- Fifteen different Integration Mode Options (Sub−frame Integration Times utilizing Electronic Shuttering as well as Multi−frame Integration Times)
- Four different Optical Black Clamp (AD9845 CLPOB) Modes

Delay Line Initialization

Upon power up, or when the BOARD_RESET button is depressed, the PLD programs the 10 silicon delay IC's on the Timing Generator Board to their default delay settings via a 3 wire serial interface. See Table 10 for details.

AFE Register Initialization

Upon power up, or when the BOARD_RESET button is depressed, the PLD programs the registers of the two AFE chips on the Timing Generator Board to their default settings via a 3 wire serial interface. See Table 11 for details.

ALTERA CODE I/O

Table 2. INPUTS

Symbol	Description
POWER_ON_DELAY	The rising edge of this signal clears and re−initializes the PLD
SYSTEM_CLK	60 MHz clock, 2X the desired pixel clock rate
INTEGRATE_CLK	Single capture mode integration timing control clock
JMP0	Output mode select (High = Dual / Low = Single)
JMP1	Operating mode select (High = Single Capture / Low = Free Running)
JMP2	Binning select control line (High = 2x2 binning / Low = no binning)
JMP3	Not used
DIO0	External trigger in Single Capture operating mode
DIO[5..1]	Integration time select lines in Single Capture operating mode
DIO[8..6]	Electronic shutter mode control lines (See Table 14)
DIO[11..9]	Free Running Multi frame integration mode control lines (See Table 12 and Table 13)
DIO[13..12]	AD9845 CLPOB MODE control lines (See Table 9)
DIO[19..14]	(Not used for KAI−11002 operation)

Table 3. OUTPUTS

Symbol	Description
V1_CLK	KAI−11002 CCD V1 Clock
V2_CLK	KAI−11002 CCD V2 Clock
H1_CLK	KAI−11002 CCD H1BL, H1SL, H1SR, H1L Left, H1L Right Clocks
H1BR_CLK	KAI−11002 CCD H1BR Clock
H2_CLK	KAI−11002 CCD H2BL, H2SL, H2SR, Clocks
H2BR_CLK	KAI−11002 CCD H2BR Clock
R_CLK	KAI−11002 CCD Reset Clock
FDG	KAI−11002 Fast Dump Gate
V3RD	KAI−11002 V2 Third Level Control Signal
V_SHUTTER	Electronic Shutter Control Signal
SHP	AD9845 Sample CCD Reset Level
SHD	AD9845 Sample CCD Data Level
DATACLK	AD9845 A/D Convert Clock
PBLK	AD9845 Pixel Blanking
CLPOB	AD9845 Black Level Clamp
CLPDM	AD9845 Dc Restore Input Clamp
VD	AD9845 Optional Vertical Drive Sync
HD	AD9845 Optional Horizontal Drive Sync
PIX	PCI−1424 Frame Grabber Pixel Rate Synchronization
FRAME	PCI−1424 Frame Grabber Frame Rate Synchronization
LINE	PCI−1424 Frame Grabber Line Rate Synchronization
CH1_SLOAD	Serial Load Enable, Ch1 AD9845 AFE
CH2_SLOAD	Serial Load Enable, Ch2 AD9845 AFE
SLOAD	Serial Load Enable, Delay Line IC's

Table 3. OUTPUTS

Symbol	Description
SCLOCK	Serial Clock (AD9845, Delay Line IC's)
SDATA	Serial Data (AD9845, Delay Line IC's)
SERIAL_ENA	Tri−State Control Of PLD/External Enable Of Serial Interface
INTEGRATE	High During CCD Integration Time

KAI−11002 TIMING CONDITIONS

Table 4. SYSTEM TIMING CONDITIONS

Description	Symbol	Time	Notes
System Clock Period	Tsys	16.67 ns	60 MHz system clock
Unit integration time	Uint	1 ms	
Power stable delay	Tpwr	30 ms	Typical
Default Serial Load Time	Tsload	112.5 μs	Typical
Integration Time	Tint		Operating mode dependent

Table 5. CCD TIMING CONDITIONS

Description	Symbol	Time	Pixel Counts	Notes
H1, H2, RESET period	Tpix	33.33 ns	1	30 MHz clocking of H1, H2, RESET
Photodiode Transfer setup	T3P	25 μs	750	
Photodiode Transfer Time	TV3rd	12 μs	360	
Photodiode Readout delay	T3D	25 μs	750	
Diode Transfer delay	Tdd	50 μs	1500	
VCCD Delay	Tvd	0.13 μs	4	
VCCD Transfer Time	TVCCD	10 μs	300	
HCCD Delay	Thd	10 μs	300	
Vertical Transfer period	Vperiod	20.13 μs	604	Vperiod = Tvd + TVCCD + Thd
Shutter Pulse Time	Ts	5 μs	150	
Shutter Pulse Delay	Tsd	2 μs	60	
Single Output Pixels per line	PIX_X1		4200	4080 CCD pixels plus 120 overclock
Dual Output Pixels per line	PIX_X2		2144	2040 CCD pixels plus 104 overclock
Lines per frame	PIX_Y		2736	2720 CCD lines plus 16 overclock
RESET clock pulse width	Tr	5 ns		Tr is set by hardware on imager board
Fast Dump Flush Time	Tflush	50 ms		
Fast Dump Flush Period	Tvflush	17.06 μs	512	50% duty cycle vertical clocks

Table 6. AFE TIMING CONDITIONS

Description	Symbol	Time	Pixel Counts	Notes
SHP,SHD,DATACLK period	Tpix	33.3 ns	1	30 MHz clocking of SHP,SHD,DATACLK
SHP pulse width	Tshp	7.5 ns		Tshp is set by hardware on timing board
SHD pulse width	Tshd	7.5 ns		Tshd is set by hardware on timing board
CLPOB1 line start	CLPOB1_ls		2	Line counter, CLPOB modes 1,2 only

Table 6. AFE TIMING CONDITIONS

Description	Symbol	Time	Pixel Counts	Notes
CLPOB1 line end	CLPOB1_le		10	Line counter, CLPOB modes 1,2 only
CLPOB1 start pixel 1 output	CLPOB1_ps1		100	Horizontal counter, CLPOB modes 1,2 only
CLPOB1 end pixel 1 output	CLPOB1_pe1		4000	Horizontal counter, CLPOB modes 1,2 only
CLPOB2 start pixel 1 output	CLPOB2_ps1		4161	Horizontal counter, CLPOB modes 0,2 only
CLPOB2 end pixel 1 output	CLPOB2_pe1		4190	Horizontal counter, CLPOB modes 0,2 only
CLPDM start pixel 1 output	CLPDM_ps1		4131	Horizontal counter
CLPDM end pixel 1 output	CLPDM_pe1		4156	Horizontal counter
CLPOB1 start pixel 2 output	CLPOB1_ps2		100	Horizontal counter, CLPOB modes 1,2 only
CLPOB1 end pixel 2 output	CLPOB1_pe2		1800	Horizontal counter, CLPOB modes 1,2 only
CLPOB2 start pixel 2 output	CLPOB2_ps2		2105	Horizontal counter, CLPOB modes 0,2 only
CLPOB2 end pixel 2 output	CLPOB2_pe2		2134	Horizontal counter, CLPOB modes 0,2 only
CLPDM start pixel 2 output	CLPDM_ps2		2075	Horizontal counter
CLPDM end pixel 2 output	CLPDM_pe2		2100	Horizontal counter
PBLK start pixel	PBLK_ps		1	Vertical transfer counter
PBLK end pixel	PBLK_pe		580	Vertical transfer counter

Table 7. PCI−1424 TIMING CONDITIONS

Description	Symbol	Time	Pixel Counts	Notes
PIX period	Tpix	33.3 ns	1	30 MHz clocking of PIX sync signal

MODES OF OPERATION

The following modes of operation are available to the user.

Output Modes

The output mode is selected by setting the JMP0, JMP1 and JMP2 inputs to the appropriate level.

Table 8. OUTPUT MODE JUMPER SETTINGS

JMP2 (Binning)	JMP1 (OPMODE)	JMP0 (Output)	Output Mode
LOW	LOW	LOW	Dual Output, Free−Running, No Binning (2144 x 2736 x 2 Out)
LOW	LOW	HIGH	Single Output, Free−Running, No Binning (4200 x 2736 x 1 Out)
LOW	HIGH	LOW	Dual Output, Single Capture, No Binning (2144 x 2736 x 2 Out)
LOW	HIGH	HIGH	Single Output, Single Capture, No Binning (4200 x 2736 x 1 Out)
HIGH	LOW	LOW	Dual Output, Free−Running, 2x2 Binning (1072 x 1368 x 2 Out)
HIGH	LOW	HIGH	Single Output, Free−Running, 2x2 Binning (2100 x 1368 x 1 Out)
HIGH	HIGH	LOW	Dual Output, Single Capture, 2x2 Binning (1072 x 1368 x 2 Out)
HIGH	HIGH	HIGH	Single Output, Single Capture, 2x2 Binning (2100 x 1368 x 1 Out)

Single Output Mode

The KAI−11002 device features a split horizontal register and two output amplifiers. Setting the JMP0 jumper to the high position causes all of the CCD pixels to be clocked out the CCD's left output amplifier. See KAI−11002 device specification (References) for details.

Dual Output Mode

The KAI−11002 device features a split horizontal register and two output amplifiers. Setting the JMP0 jumper to the low position causes each half of the horizontal register to be clocked out in opposite directions, increasing the frame rate by approximately 2. See KAI−11002 device specification for details (References).

Binning Mode (2x2)

Utilizing the JMP2 input, the timing can be set to accumulate 2 lines of charge in the horizontal register before clocking the charge down the horizontal register; 2 registers of charge are then accumulated in the output structure floating diffusion before clocking the charge out of the device. In this way, the total charge of a 2x2 pixel area is summed into one measurement.

Free−Running Mode

In free−running operating mode charge is transferred from the photodiodes and then read out of the device in a continuous manner. See Figure 2.

Single Capture Mode

In single capture operating mode an external trigger is required to initiate the capture sequence. Upon the rising edge of the DIO0 control line the electronic shutter is activated. Then charge is allowed to accumulate in the photodiodes for a period of time set by the integration time control lines D[5..1]. In the last 50 ms of integration time residual charge is fast dumped from the vertical CCDs, and then the charge is transferred from the photodiodes and read out of the device. See Figure 3.

Multi−Frame Integration Modes

In free−running operating mode, integration times of more than a frame time can be achieved by varying the time between transfer of charge from the photodiodes. In Multi−frame Integration Mode, the Integration time can be set from 1X to 8X the frame time via the DIO interface (See Table 12 and Table 13).

Electronic Shutter Modes

Integration times less than one frame time can be achieved by electronic shuttering of the device. In Electronic Shutter Mode, the integration time can be set from 1X to 1/8X frame time via the DIO interface (See Electronic Shutter State).

Black Clamp Modes

One of the features of the AD9845 AFE chip is an optical black clamp. The black clamp (CLPOB) is asserted during the CCD's dark pixels and is used to remove residual offsets in the signal chain, and to track low frequency variations in the CCD's black level. Several options for operating this black clamp are provided and are controlled by the digital inputs D[13..12]. The default CLPOB mode is 0.

Table 9. BLACK CLAMP MODES

CLPOB Mode DIO[13..12]	Black Clamp Operation	Notes
0	Several dark pixels at the end of each line	Default Mode
1	Several dark lines at the beginning of each frame	
2	Several dark lines per frame, and several dark pixels per line	
3	Off, no black clamp, CLPOB always held high	

PIXEL RATE CLOCKS GENERATION

The pixel rate clocks are derived from the system clock. They operate at 1/2 the frequency of the system clock. The PIXEL_CLK signal is generated from the rising edge of the system clock. The DELAYED_PIX_CLK signal is generated from the falling edge of the system clock. By utilizing both edges of the system clock, 4 start positions for the pixel rate clocks are achieved.

1. The PIXEL_CLK signal
2. The DELAYED_PIX_CLK signal occurs 25% later than the PIXEL_CLK signal
3. The inverse of the PIXEL_CLK signal occurs 50% later than the PIXEL_CLK signal
4. The inverse of the DELAYED_PIX_CLK signal occurs 75% later than the PIXEL_CLK signal

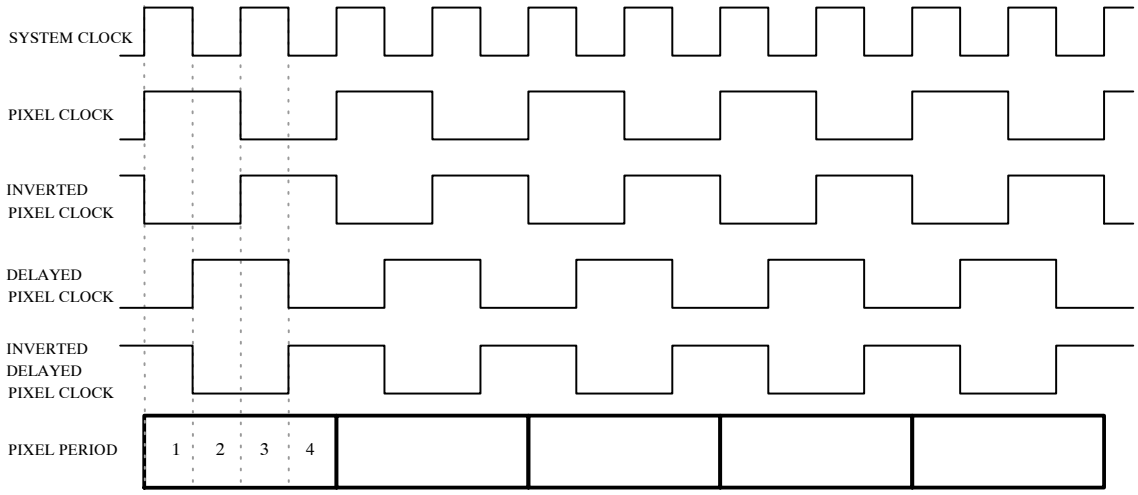

Figure 1. Pixel Clock Generation Timing

One of these four signals is chosen to be the input signal source for a particular pixel rate signal, and then the position of the signal is optimized using a DS1020 programmable delay line IC.

TIMING GENERATOR STATE MACHINE DESCRIPTION

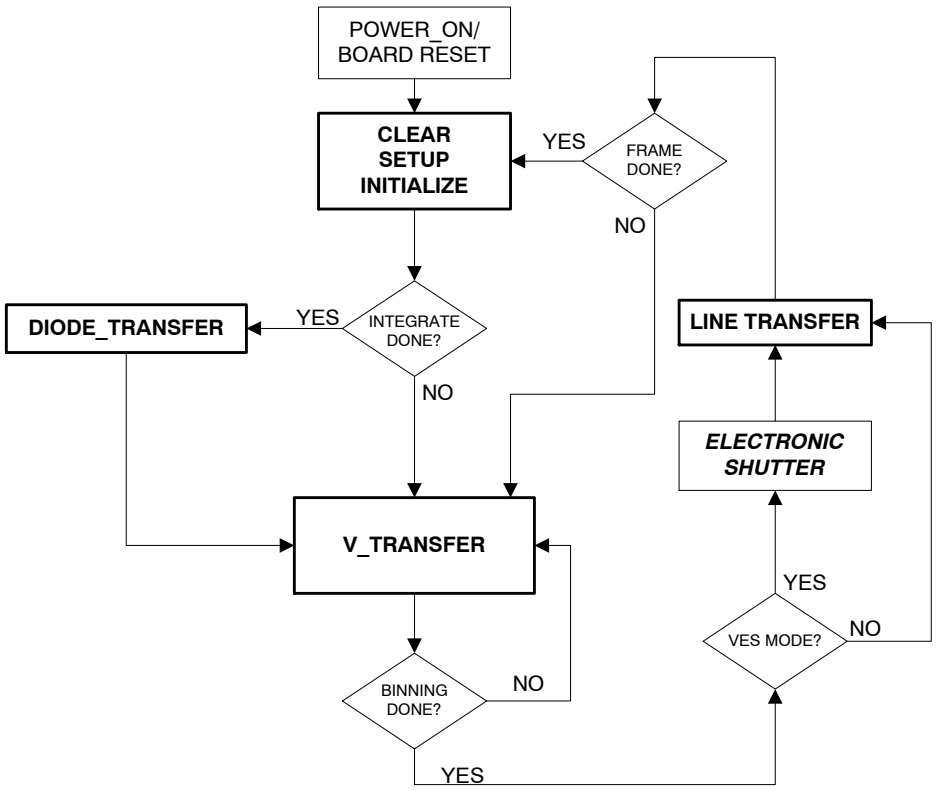

Figure 2. Timing Generator State Machine (Free−Running Mode)

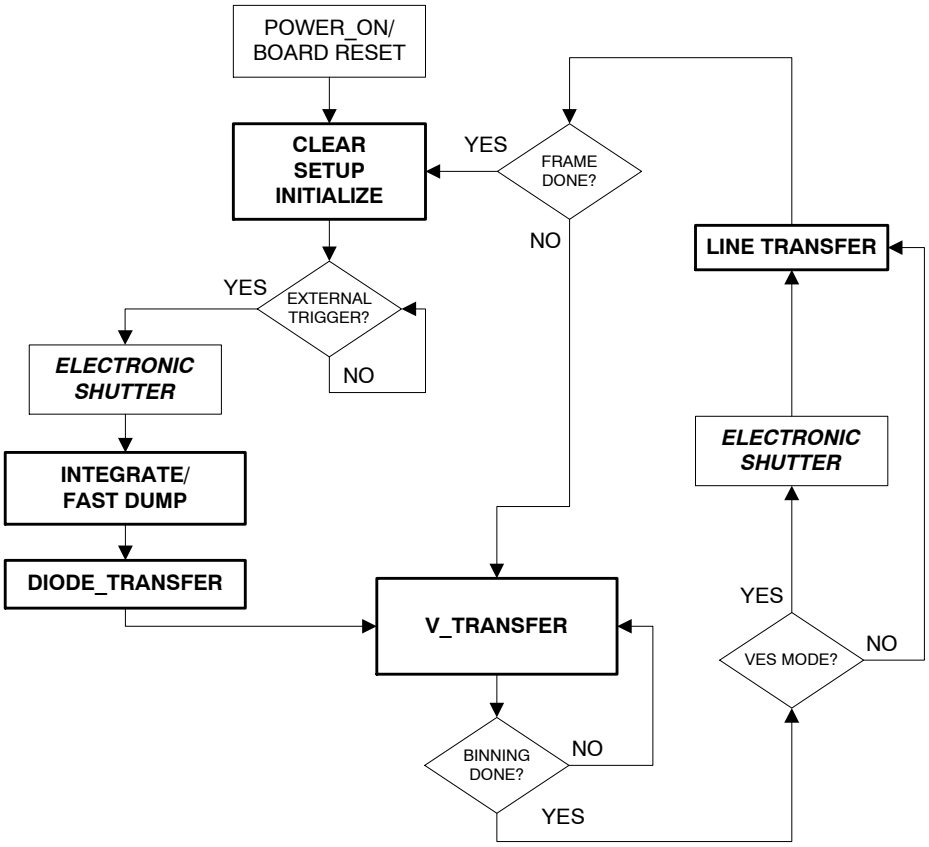

Figure 3. Timing Generator State Machine (Single Capture Mode)

Power−On / Board Reset Initialize State

When the board is powered up or the Board Reset button is pressed, the Altera PLD is internally reset. When this occurs, state machines in the PLD will first serially load the initial default values into the ten delay line IC's on the board, and then serially load the initial default values into the AFE registers. Upon completion of the serial load of the AFE, the board will be ready to proceed according to the output mode selected.

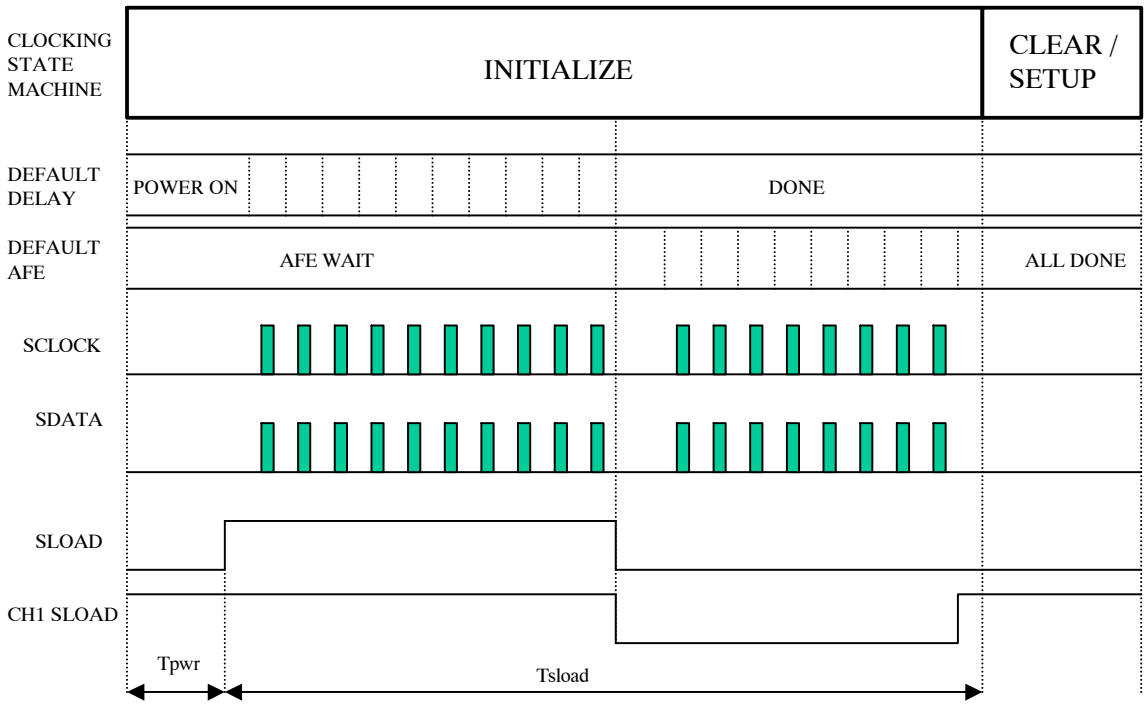

Figure 4. Power−On Initialization Timing

Delay Register Initialization

The Programmable Silicon Delay Lines allow the Horizontal Clocks, Reset Clock, Clamp, Sample, and Data Clock signals to be adjusted within the sub−pixel timing. On power−up or board reset, the delay lines are programmed with values stored in the Altera device. These values are chosen to conform to the timing requirements of the CCD image sensor and to achieve optimum device performance (See the KAI−11002 device specification for details). The delay values shown in Table 10 are typical values, and may vary on an individual Evaluation Board set.

For programming purposes, the silicon delay lines are cascaded, i.e., the serial output pin of device 1 is tied to the serial input pin of device 2 and so on. Therefore, when making an adjustment to one or more delay lines, all the delay lines must be reprogrammed. The total number of serial bits must be eight times the number of units daisy−chained and each group of 8 bits must be sent in MSB−to−LSB order (See References). The total delay on each output signal is calculated as:

Delay = 10.0 + 0.25 * [Delay Code] (ns)

Refer to the Dallas Semiconductor DS1020 Programmable Silicon Delay Line Specification Sheet (References) for details.

Table 10. DEFAULT DELAY IC PROGRAMMING

Delay IC Programming Order	Delay IC Output Signal	Delay IC Input Signal Source	Delay Code (Typical)	Delay (ns) (Typical)
1	AD9845 DATACLK	PIXEL CLK	32	18.0
2	CH2 AD9845 SHP	PIXEL CLK	24	16.0
3	CH1 AD9845 SHP	PIXEL CLK	24	16.0
4	CH2 AD9845 SHD	INVERTED PIXEL CLK	20	15.0
5	CH1 AD9845 SHD	INVERTED PIXEL CLK	20	15.0
6	H1 CLOCK	INVERTED PIXEL CLK	0	10.0
7	H1BR CLOCK	INVERTED PIXEL CLK	0	10.0
8	H2 CLOCK	PIXEL CLK	0	10.0
9	H2BR CLOCK	PIXEL CLK	0	10.0
10	RESET CLOCK	INVERTED PIXEL CLK	0	12.0

On power up or board−reset, the AFE registers are programmed to the default levels shown in Table 11. See the AD9845 specifications sheet (References) for details.

Table 11. DEFAULT AD9845 AFE REGISTER PROGRAMMING

Register	Description	Value	Notes
0	Operation	128	
1	VGA Gain	206	Corresponds to a VGA stage gain of 5.23 dB
2	Clamp	96	The output of the AD9845 will be clamped to code 96 during the CLPOB period
3	Control	10	PXGA gain registers enabled
4	PXGA gain0	43	Corresponds to a CDS stage gain of 0 dB
5	PXGA gain1	43	Corresponds to a CDS stage gain of 0 dB
6	PXGA gain2	43	Corresponds to a CDS stage gain of 0 dB
7	PXGA gain3	43	Corresponds to a CDS stage gain of 0 dB

Clear / Setup State

The timing generator state machine is free running. It cycles through the states depending on the jumper settings and DIO inputs, and then returns back to the clear state to begin the next frame. At the beginning of each frame, the internal PLD counters are reset.

DIODE TRANSFER State

During the DIODE_TRANSFER state, the V2_CLK is brought to the high level and charge is transported from the photodiodes to the Vertical CCD's.

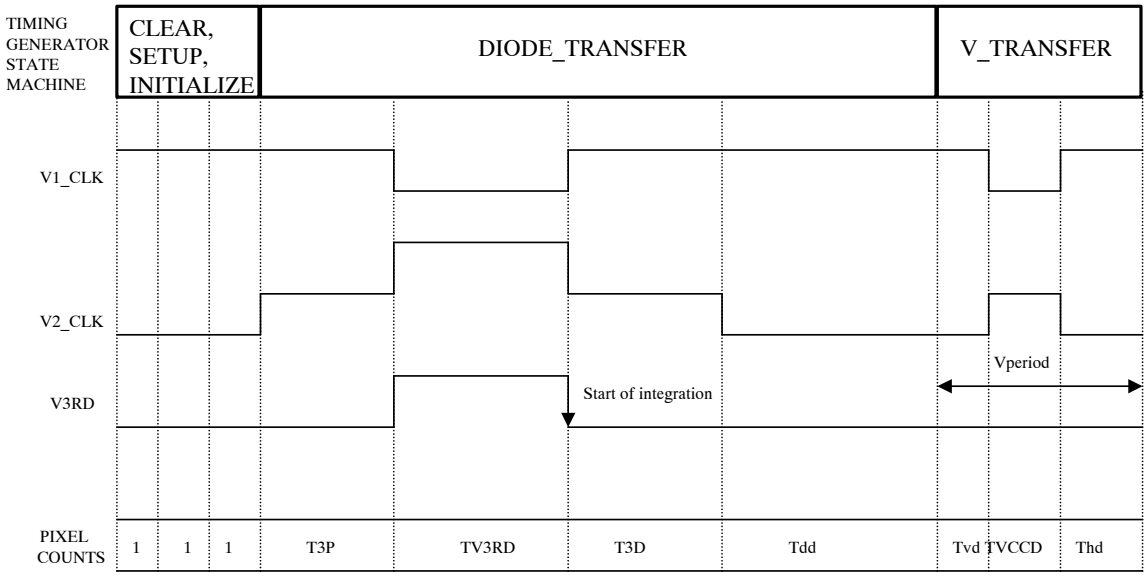

Figure 5. Diode Transfer Timing

In free−running operating mode, the integration time can be adjusted to multiple frame times by prolonging the time between photodiode charge transfer using the input control lines D[11..9]. The effective integration time is the time between the transfer of charge from the photodiodes. The default Integration Mode is INT_MODE = 0, a single frame between photodiode transfer.

In Single Output Mode, multiple frame integration time is equal to:

$$(T3P + TV3rd + T3D + Tdd) + [(Vperiod + (PIX\_X1 * Tpix)) * PIX\_Y] * (INT\_MODE + 1)$$

Table 12. SINGLE OUTPUT, FREE−RUNNING MULTI−FRAME INTEGRATION TIMES

INT_MODE DIO[11..9]	Integration Time (Frames)	Integration Time (ms)	Frame Rate (Fps)	Notes
0	1	438.19	2.28	Default
1	2	876.27	1.14	
2	3	1314.36	0.76	
3	4	1752.44	0.57	
4	5	2190.52	0.46	
5	6	2628.6	0.38	
6	7	3066.68	0.33	
7	8	3504.76	0.29	

In Dual Output Mode, multiple frame integration time is equal to:

$$(T3P + TV3rd + T3D + Tdd) + [(Vperiod + PIX\_X2 * Tpix) * PIX\_Y] * (INT\_MODE + 1)$$

Table 13. DUAL OUTPUT, FREE−RUNNING, MULTI−FRAME INTEGRATION TIMES

INT_MODE DIO[11..9]	Integration Time (Frames)	Integration Time (ms)	Frame Rate (Fps)	Notes
0	1	250.7	3.99	Default
1	2	501.3	1.99	
2	3	751.89	1.33	
3	4	1002.48	1.00	
4	5	1253.08	0.80	
5	6	1503.67	0.67	
6	7	1754.26	0.57	
7	8	2004.85	0.50	

V_TRANSFER State

During the V_TRANSFER state, each line (row) of charge is transported towards the horizontal CCD register using the Vertical clocks. A vertical transfer counter in the PLD is used to determine when the vertical clocks are forced high and low and when the vertical transfer time and horizontal delay time (Thd) are completed.

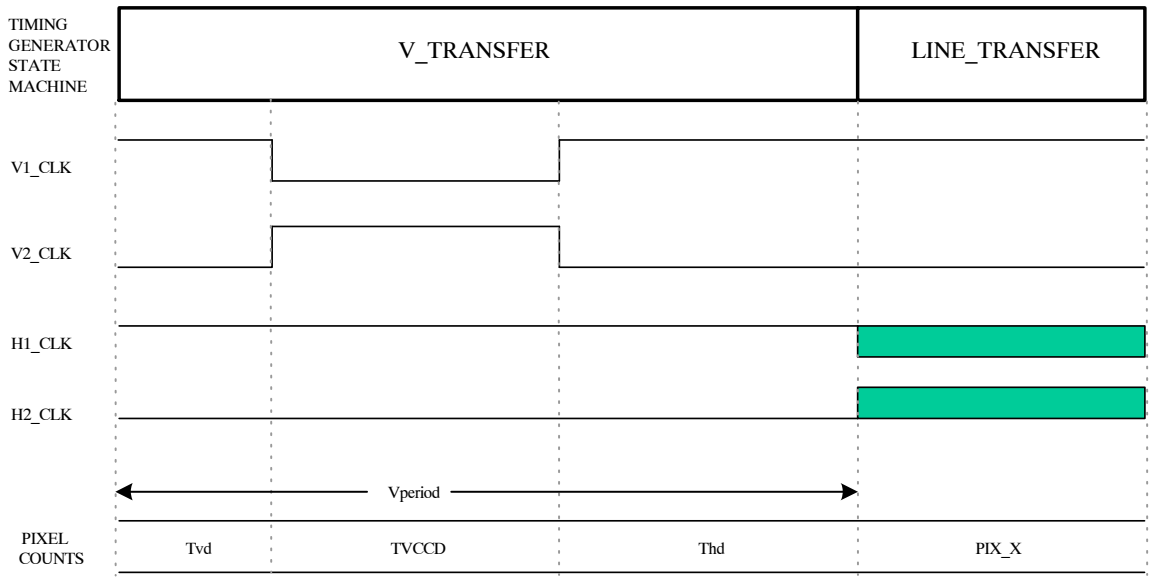

Figure 6. Vertical Transfer Timing

Binning Mode Option

When operating in 2x2 binning mode, two lines of charge are transferred into the CCD Horizontal Register A and allowed to accumulate before being clocked towards the output (Figure 7).

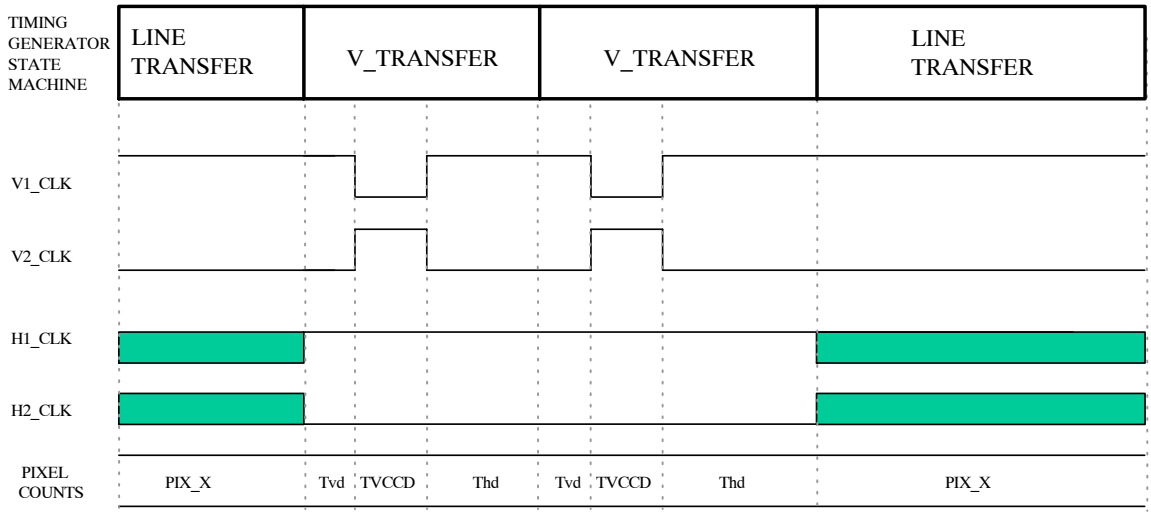

Figure 7. Vertical Transfer Timing − 2x2 Binning Mode

Electronic Shutter State

The integration time can be adjusted to be smaller than one frame time by electronic shuttering of the device. Using the input control lines D[8..6], the line on which the electronic shutter will occur can be selected. The effective integration time is then the time between when the electronic shutter occurred and the next transfer of charge from the photodiodes. The default Electronic Shutter Mode is 0, no electronic shutter.

In Single Output mode, Electronic Shutter Mode integration time is equal to:

$$Tsd + \{[(PIX\_X1 * Tpix) + Vperiod] * (PIX\_Y - VES\_LINE)\} - Vperiod + T3P + TV3rd$$

Table 14. SINGLE OUTPUT ELECTRONIC SHUTTER INTEGRATION TIMES

VES MODE DIO[8..6]	VES_LINE #	Integration Time (Frames)	Integration Time (ms)	Notes
0		1	438.19	Default
1	342	0.875	383.34	
2	684	0.75	328.58	
3	1026	0.625	273.82	
4	1368	0.5	219.06	
5	1710	0.375	164.3	
6	2052	0.25	109.54	
7	2394	0.125	54.78	

In Dual Output mode, Electronic Shutter Mode integration time is equal to:

$$Tsd + \{[(PIX\_X2 * Tpix) + Vperiod] * (PIX\_Y - VES\_LINE)\} - Vperiod + T3P + TV3rd$$

Table 15. DUAL OUTPUT ELECTRONIC SHUTTER INTEGRATION TIMES

VES MODE DIO[8..6]	VES_LINE #	Integration Time (Frames)	Integration Time (ms)	Notes
0		1	250.7	Default
1	342	0.875	219.29	
2	684	0.75	187.96	
3	1026	0.625	156.64	
4	1368	0.5	125.31	
5	1710	0.375	93.99	
6	2052	0.25	62.67	
7	2394	0.125	31.34	

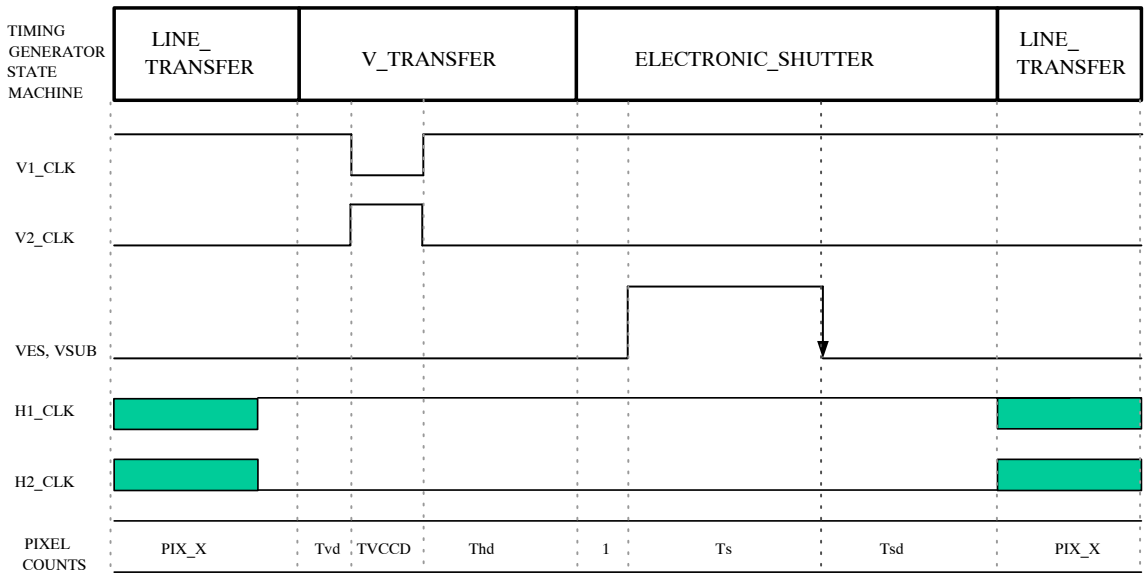

Figure 8. Electronic Shutter Timing

LINE_TRANSFER State

During the LINE_TRANSFER state, charge is transported to the CCD output structure pixel by pixel. A line transfer counter in the PLD is used to keep track of how many pixels have been transported, and to synchronize the AD9845 timing signals and the PCI−1424 timing signals with the appropriate pixels (dark pixels for black clamping, for example).

At the end of each line transfer, the Line counter is incremented. If all of the lines have been clocked out of the CCD, the state machine goes to the CLEAR / SETUP state; if not, the state machine goes to the V_TRANSFER state to transfer another line of charge into the horizontal register.

In Single Output Mode, the H1BR and H2BR clocks are identical to the H1 and H2 clocks, respectively. In Dual Output Mode, the H1BR and H2BR clocks are switched to become identical with H2 and H1, respectively. In this way, the right half of the Horizontal register is clocked in the opposite direction, to the VOUTR output of the CCD. See KAI−11002 Device Performance Specifications (References) for details.

In 2x2 Binning Mode, two registers of charge, each containing two pixels, are summed in the CCD's floating diffusion before being clocked out of the device. The 2x2 Binning Mode can be selected using output control jumpers (See Table 8). When using Binning Mode, the pixel rate delays may have to be re−adjusted and re−synchronized to achieve optimal performance.

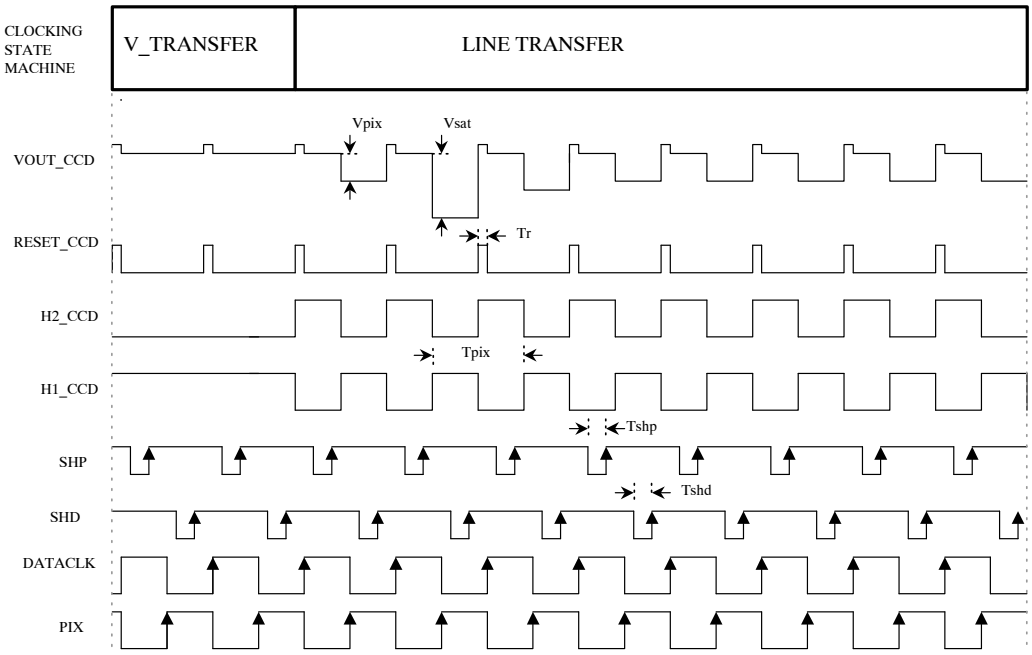

Figure 9. Horizontal Timing − Line Transfer

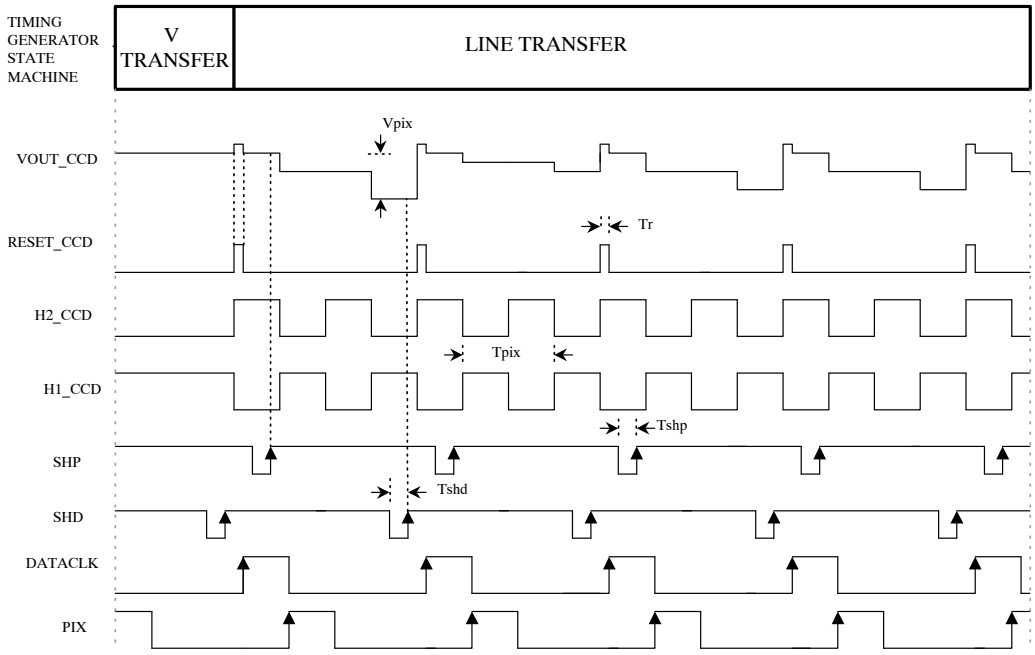

Figure 10. Horizontal Timing – 2x2 Binning Mode Line Transfer

Single Capture Operating Mode with External Trigger

The timing for the Single Capture operating mode sequence of states is shown in Figure 11:

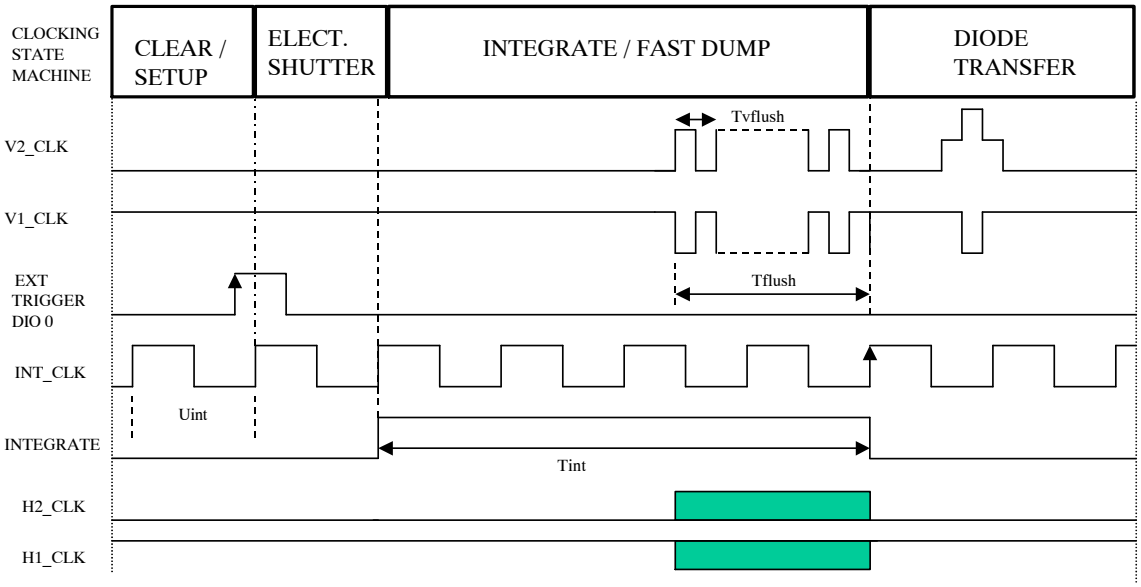

Figure 11. Single Capture with External Trigger Timing

Table 16. SINGLE CAPTURE INTEGRATION TIME OPTIONS

INT_MODE DIO[5..1]	Integration Time (ms)	Notes	INT_MODE DIO[5..1]	Integration Time (ms)	Notes
0	50	Default	16	250	
1	60		17	300	
2	70		18	350	
3	80		19	400	
4	90		20	450	
5	100		21	500	
6	110		22	550	
7	120		23	600	
8	130		24	650	
9	140		25	700	
10	150		26	750	
11	160		27	800	
12	170		28	850	
13	180		29	900	
14	190		30	950	
15	200		31	1000	

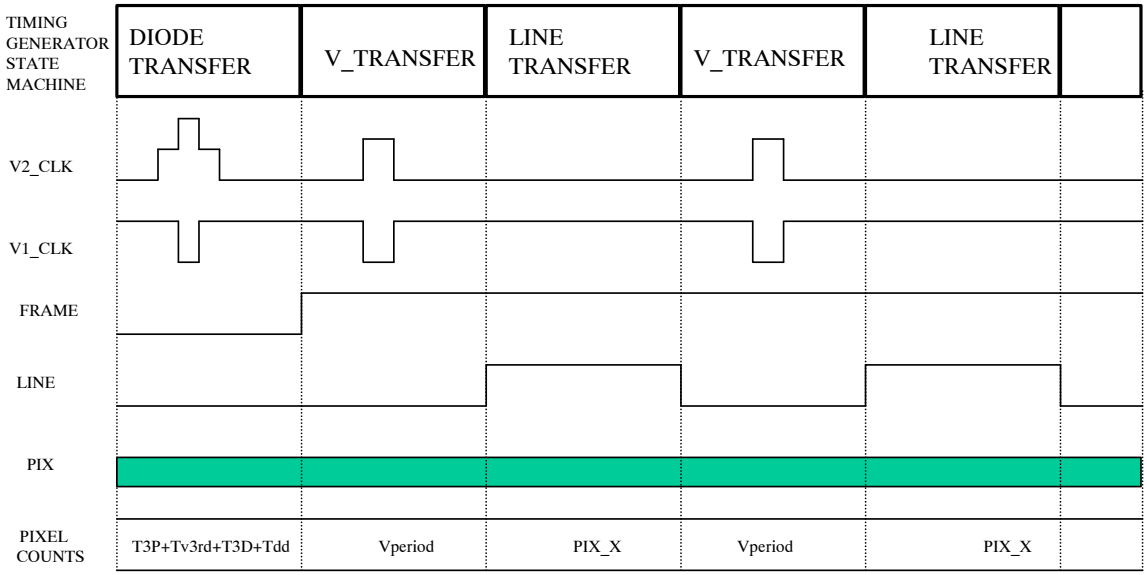

Figure 12. PCI−1424 Frame Grabber Timing

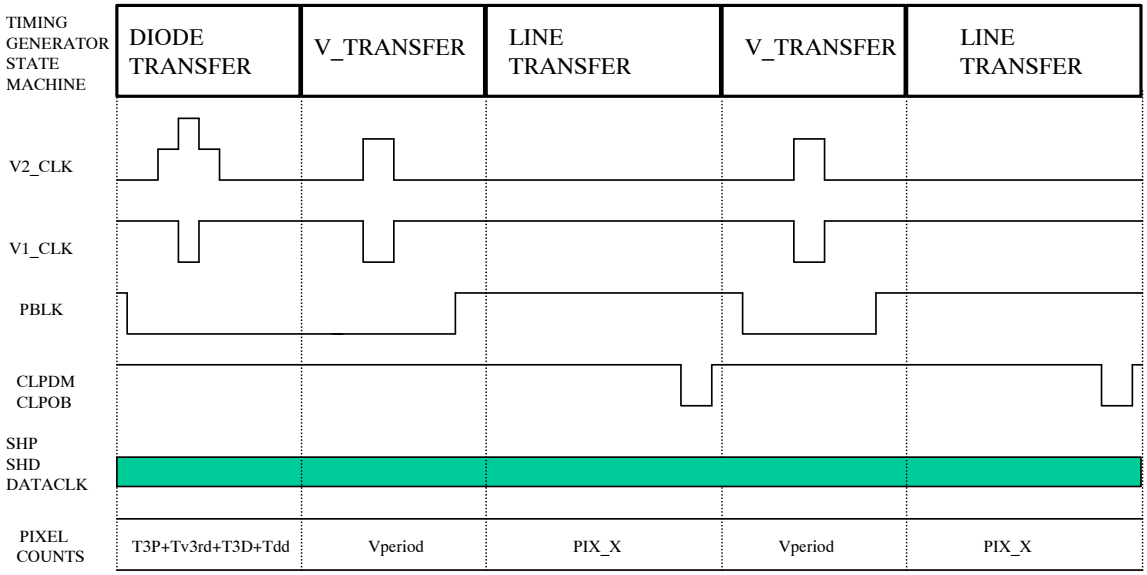

Figure 13. AD9845 Timing

Warnings and Advisories

When programming the Timing Board, the Imager Board must be disconnected from the Timing Board before power is applied. If the Imager Board is connected to the Timing Board during the reprogramming of the Altera PLD, damage to the Imager Board will occur.

Purchasers of an Evaluation Board Kit may, at their discretion, make changes to the Timing Generator Board firmware. ON Semiconductor can only support firmware developed by, and supplied by, ON Semiconductor. Changes to the firmware are at the risk of the customer.

Ordering Information

Please address all inquiries and purchase orders to:

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E−mail: info@truesenseimaging.com

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

References

- KAI−11002 Device Specification
- KAI−11002 Imager Board User Manual
- KAI−11002 Imager Board Schematic
- AD984X Timing Generator Board User Manual
- AD984X Timing Generator Board Schematic
- Analog Devices AD9845 Product Data Sheet (28 and 30 MHz operation)

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