

TLP550

- Digital Logic Isolation
- Line Receiver Feedback Control
- Power Supply Control
- Switching Power Supply
- Transistor Inverter

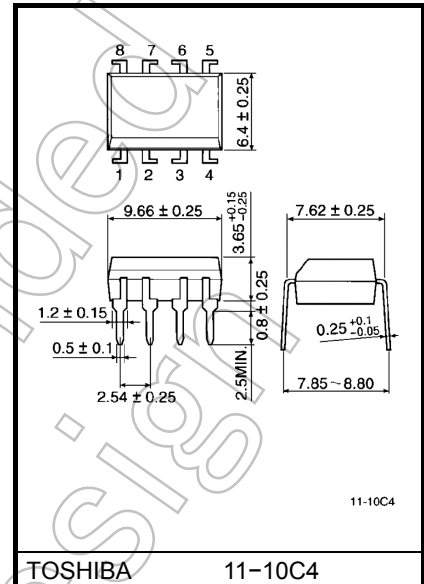
Unit: mm

TLP550 consists of a high emitting diode and a one chip photo diode-transistor.

TLP550 has no base connection, and is suitable for application at noisy environmental condition.

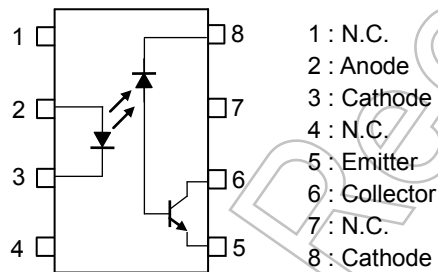
This unit is 8-lead DIP package.

- Isolation voltage : 2500 Vrms (min)
- Propagation delay time (t_{pHL} / t_{pLH}):
 $t_{pHL} = 0.5\mu s$ (typ.), $t_{pLH} = 0.6\mu s$ (typ.)
 $(R_L = 1.9 k\Omega)$
- TTL compatible
- UL recognized: UL1577, file No. E67349

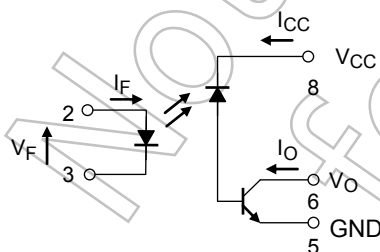


Weight: 0.54 g (typ.)

Pin Configuration (top view)



Schematic



Start of commercial production
1981/09

Current Transfer Ratio

Classification	Current Transfer Ratio (%) (I _C /I _F)		Marking of Classification
	Min	Max	
(None)	10	—	Blank, O, Y
Rank O	19	—	O
Rank Y	35	—	Y

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
LED	Forward current (Note 1)	I _F	25	mA
	Pulse forward current (Note 2)	I _{FP}	50	mA
	Peak transient forward current (Note 3)	I _{FPT}	1	A
	Reverse voltage	V _R	5	V
	Diode power dissipation (Note 4)	P _D	45	mW
Detector	Output current	I _O	8	mA
	Peak output current	I _{OP}	16	mA
	Supply voltage	V _{CC}	-0.5~15	V
	Output voltage	V _O	-0.5~15	V
	Output power dissipation (Note 5)	P _O	100	mW
Operating temperature range		T _{opr}	-55~100	°C
Storage temperature range		T _{stg}	-55~125	°C
Lead solder temperature (10s)		T _{sol}	260	°C
Isolation voltage (AC, 1minute, R.H. = 40 to 60%) (Note 6)		BV _S	2500	V _{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

(Note 1) Derate 0.8mA above 70°C.

(Note 2) 50% duty cycle, 1ms pulse width.

Derate 1.6mA / °C above 70°C.

(Note 3) Pulse width 1μs, 300pps.

(Note 4) Derate 0.9mW / °C above 70°C.

(Note 5) Derate 2mW / °C above 70°C.

Electrical Characteristics (Ta = 25°C)

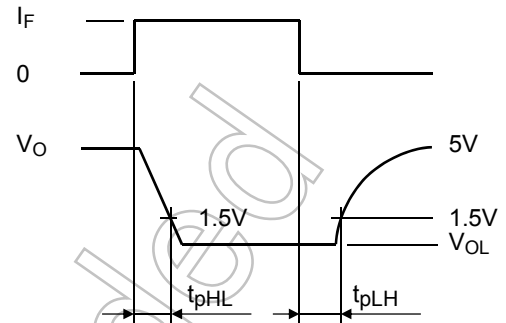
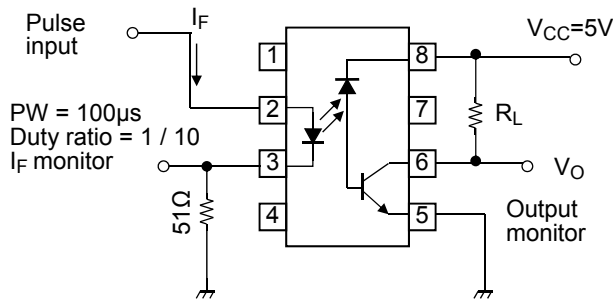
Characteristic		Symbol	Test condition	Min	Typ.	Max	Unit	
LED	Forward voltage	V_F	$I_F = 16 \text{ mA}$	1.45	1.65	1.85	V	
	Forward voltage temperature coefficient	$\Delta V_F / \Delta T_a$	$I_F = 16 \text{ mA}$	—	-2	—	mV / °C	
	Reverse current	I_R	$V_R = 5 \text{ V}$	—	—	10	μA	
	Capacitance between terminal	C_T	$V_F = 0, f = 1 \text{ MHz}$	—	60	—	pF	
Detector	High level output current	$I_{OH(1)}$	$I_F = 0 \text{ mA}, V_{CC} = V_O = 5.5 \text{ V}$	—	3	500	nA	
		$I_{OH(2)}$	$I_F = 0 \text{ mA}, V_{CC} = V_O = 15 \text{ V}$	—	—	5	μA	
		I_{OH}	$I_F = 0 \text{ mA}, V_{CC} = V_O = 15 \text{ V}$ $T_a = 70^\circ\text{C}$	—	—	50	μA	
	High level supply voltage	I_{CCH}	$I_F = 0 \text{ mA}, V_{CC} = 15 \text{ V}$	—	0.01	1	μA	
Coupled	Current transfer ratio	I_O / I_F	$I_F = 16 \text{ mA}$ $V_{CC} = 4.5 \text{ V}$ $V_O = 0.4 \text{ V}$	$T_a = 25^\circ\text{C}$	10	40	—	%
				Rank: O	19	40	—	
				Rank: Y	35	50	—	
				$T_a = 0\sim 70^\circ\text{C}$	5	—	—	
				Rank: O, Y	15	—	—	
Low level output voltage	V_{OL}	$I_F = 16 \text{ mA}, V_{CC} = 4.5 \text{ V}$ $I_O = 1.1 \text{ mA}$ (rank O: $I_O = 2.4 \text{ mA}$)	—	—	0.4	V		
Isolation resistance	R_S	R.H. = 40~60%, $V = 1 \text{ kV DC}$ (Note 6)	—	10^{12}	—	Ω		
Capacitance between input to output	C_S	$V = 0, f = 1 \text{ MHz}$	—	0.8	—	pF		

Switching Characteristics (Ta = 25°C)

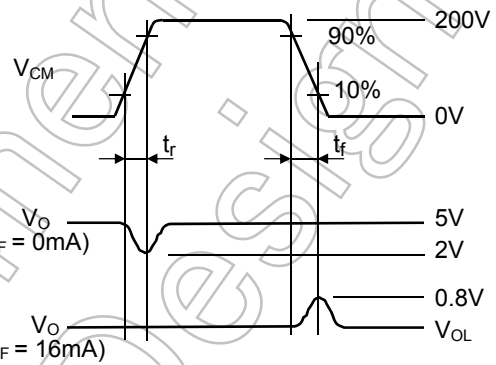
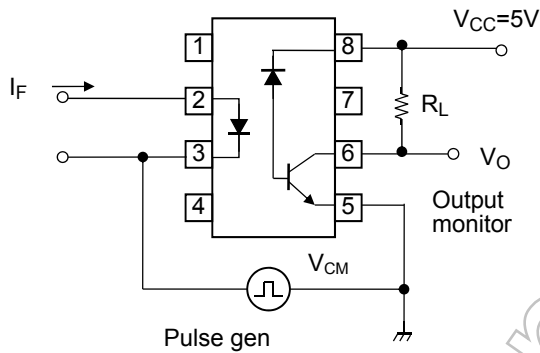
Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (H → L)	t_{pHL}	$I_F = 0 \rightarrow 16 \text{ mA}, V_{CC} = 5 \text{ V}, R_L = 4.1 \text{ k}\Omega$	—	0.3	0.8	μs
		(Note 7) Rank O: $R_L = 1.9 \text{ k}\Omega$	—	0.5	0.8	
Propagation delay time (L → H)	t_{pLH}	$I_F = 16 \rightarrow 0 \text{ mA}, V_{CC} = 5 \text{ V}, R_L = 4.1 \text{ k}\Omega$	—	1.0	2.0	μs
		(Note 7) Rank O: $R_L = 1.9 \text{ k}\Omega$	—	0.6	1.2	
Common mode transient immunity at high output level	C_{MH}	$I_F = 0 \text{ mA}, V_{CM} = 200 \text{ V}_{p-p}$ $R_L = 4.1 \text{ k}\Omega$ (rank O: $R_L = 1.9 \text{ k}\Omega$) (Note 8)	—	1500	—	V / μs
Common mode transient immunity at low output level	C_{ML}	$I_F = 16 \text{ mA}, V_{CM} = 200 \text{ V}_{p-p}$ $R_L = 4.1 \text{ k}\Omega$ (rank O: $R_L = 1.9 \text{ k}\Omega$) (Note 8)	—	-1500	—	V / μs

(Note 6) Device considered two-terminal device: Pins 1, 2, 3 and 4 shorted together and pin 5, 6, 7 and 8 shorted together.

(Note 7) Switching time test circuit.



(Note 8) Common mode transient immunity test circuit.

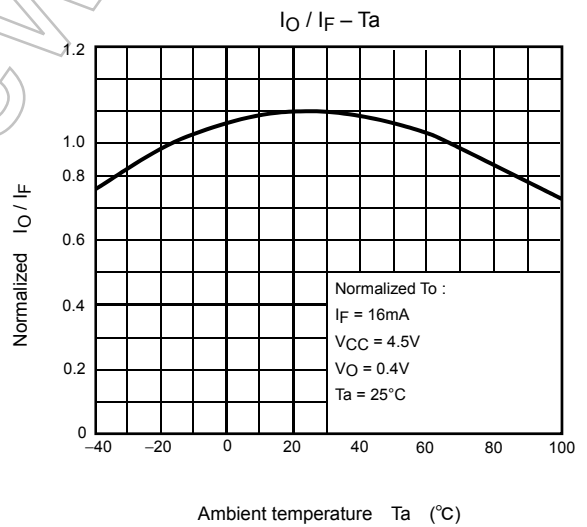
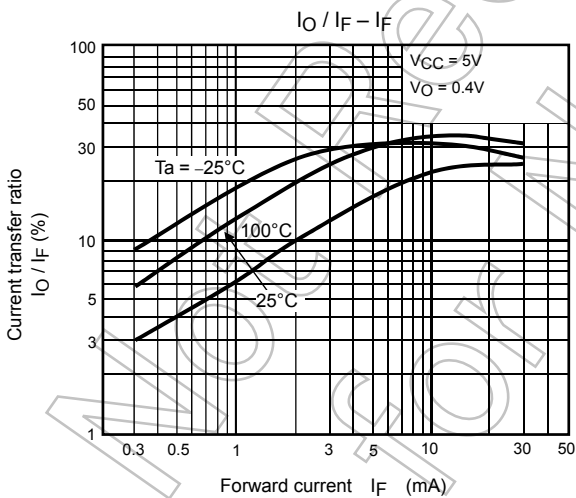
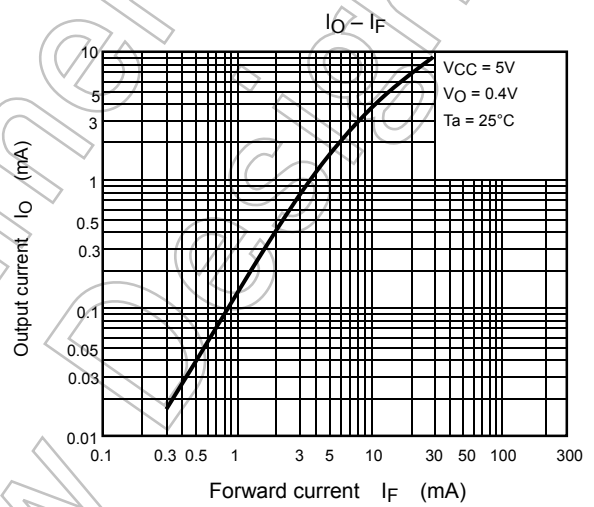
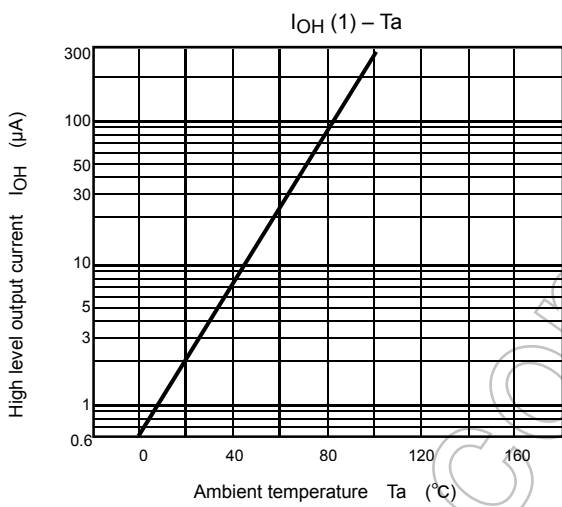
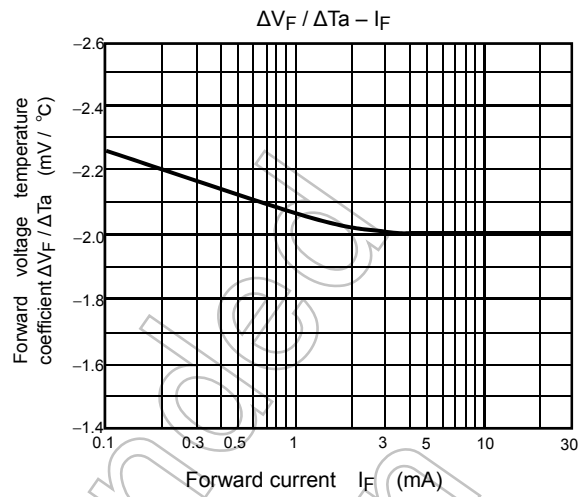
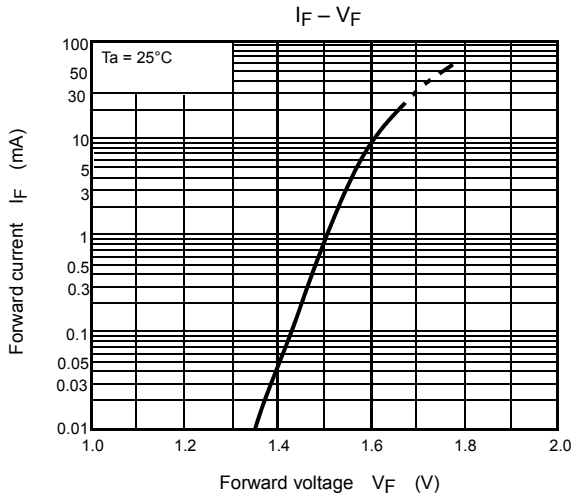


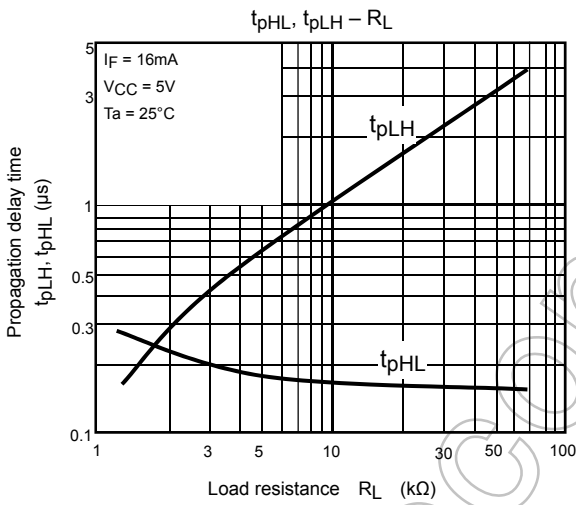
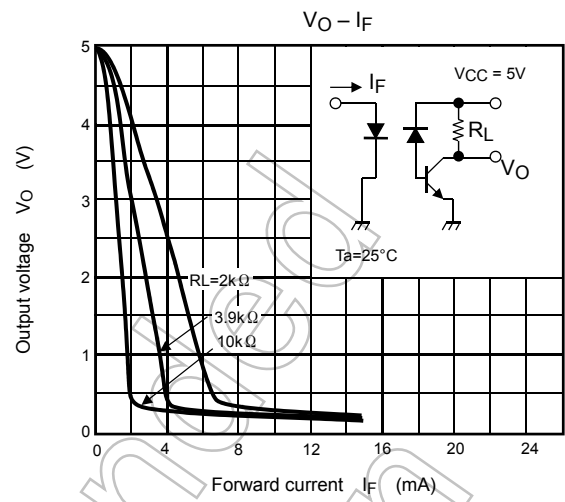
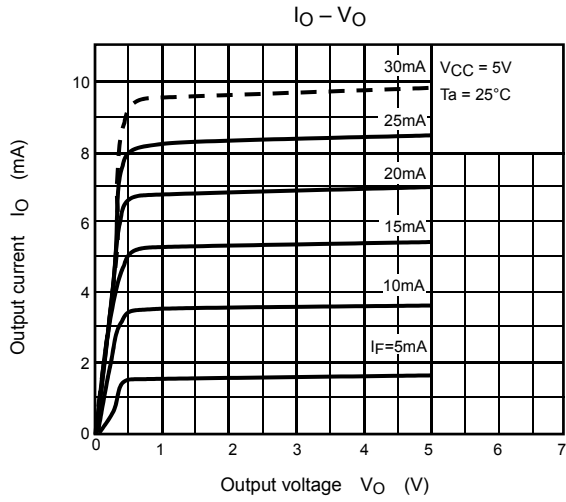
$Z_0=50\Omega$

$$CM_H = \frac{160 (V)}{t_f (\mu s)}, \quad CM_L = \frac{160 (V)}{t_f (\mu s)}$$

(Note 9) Maximum electrostatic discharge voltage for any pins: 100V (C = 200pF, R = 0)

Not Recommended for New





Not Recommended for New Design

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