

MOSFET

PowerStage 3x3

Features

- Dual N-channel OptiMOS™ MOSFET
- Enhancement mode
- Logic level (4.5V rated)
- Avalanche rated
- 100% Lead-free; RoHS compliant
- Halogen-free according to IEC61249-2-21

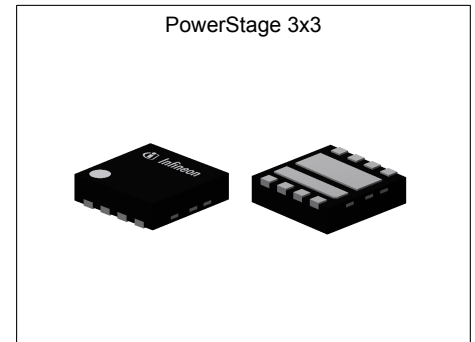
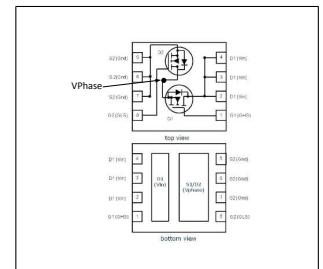


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	30	V
$R_{DS(on),max}$	9.5	m Ω
I_D	25	A
Q_{oss}	4.6	nC
$Q_G(0V..4.5V)$	4.0	nC



Type / Ordering Code	Package	Marking	Related Links
BSZ0910ND	PG-WISON-8	0910ND	-

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified, one transistor active

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	25 11.1 9.5 5.7	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}^{1)}$ $V_{GS}=4.5\text{ V}$, $T_A=25\text{ °C}^{1)}$ $V_{GS}=4.5\text{ V}$, $T_A=25\text{ °C}^{2)}$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	40	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	20	mJ	$I_D=9\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	31 1.9	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{THJA}=65\text{ °C/W}^{1)}$
Operating and storage temperature	T_j , T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	4	°C/W	-
Device on PCB, 6 cm ² cooling area ¹⁾	R_{thJA}	-	-	65	°C/W	-
Device on PCB, minimal footprint ²⁾	R_{thJA}	-	-	180	°C/W	-

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

²⁾ device mounted on a minimum pad (one layer, 70 µm thick)

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2	V	$V_{DS}=V_{GS}$, $I_D=250\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=30\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ }^\circ\text{C}$ $V_{DS}=30\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	7.7	9.5	$\text{m}\Omega$	$V_{GS}=10\text{ V}$, $I_D=9\text{ A}$ $V_{GS}=4.5\text{ V}$, $I_D=9\text{ A}$
Gate resistance ¹⁾	R_G	1.8	3.5	7	Ω	-
Transconductance	g_{fs}	-	33	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$, $I_D=9\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	590	800	pF	$V_{GS}=0\text{ V}$, $V_{DS}=15\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	170	230	pF	$V_{GS}=0\text{ V}$, $V_{DS}=15\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	21	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=15\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	6.2	-	ns	$V_{DD}=15\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=9\text{ A}$, $R_{G,ext}=6\text{ }\Omega$
Rise time	t_r	-	3.2	-	ns	$V_{DD}=15\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=9\text{ A}$, $R_{G,ext}=6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	18.5	-	ns	$V_{DD}=15\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=9\text{ A}$, $R_{G,ext}=6\text{ }\Omega$
Fall time	t_f	-	2.8	-	ns	$V_{DD}=15\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=9\text{ A}$, $R_{G,ext}=6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	1.5	-	nC	$V_{DD}=15\text{ V}$, $I_D=9\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	0.9	-	nC	$V_{DD}=15\text{ V}$, $I_D=9\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge	Q_{gd}	-	1.0	-	nC	$V_{DD}=15\text{ V}$, $I_D=9\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Switching charge	Q_{sw}	-	1.5	-	nC	$V_{DD}=15\text{ V}$, $I_D=9\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total ¹⁾	Q_g	-	4.0	5.6	nC	$V_{DD}=15\text{ V}$, $I_D=9\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	2.6	-	V	$V_{DD}=15\text{ V}$, $I_D=9\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total ¹⁾	Q_g	-	8.2	11.4	nC	$V_{DD}=15\text{ V}$, $I_D=9\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	3.4	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Output charge ¹⁾	Q_{oss}	-	4.6	-	nC	$V_{DD}=15\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	25	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	40	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.86	1.1	V	$V_{GS}=0\text{ V}, I_F=9\text{ A}, T_j=25\text{ °C}$
Reverse recovery charge ¹⁾	Q_{rr}	-	5	-	nC	$V_R=15\text{ V}, I_F=9\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

¹⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

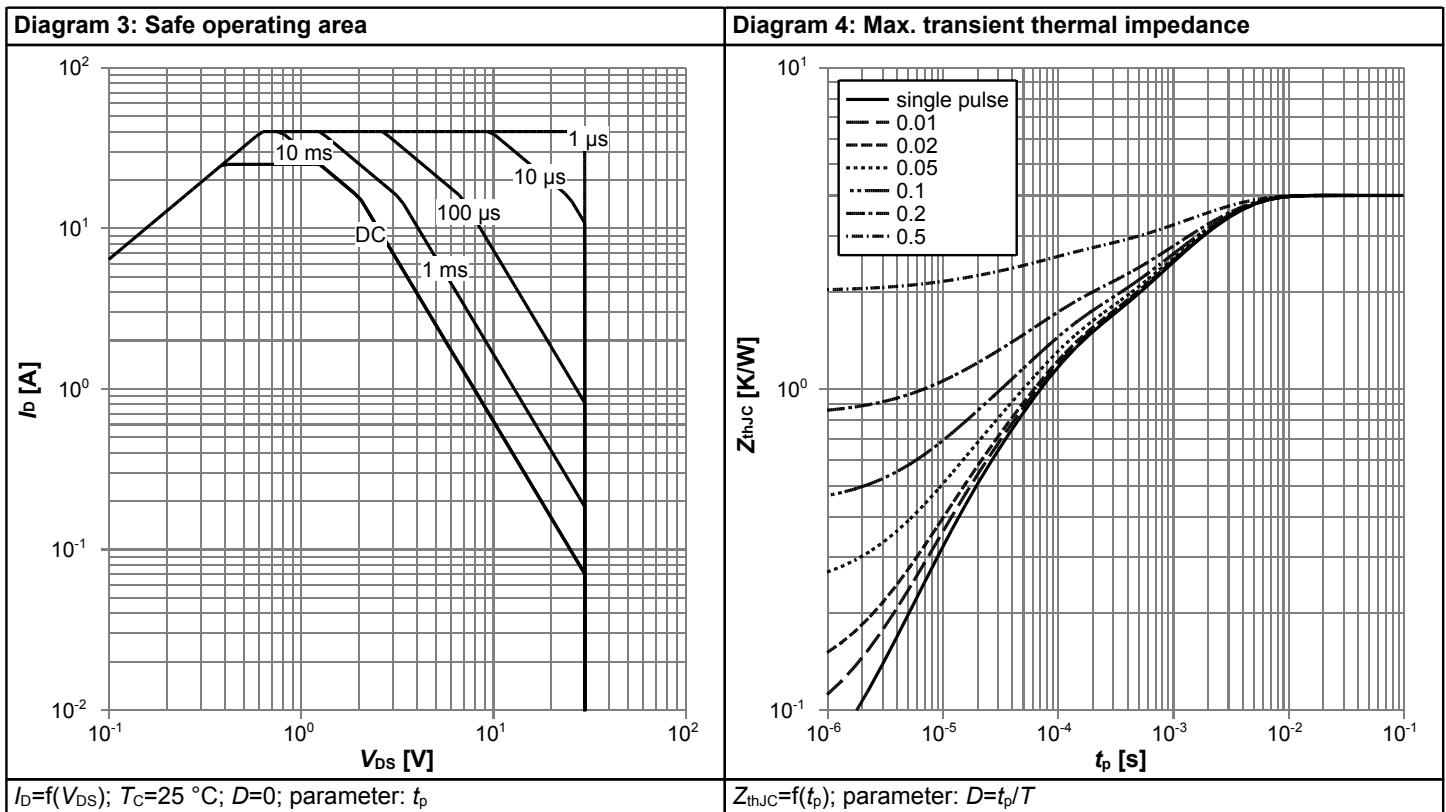
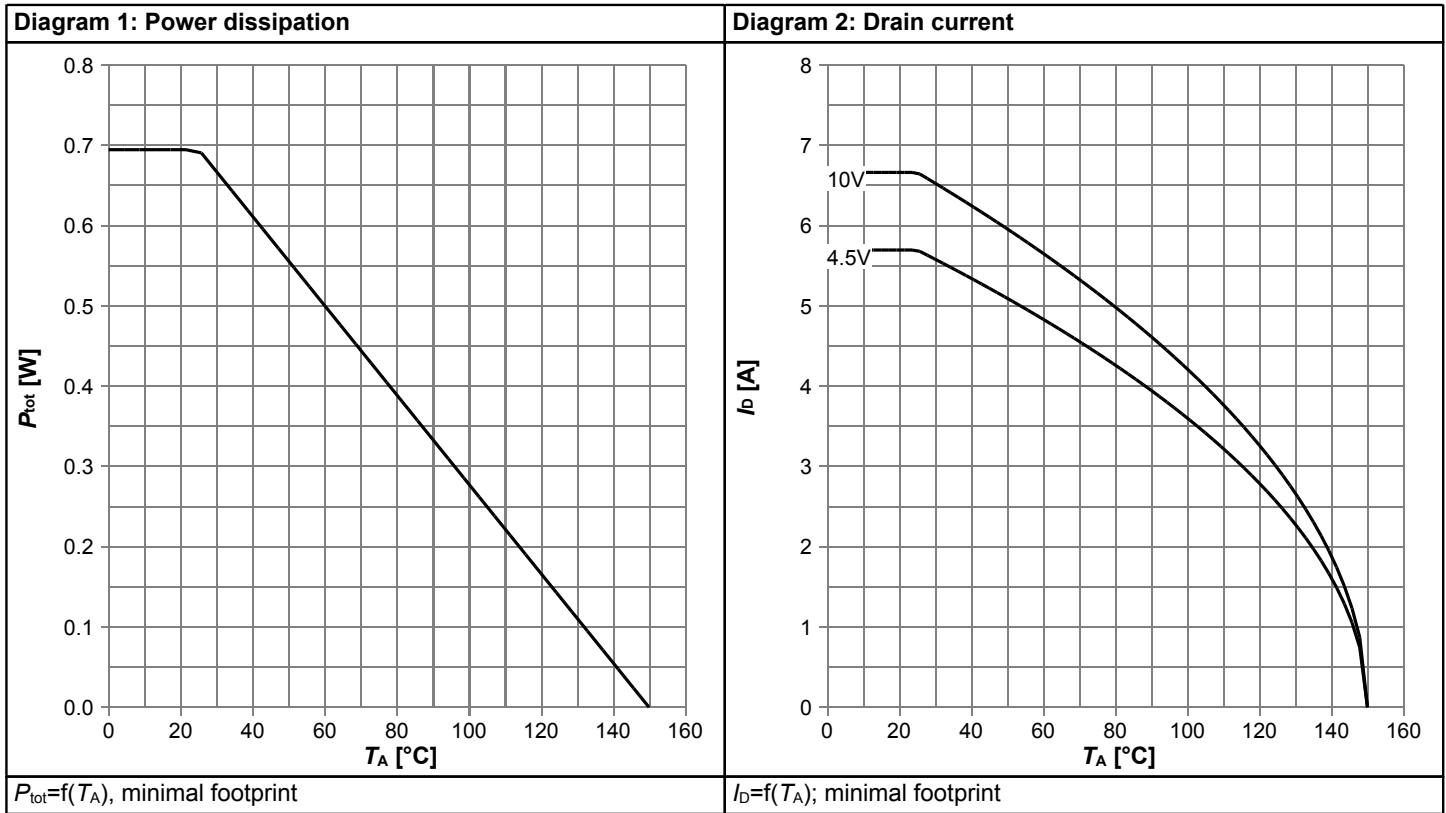
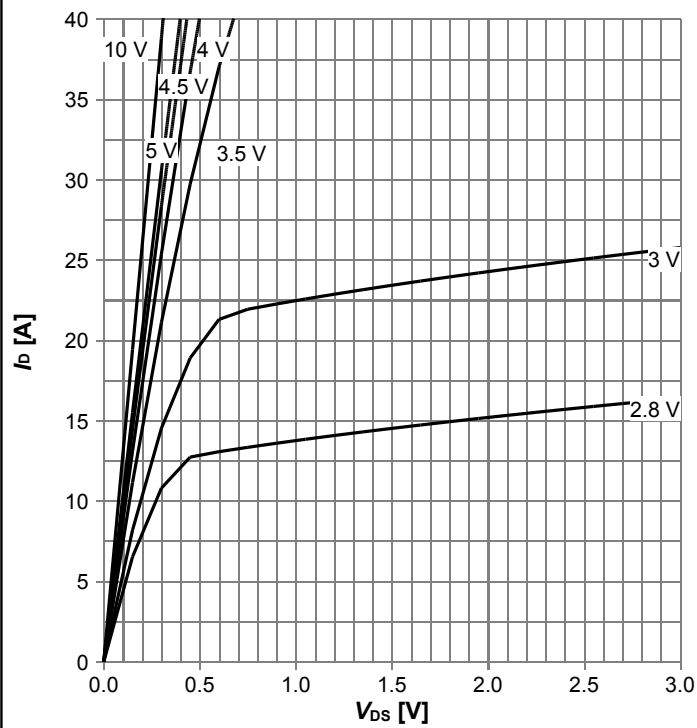
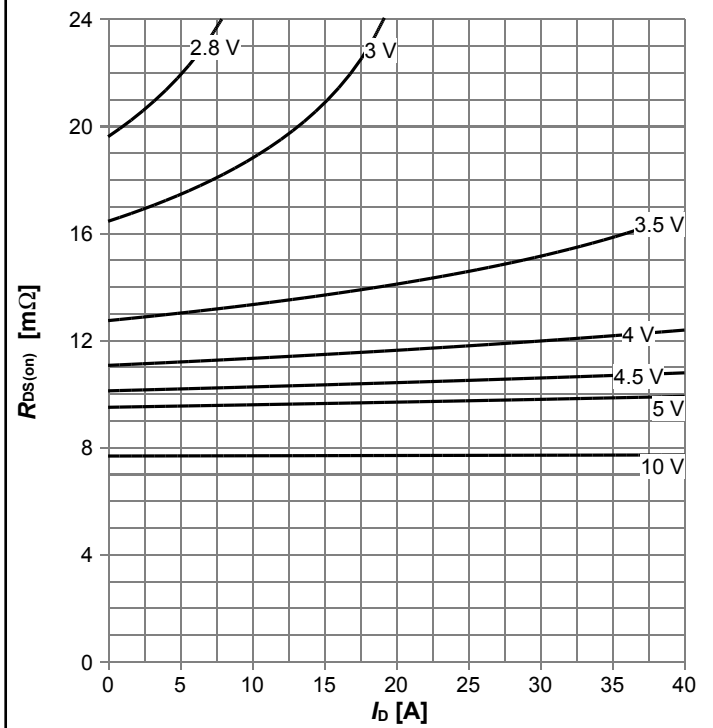


Diagram 5: Typ. output characteristics



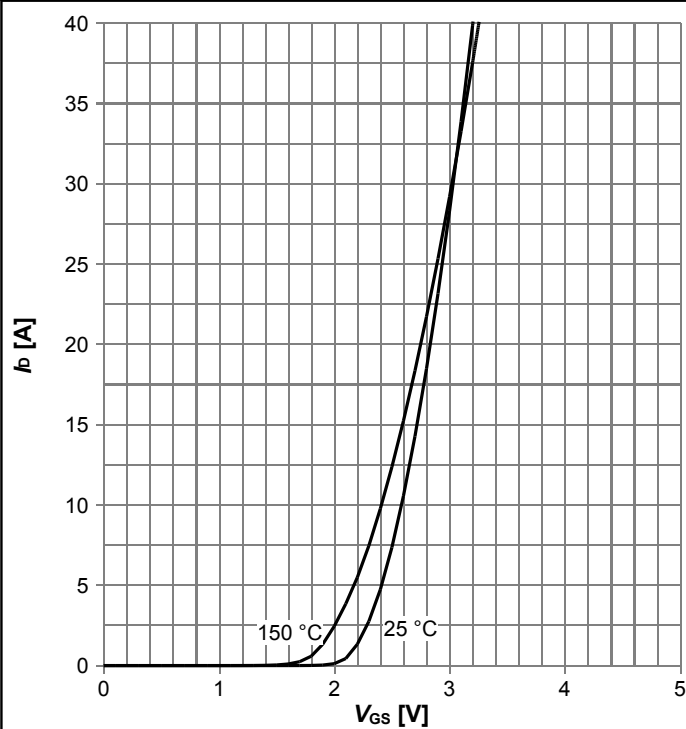
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



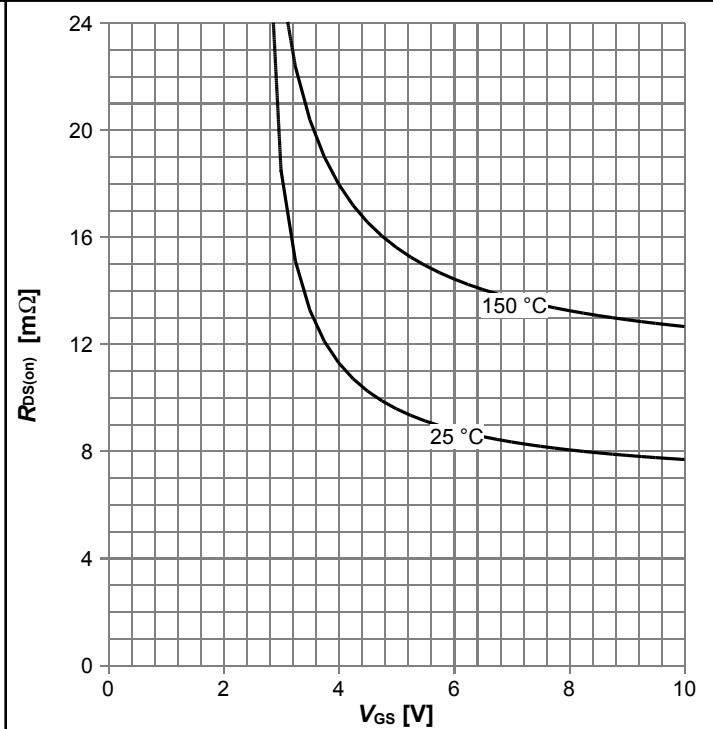
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



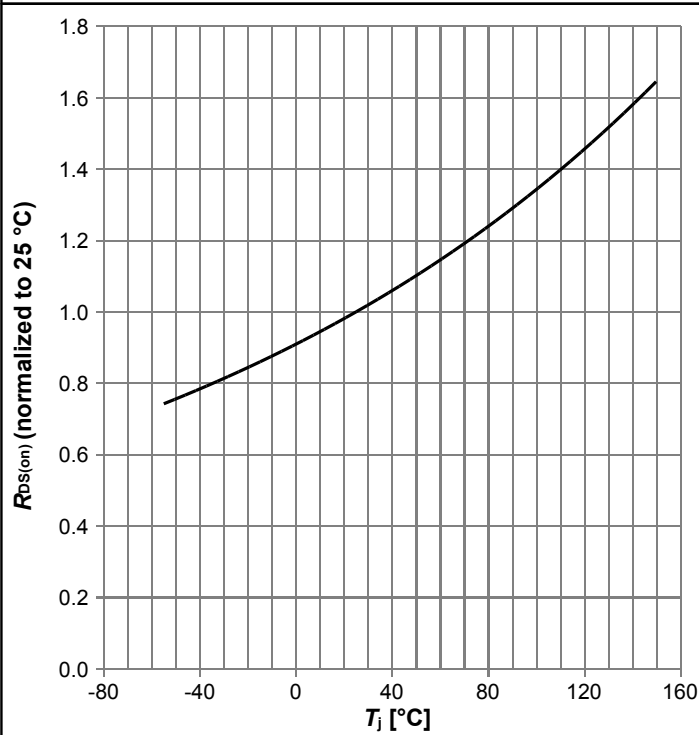
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D| R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



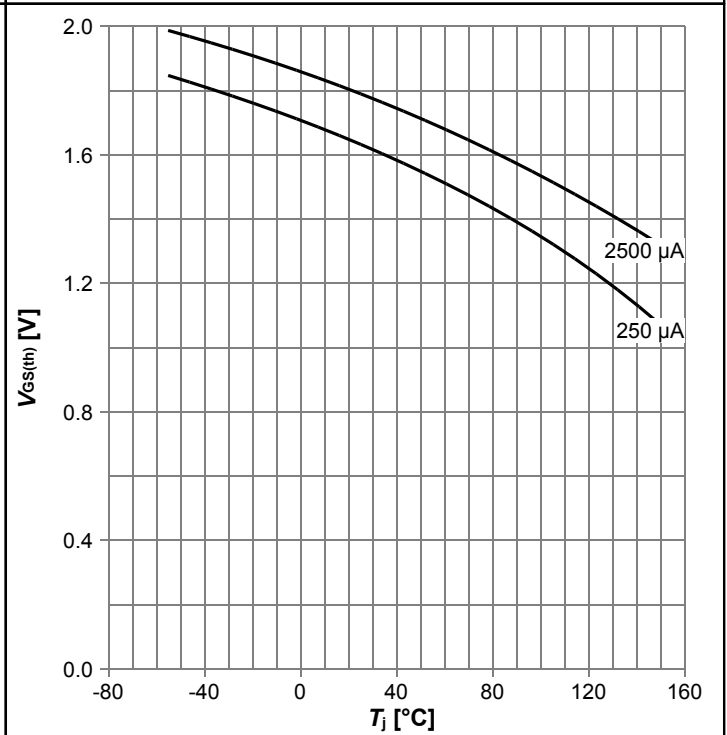
$R_{DS(on)} = f(V_{GS})$, $I_D = 9\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



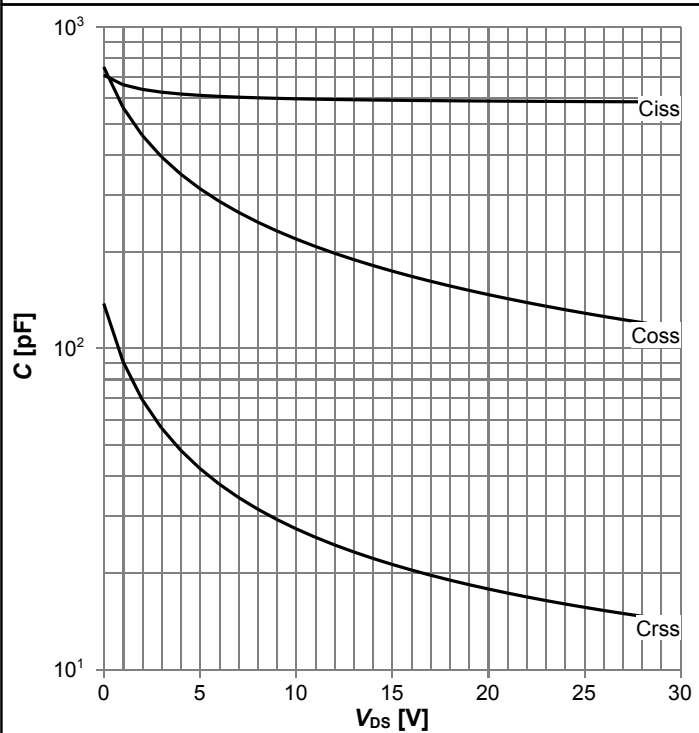
$R_{DS(on)}=f(T_j)$, $I_D=9\text{ A}$, $V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



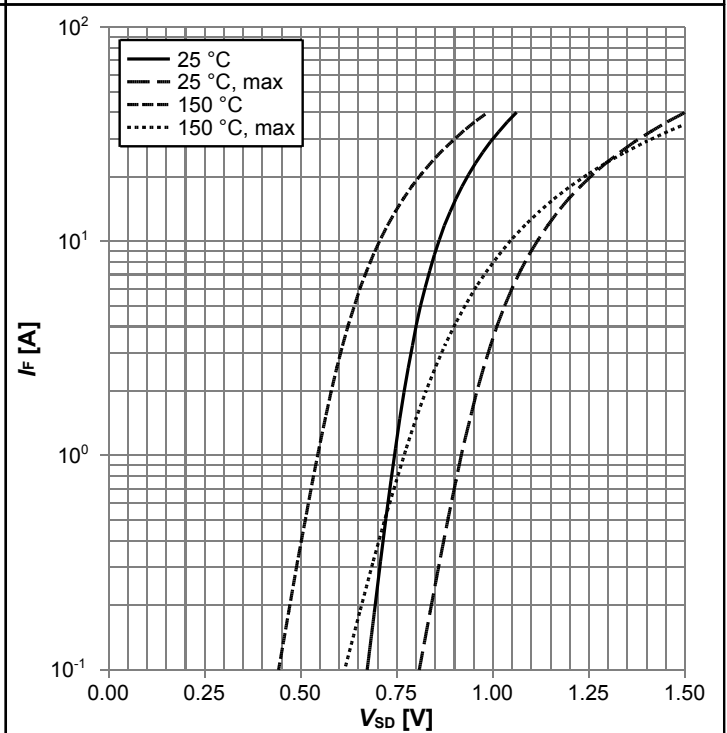
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



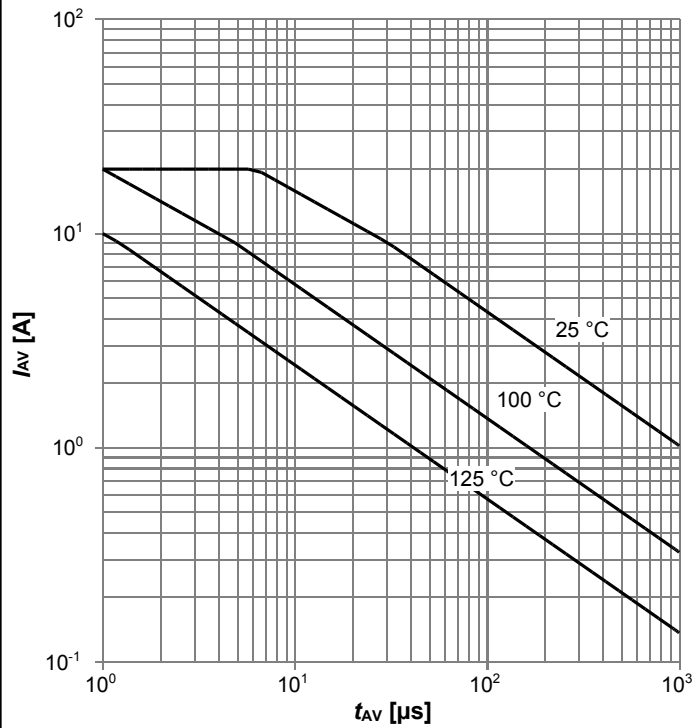
$C=f(V_{DS})$; $V_{GS}=0\text{ V}$; $f=1\text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



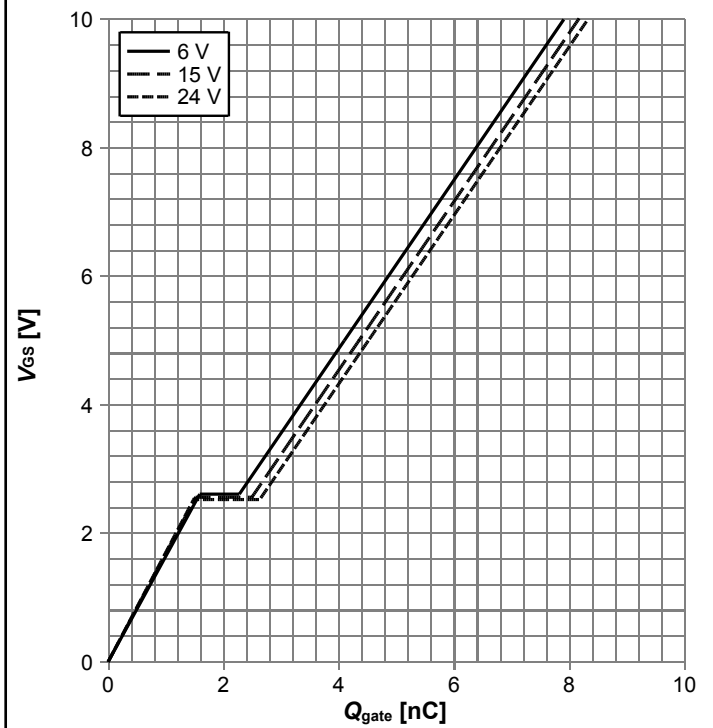
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



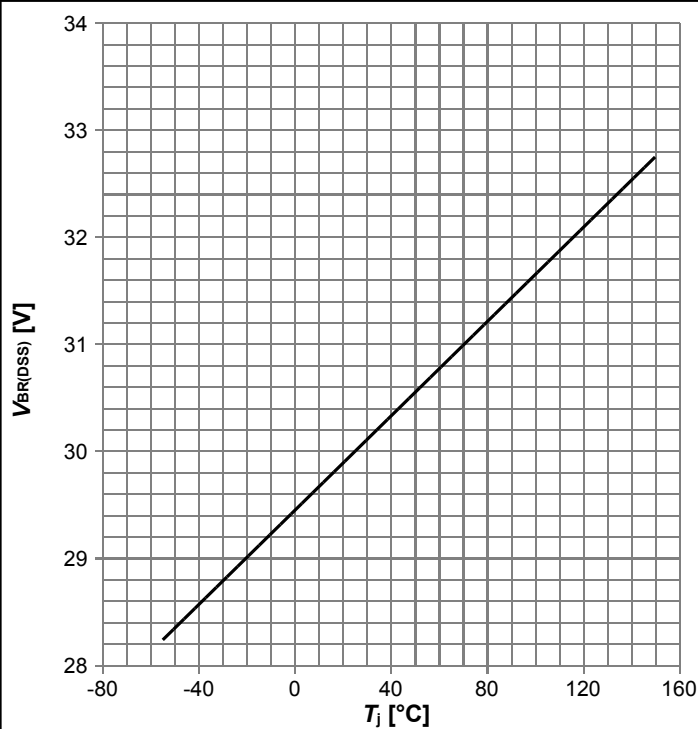
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



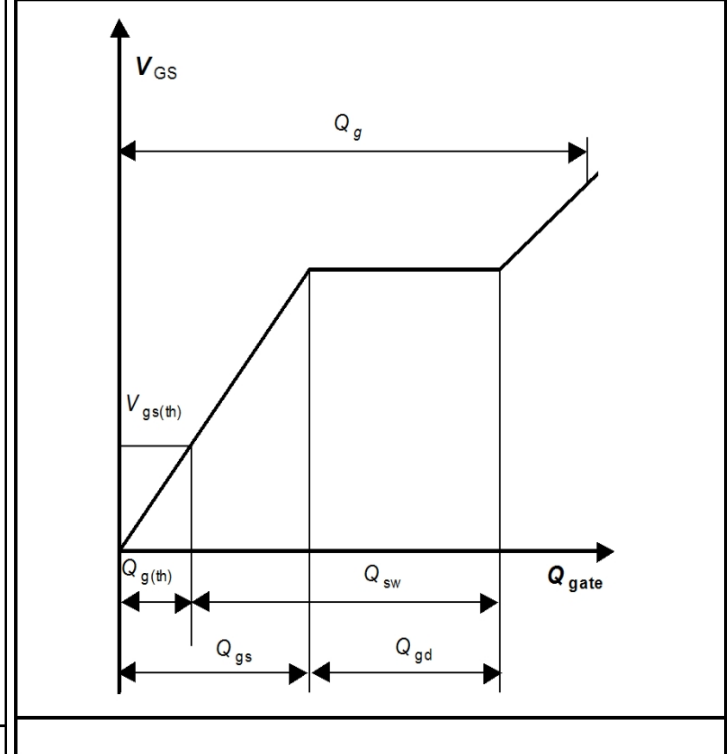
$V_{GS}=f(Q_{gate}), I_D=9 \text{ A pulsed}, T_j=25 \text{ °C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

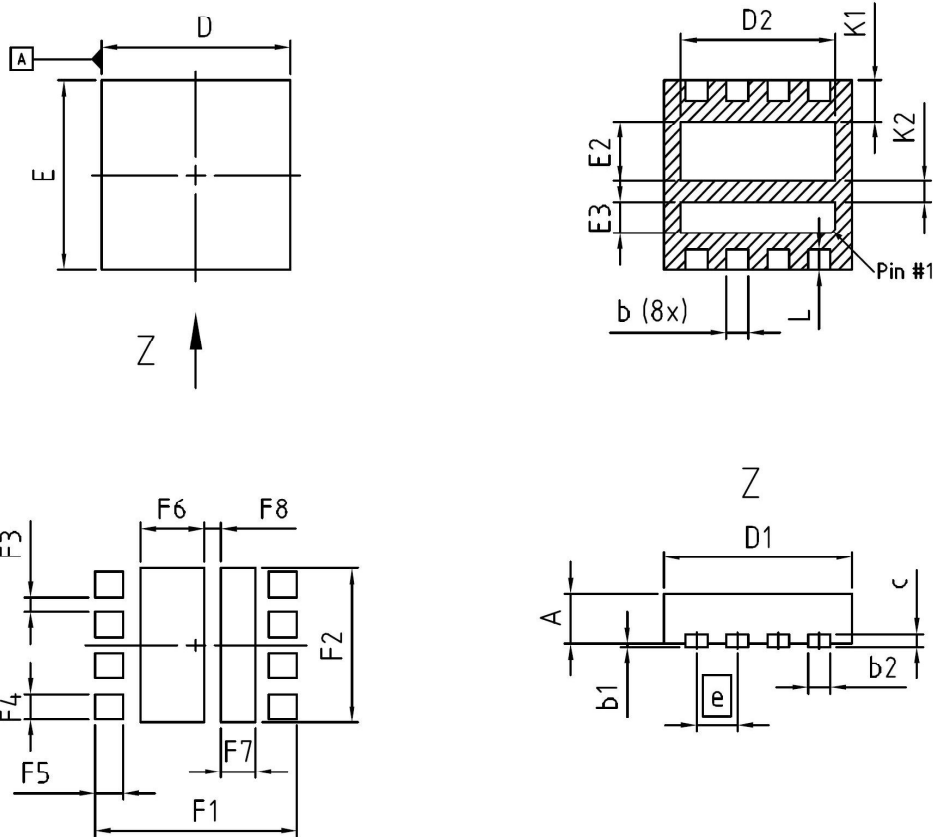


$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Gate charge waveforms



5 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.90	0.028	0.035
b	0.25	0.45	0.010	0.018
b1	0.00	0.05	0.000	0.002
b2	0.25	0.45	0.010	0.018
c	0.10	0.30	0.004	0.012
D=D1	2.90	3.10	0.114	0.122
D2	2.35	2.55	0.093	0.100
E=E1	2.90	3.10	0.114	0.122
E2	0.85	1.05	0.033	0.041
E3	0.39	0.59	0.015	0.023
K1	0.55	0.75	0.022	0.030
K2	0.23	0.43	0.009	0.017
e	0.65 (BSC)		0.026 (BSC)	
N	8		8	
L	0.22	0.42	0.009	0.017
F1	3.21		0.126	
F2	2.45		0.096	
F3	0.25		0.010	
F4	0.40		0.016	
F5	0.45		0.018	
F6	1.01		0.040	
F7	0.55		0.022	
F8	0.27		0.011	

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REVISION 01

Figure 1 Outline PG-WISON-8, dimensions in mm/inches

Revision History

BSZ0910ND

Revision: 2017-11-23, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2017-11-23	Release of final version

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