

FEATURES

- 2 mA full-scale current $\pm 20\%$, with $V_{REF} = \pm 10\text{ V}$
- 0.9 μs settling time to $\pm 0.1\%$
- 12 MHz multiplying bandwidth
- Midscale glitch of -1 nV-sec
- Midscale or zero-scale reset
- 4 separate, 4-quadrant multiplying reference inputs
- SPI-compatible, 3-wire interface
- Double-buffered registers enable
- Simultaneous multichannel change
- Internal power-on reset
- Compact 28-lead SSOP

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC)
- Military temperature range (-55°C to $+125^\circ\text{C}$)
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- Automatic test equipment
- Instrumentation
- Digitally controlled calibration

GENERAL DESCRIPTION

The **AD5544-EP** quad, 16-bit, current output, digital-to-analog converter (DAC) is designed to operate from a 2.7 V to 5.5 V supply range.

The applied external reference input voltage (V_{REFx}) determines the full-scale output current. Integrated feedback resistors (R_{FB}) provide temperature-tracking, full-scale voltage outputs when combined with an external I-to-V precision amplifier.

A double-buffered serial data interface offers high speed, 3-wire, SPI- and microcontroller-compatible inputs using serial data in (SDI), a chip select (\overline{CS}), and clock (CLK) signals. In addition, a serial data out pin (SDO) allows for daisy chaining when multiple

FUNCTIONAL BLOCK DIAGRAM

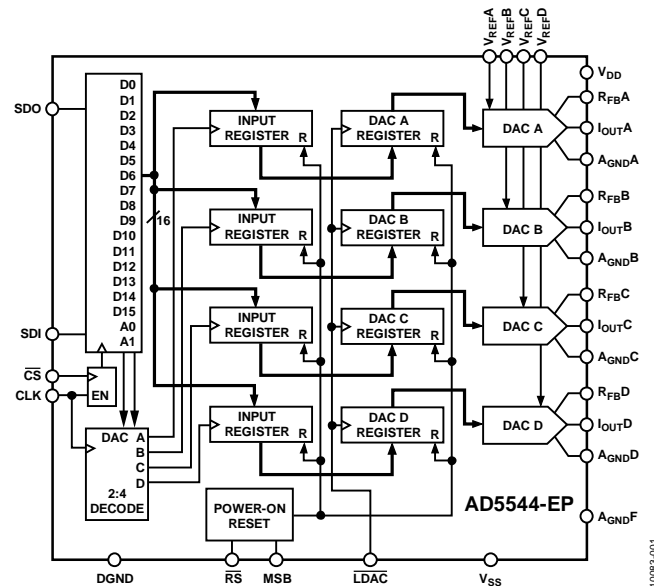


Figure 1.

packages are used. A common, level-sensitive, load DAC strobe (\overline{LDAC}) input allows the simultaneous update of all DAC outputs from previously loaded input registers. Additionally, an internal power-on reset forces the output voltage to 0 at system turn-on. The MSB pin allows system reset assertion (\overline{RS}) to force all registers to zero code when $\text{MSB} = 0$ or to half-scale code when $\text{MSB} = 1$. The **AD5544-EP** is packaged in the compact 28-lead SSOP.

Additional application and technical information can be found in the [AD5544](#) data sheet.

Rev. 0

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TABLE OF CONTENTS

| | | | |
|---------------------------------|---|--|----|
| Features | 1 | Absolute Maximum Ratings | 5 |
| Enhanced Product Features | 1 | ESD Caution..... | 5 |
| Applications..... | 1 | Pin Configuration and Function Descriptions..... | 6 |
| Functional Block Diagram | 1 | Typical Performance Characteristics | 8 |
| General Description | 1 | Outline Dimensions | 10 |
| Revision History | 2 | Ordering Guide | 10 |
| Specifications..... | 3 | | |
| Timing Diagrams..... | 4 | | |

REVISION HISTORY

4/12—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, $I_{OUTX} = \text{virtual GND}$, $A_{GNDX} = 0\text{ V}$, $V_{REFA} = V_{REFB} = V_{REFC} = V_{REFD} = 10\text{ V}$, $T_A = \text{full operating temperature range of } -55^\circ\text{C to } +125^\circ\text{C}$, unless otherwise noted.

Table 1.

| Parameter | Symbol | Test Condition/Comments | Min | Typ | Max | Unit |
|--|-----------------------|--|------|------------|-----------|-----------------------|
| STATIC PERFORMANCE¹ | | | | | | |
| Resolution | N | 1 LSB = $V_{REFX}/2^{16} = 153\ \mu\text{V}$ when $V_{REF} = 10\text{ V}$ | | | 16 | Bits |
| Relative Accuracy | INL | | | | ± 1.5 | LSB |
| Differential Nonlinearity | DNL | | | | ± 1.5 | LSB |
| Output Leakage Current | I_{OUTX} | Data = 0x0000, $T_A = 25^\circ\text{C}$ Data = 0x0000, $T_A = 85^\circ\text{C}$ | | | 10 20 | nA nA |
| Full-Scale Gain Error | G_{FSE} | Data = 0xFFFF | | ± 0.75 | ± 4 | mV |
| Full-Scale Tempco ² | TCV_{FS} | | | 1 | | ppm/ $^\circ\text{C}$ |
| Feedback Resistor | R_{FBX} | $V_{DD} = 5\text{ V}$ | 4 | 6 | 8 | k Ω |
| REFERENCE INPUT | | | | | | |
| V_{REFX} Range | V_{REFX} | | -15 | | +15 | V |
| Input Resistance | R_{REFX} | | 4 | 6 | 8 | k Ω |
| Input Resistance Match | R_{REFX} | Channel-to-channel | | 0.35 | | % |
| Input Capacitance ² | C_{REFX} | | | 5 | | pF |
| ANALOG OUTPUT | | | | | | |
| Output Current | I_{OUTX} | Data = 0xFFFF | 1.25 | | 2.5 | mA |
| Output Capacitance ² | C_{OUTX} | Code dependent | | 35 | | pF |
| LOGIC INPUT AND OUTPUT | | | | | | |
| Logic Input Low Voltage | V_{IL} | | | | 0.8 | V |
| Logic Input High Voltage | V_{IH} | | 2.4 | | | V |
| Input Leakage Current | I_{IL} | | | | 1 | μA |
| Input Capacitance ² | C_{IL} | | | | 10 | pF |
| Logic Output Low Voltage | V_{OL} | $I_{OL} = 1.6\text{ mA}$ | | | 0.4 | V |
| Logic Output High Voltage | V_{OH} | $I_{OH} = 100\ \mu\text{A}$ | 4 | | | V |
| INTERFACE TIMING^{2, 3} | | | | | | |
| Clock Width High | t_{CH} | | 25 | | | ns |
| Clock Width Low | t_{CL} | | 25 | | | ns |
| $\overline{\text{CS}}$ to Clock Setup | t_{CSS} | | 0 | | | ns |
| Clock to $\overline{\text{CS}}$ Hold | t_{CSH} | | 25 | | | ns |
| Clock to SDO Propagation Delay | t_{PD} | | 2 | | 20 | ns |
| Load DAC Pulse Width | t_{LDAC} | | 25 | | | ns |
| Data Setup | t_{DS} | | 20 | | | ns |
| Data Hold | t_{DH} | | 20 | | | ns |
| Load Setup | t_{LDS} | | 5 | | | ns |
| Load Hold | t_{LDH} | | 25 | | | ns |
| SUPPLY CHARACTERISTICS | | | | | | |
| Power Supply Range | $V_{DD\text{ RANGE}}$ | | 2.7 | | 5.5 | V |
| Positive Supply Current | I_{DD} | Logic inputs = 0 V | | | 5 | μA |
| Negative Supply Current | I_{SS} | Logic inputs = 0 V, $V_{SS} = -5\text{ V}$ | | 0.001 | 9 | μA |
| Power Dissipation | P_{DISS} | Logic inputs = 0 V | | | 1.25 | mW |
| Power Supply Sensitivity | PSS | $\Delta V_{DD} = \pm 5\%$ | | | 0.006 | %/% |

| Parameter | Symbol | Test Condition/Comments | Min | Typ | Max | Unit |
|--------------------------------------|-----------------------------------|---|-----|-----|-----|------------------------------|
| AC CHARACTERISTICS ⁴ | | | | | | |
| Output Voltage Settling Time | t_s | To $\pm 0.1\%$ of full scale, data = 0x0000 to 0xFFFF to 0x0000 | | 0.9 | | μs |
| Reference Multiplying Bandwidth (BW) | BW – 3 dB | $V_{\text{REF}X} = 5\text{ V p-p}$, data = 0xFFFF, $C_{\text{FB}} = 2.0\text{ pF}$, | | 12 | | MHz |
| DAC Glitch Impulse | Q | $V_{\text{REF}X} = 8\text{ V}$, data = 0x0000 to 0x8000 to 0x0000 | | -1 | | nV-sec |
| Feedthrough Error | $V_{\text{OUT}X}/V_{\text{REF}X}$ | Data = 0x0000, $V_{\text{REF}X} = 100\text{ mV rms}$, $f = 100\text{ kHz}$ | | -65 | | dB |
| Crosstalk Error | $V_{\text{OUT}A}/V_{\text{REF}B}$ | Data = 0x0000, $V_{\text{REF}B} = 100\text{ mV rms}$, adjacent channel, $f = 100\text{ kHz}$ | | -90 | | dB |
| Digital Feedthrough | Q | $\overline{\text{CS}} = 1$, $f_{\text{CLK}} = 1\text{ MHz}$ | | 0.6 | | nV-sec |
| Total Harmonic Distortion | THD | $V_{\text{REF}X} = 5\text{ V p-p}$, data = 0xFFFF, $f = 1\text{ kHz}$ | | -98 | | dB |
| Output Spot Noise Voltage | e_N | $f = 1\text{ kHz}$, BW = 1 Hz | | 7 | | $\text{nV}/\sqrt{\text{Hz}}$ |

¹ All static performance tests (except $I_{\text{OUT}X}$) are performed in a closed-loop system using an external precision OP177 I-to-V converter amplifier. The AD5544 R_{FB} terminal is tied to the amplifier output. Typical values represent average readings measured at 25°C.

² These parameters are guaranteed by design and not subject to production testing.

³ All input control signals are specified with $t_r = t_f = 2.5\text{ ns}$ (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

⁴ All ac characteristic tests are performed in a closed-loop system using an AD8038 I-to-V converter amplifier.

TIMING DIAGRAMS

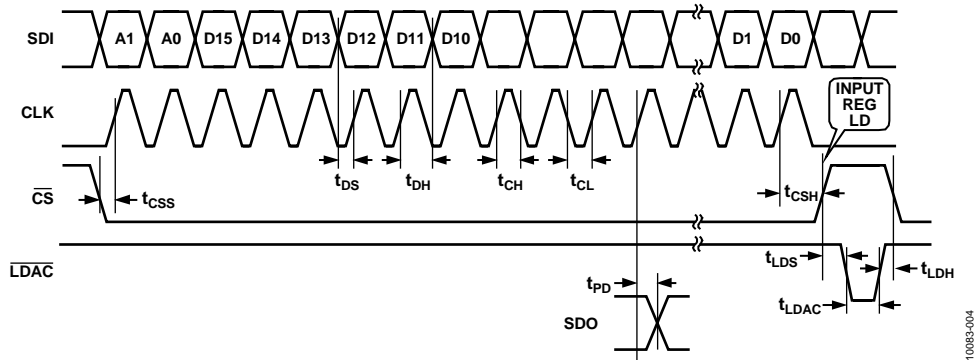


Figure 2. Timing Diagram

10083-004

ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter | Rating |
|--|---------------------------------------|
| V_{DD} to GND | -0.3 V, +8 V |
| V_{SS} to GND | +0.3 V, -7 V |
| V_{REFX} to GND | -18 V, +18 V |
| Logic Input and Output to GND | -0.3 V, +8 V |
| $V(I_{OUTX})$ to GND | -0.3 V, $V_{DD} + 0.3$ V |
| A_{GNDX} to DGND | -0.3 V, +0.3 V |
| Input Current to Any Pin Except Supplies | ±50 mA |
| Package Power Dissipation | $(T_J \text{ max} - T_A)/\theta_{JA}$ |
| Thermal Resistance | θ_{JA} |
| 28-Lead SSOP | 100°C/W |
| 32-Lead LFCSP | 32.5°C/W |
| Maximum Junction Temperature (T_J Max) | 150°C |
| Operating Temperature Range, Enhanced Product (EP Version) | -55°C to +125°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature | |
| Vapor Phase, 60 Sec | 215°C |
| Infrared, 15 Sec | 220°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

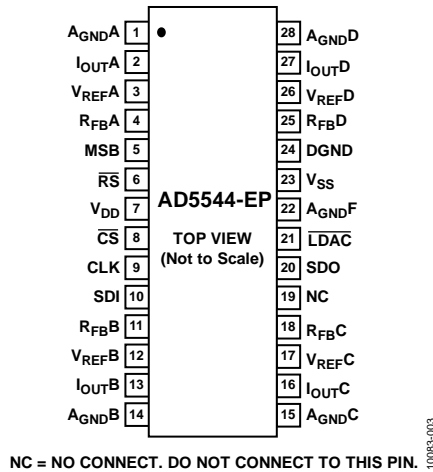


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|--------------------|---|
| 1 | A _{GND} A | DAC A Analog Ground. |
| 2 | I _{OUT} A | DAC A Current Output. |
| 3 | V _{REF} A | DAC A Reference Voltage Input Terminal. Establishes DAC A full-scale output voltage. This pin can be tied to the V _{DD} pin. |
| 4 | R _{FB} A | Establish the voltage output for DAC A by connecting to an external amplifier output. |
| 5 | MSB | MSB Pin. Set pin during a reset pulse (\overline{RS}) or at system power-on if tied to ground or V _{DD} . |
| 6 | \overline{RS} | Reset Pin, Active Low Input. Input registers and DAC registers are set to all 0s or half-scale code, determined by the voltage on the MSB pin. Register data = 0x0000 when MSB = 0. |
| 7 | V _{DD} | Positive Power Supply Input. Specified range of operation: 5 V ± 10%. |
| 8 | \overline{CS} | Chip Select, Active Low Input. Disables shift register loading when high. Transfers serial register data to the input register when \overline{CS} /LDAC returns high. Does not affect LDAC operation. |
| 9 | CLK | Clock Input. Positive edge clocks data into the shift register. |
| 10 | SDI | Serial Data Input. Input data loads directly into the shift register. |
| 11 | R _{FB} B | Establish the voltage output for DAC B by connecting to an external amplifier output. |
| 12 | V _{REF} B | DAC B Reference Voltage Input Terminal. Establishes DAC B full-scale output voltage. This pin can be tied to the V _{DD} pin. |
| 13 | I _{OUT} B | DAC B Current Output. |
| 14 | A _{GND} B | DAC B Analog Ground. |
| 15 | A _{GND} C | DAC C Analog Ground. |
| 16 | I _{OUT} C | DAC C Current Output. |
| 17 | V _{REF} C | DAC C Reference Voltage Input Terminal. Establishes DAC C full-scale output voltage. This pin can be tied to the V _{DD} pin. |
| 18 | R _{FB} C | Establish the voltage output for DAC C by connecting to an external amplifier output. |
| 19 | NC | No Connect. Do not connect to this pin. |
| 20 | SDO | Serial Data Output. Input data loads directly into the shift register. Data appears at SDO at 19 clock pulses for the AD5544-EP after input at the SDI pin. |
| 21 | \overline{LDAC} | Load DAC Register Strobe, Level Sensitive Active Low. Transfers all input register data to DAC registers. Asynchronous active low input. |
| 22 | A _{GND} F | High Current Analog Force Ground. |
| 23 | V _{SS} | Negative Bias Power Supply Input. Specified range of operation: -5.5 V to +0.3 V. |
| 24 | DGND | Digital Ground Pin. |
| 25 | R _{FB} D | Establish the voltage output for DAC D by connecting to an external amplifier output. |

| Pin No. | Mnemonic | Description |
|---------|-------------|--|
| 26 | V_{REFD} | DAC D Reference Voltage Input Terminal. Establishes DAC D full-scale output voltage. This pin can be tied to the V_{DD} pin. |
| 27 | I_{OUTD} | DAC D Current Output. |
| 28 | $A_{GND D}$ | DAC D Analog Ground. |

TYPICAL PERFORMANCE CHARACTERISTICS

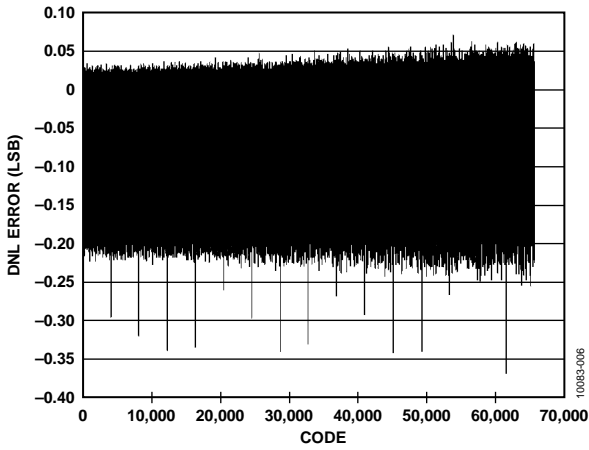


Figure 4. DNL Error vs. Code, $T_A = 25^\circ\text{C}$

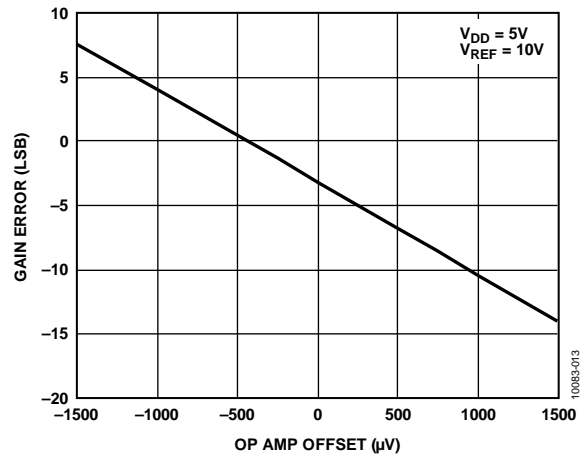


Figure 7. Gain Error vs. Op Amp Offset

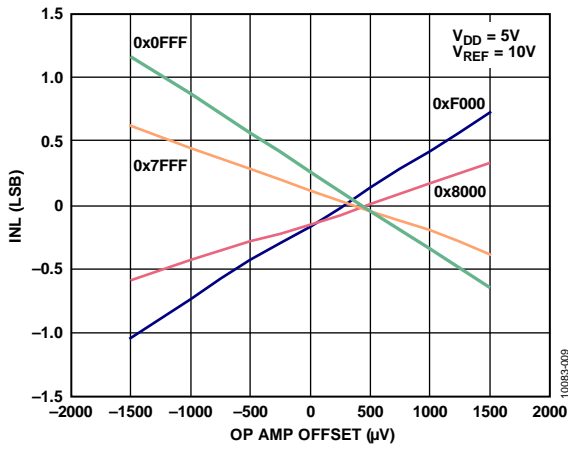


Figure 5. INL Error vs. Op Amp Offset

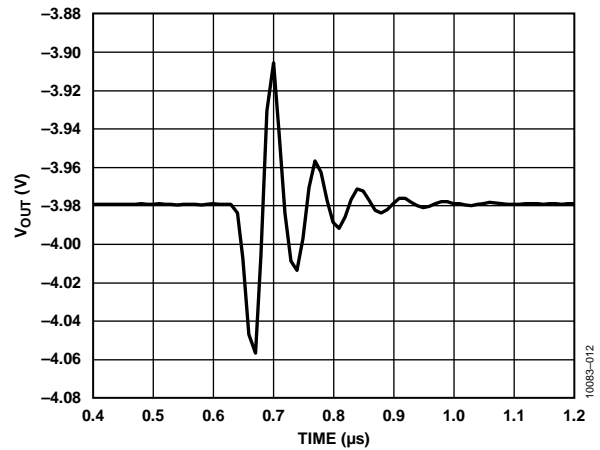


Figure 8. Midscale Transition

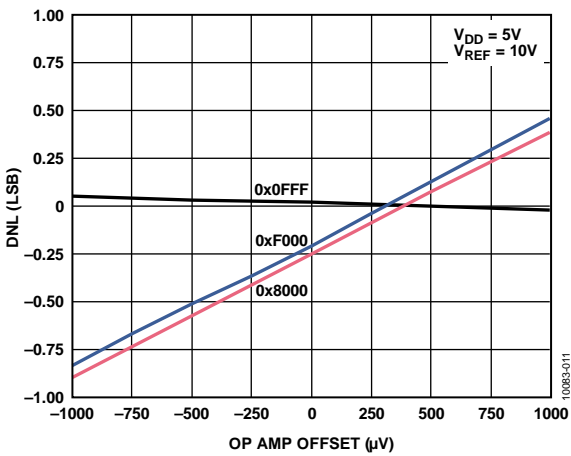


Figure 6. DNL Error vs. Op Amp Offset

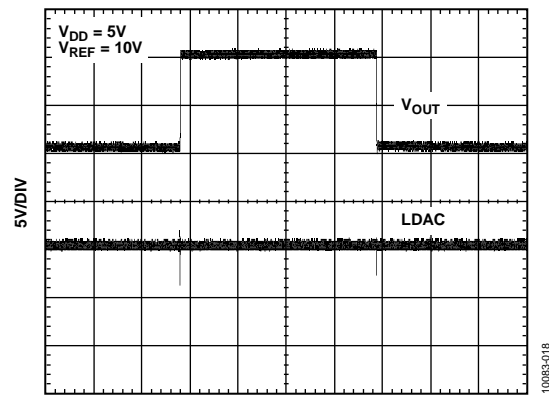


Figure 9. Large Signal Settling Time

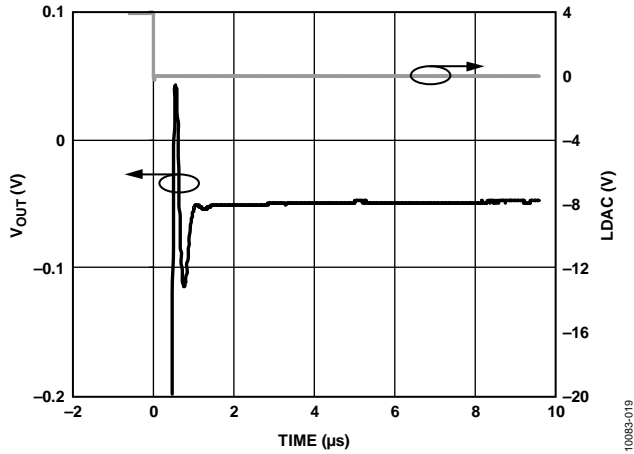


Figure 10. Small Signal Settling Time

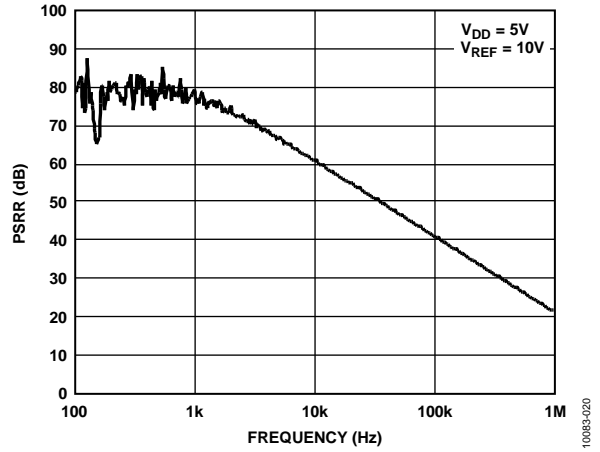


Figure 12. Power Supply Rejection vs. Frequency

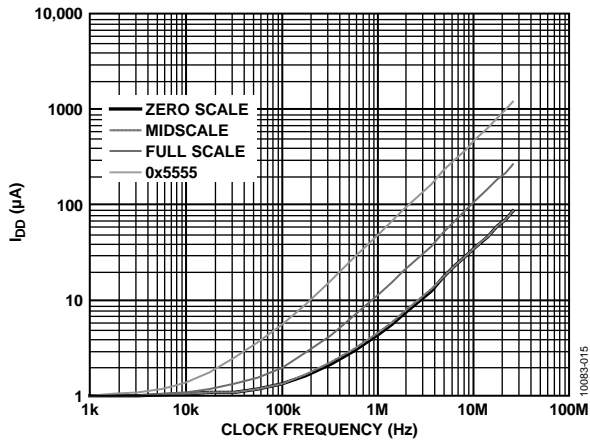


Figure 11. Power Supply Current vs. Clock Frequency

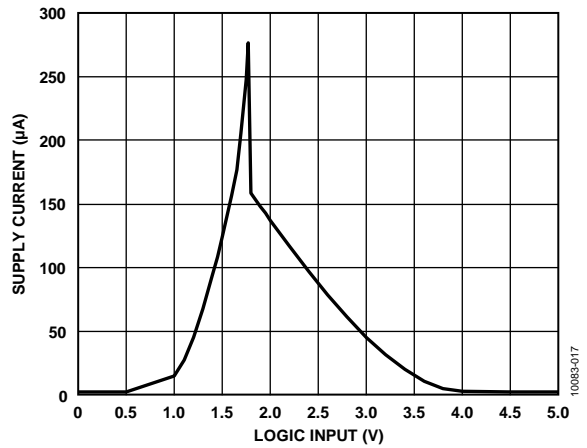
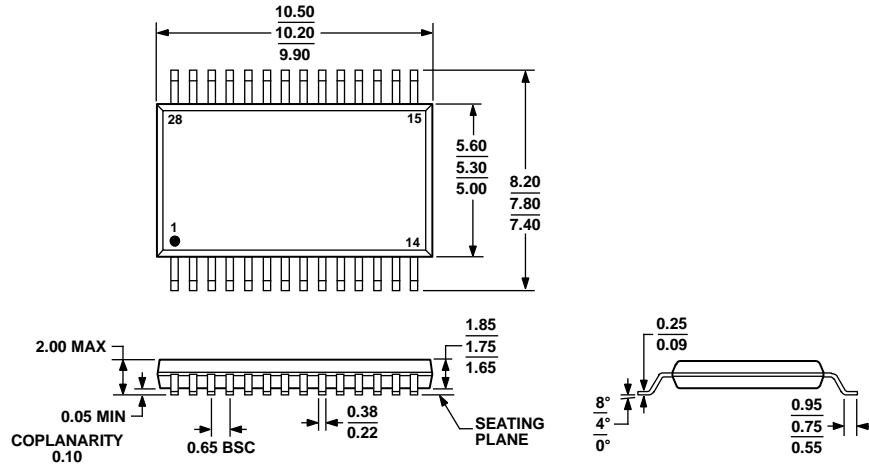


Figure 13. Power Supply Current vs. Logic Input Voltage

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-150-AH
 Figure 4. 28-Lead Shrink Small Outline Package [SSOP]
 (RS-28)
 Dimensions shown in millimeters

ORDERING GUIDE

| Model | Resolution (Bits) | INL LSB | DNL LSB | Temperature Range | Package Description | Package Option |
|--------------|-------------------|---------|---------|-------------------|---|----------------|
| AD5544SRS-EP | 16 | ±1.5 | ±1.5 | -55°C to +125°C | 28-Lead Shrink Small Outline Package [SSOP] | RS-28 |

NOTES

NOTES