



Package Style: Laminate 24-Pin 5mm x 5mm x 1mm

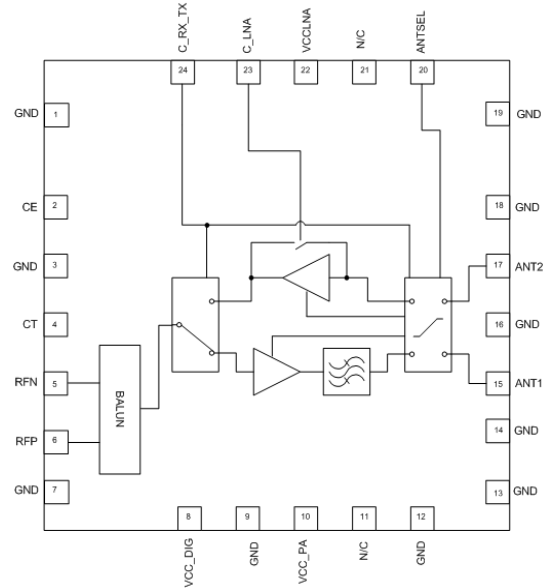


Features

- Tx Output Power = 18dBm
- Integrated RF Front End Module with Rx Balun, PA, Filter, LNA with Bypass Mode, and DP2T Switch
- Single Bidirectional Differential Transceiver Interface.
- Voltage Range = 2.0V to 3.6V

Applications

- ZigBee® 802.15.4 Based Systems for Remote Monitoring and Control
- AA Battery Operation
- 2.4GHz ISM Band Applications
- Smart Meters for Energy Management



Functional Block Diagram

Product Description

The RF6555 integrates a complete solution in a single Front End Module (FEM) for WiFi and ZigBee® applications in the 2.4GHz to 2.5GHz band. This FEM integrates the PA plus harmonic filter in the transmit path. The RF6555 also has an integrated LNA with bypass mode internally. The RF6555 provides a single balanced TDD access for Rx and Tx paths along with two ports on the output for connecting a diversity solution or a test port. The device is provided in a 5mm x 5mm x 1mm, 24-pin laminate package.

Ordering Information

RF6555	3.3V Front End Module for AMR systems in the 2.4GHz to 2.5GHz Band
RF6555SQ	Standard 25 piece bag
RF6555SR	Standard 100 piece reel
RF6555TR13	Standard 2500 piece reel
RF6555PCK-410	Fully assembled evaluation board and 5 loose pieces

Optimum Technology Matching® Applied

- | | | | |
|---|--------------------------------------|--|------------------------------------|
| <input type="checkbox"/> GaAs HBT | <input type="checkbox"/> SiGe BiCMOS | <input checked="" type="checkbox"/> GaAs pHEMT | <input type="checkbox"/> GaN HEMT |
| <input type="checkbox"/> GaAs MESFET | <input type="checkbox"/> Si BiCMOS | <input type="checkbox"/> Si CMOS | <input type="checkbox"/> BiFET HBT |
| <input checked="" type="checkbox"/> InGaP HBT | <input type="checkbox"/> SiGe HBT | <input type="checkbox"/> Si BJT | <input type="checkbox"/> LD MOS |

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Absolute Maximum Ratings

Parameter	Rating	Unit
DC Supply Voltage	4.0	V
DC Supply Current	150	mA
Operating Case Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
ESD Human Body Model RF Pins	1000	V
ESD Human Body Model All Other Pins	500	V
ESD Charge Device Model All Pins	500	V
Moisture Sensitivity Level	MSL 2	
Maximum Tx Input Power	+5	dBm
Maximum Rx Input Power	+8	dBm



Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

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RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					Specifications must be met across supply voltage, control voltage, and temperature ranges unless otherwise specified.
V _{BATT}	2.0	3.0	3.6	V _{DC}	
Operating Temperature Range	-40	+25	+85	°C	
Z ₀		50		Ω	
Off Mode Current		0.5	1	μA	All logic low, Temp = 25 °C; Over Voltage.
Storage Temperature	-40		+150	°C	
ESD, HBM	1000			V	RF pins
ESD, HBM	500			V	All other pins
ESD, CDM	500			V	All pins
MSL	MSL3				
Current Sourced through CT Pin			18	mA	
Voltage Drop from CT Pin to RXP/RXN			0.1	V	
Tx Path					
Frequency	2405		2480	MHz	
Input Return Loss	10			dB	Pins 5, 6 (RFN, RFP) 100Ω differential
Output Return Loss	10			dB	
Gain	22	25		dB	2.7V to 3.6V.
	21			dB	V _{CC} = 2.0V; Temp = 25 °C
Gain Flatness	-0.8		+0.8	dB	
Rated Output Power	18			dBm	Nominal conditions (V _B = 3.0 to 3.6, All Temp)
	16			dBm	Nominal conditions (V _B = 2.7, All Temp)
	14			dBm	Nominal conditions (V _B = 2.0, All Temp)
Supply Current		70	100	mA	P _O = 18dBm 802.15.4 OQPSK
Thermal Resistance		78		°C/W	V _{CC} = 3.0V, P _{OUT} = 18dBm, T _{REF} = 85 °C
Harmonics 2fo to 5fo		-45	-42	dBm/MHz	At 18dBm, V _{CC} = 3.0V to 3.6V
VSWR Stability and Load	4:1				
VSWR No Damage	8:1				
Gain Settling Time		1	10	μS	

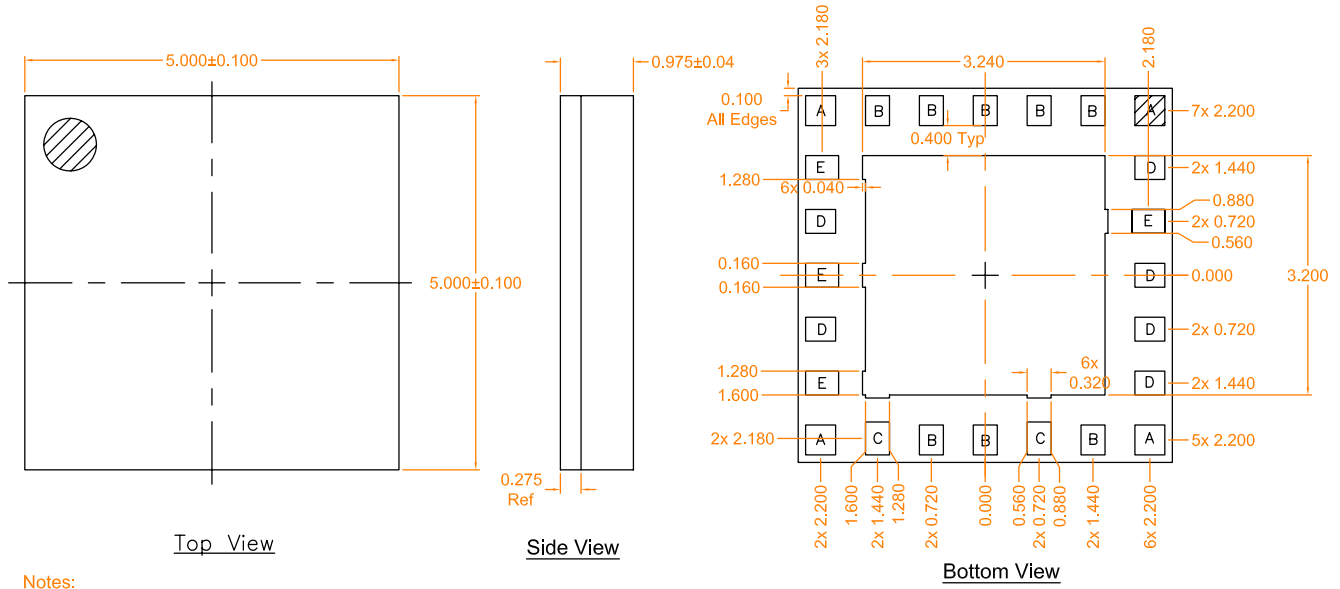
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Rx Path					
Frequency	2405		2480	MHz	
Gain	8.5	11	13	dB	
Noise Figure		3		dB	Temp = 25 °C; over voltage and frequency.
Current		8	12	mA	Nominal conditions
IIP3		7		dBm	
Gain Flatness	-0.5		+0.5	dB	
Input Return Loss	10	15		dB	
Output Return Loss	10			dB	Pins 5, 6 (RFN, RFP) 100Ω differential
Amplitude Imbalance	-1		+1	dB	
Phase Imbalance	-15		+15	dB	
Maximum Input Power	5			dBm	
Bypass Mode					
Frequency	2405		2480	MHz	
Insertion Loss/Noise Figure		5	6.5	dB	SW 1dB, Bypass 2.5dB, Balun 1.5dB
Current		50		μA	
IIP3		23		dBm	
Gain Flatness	-0.5		+0.5	dB	
Input Return Loss	10	12		dB	
Output Return Loss	10			dB	Pins 5, 6 (RFN, RFP) 100Ω differential
Amplitude Imbalance	-1		+1	dB	
Phase Imbalance	-15		+15	dB	
Maximum Input Power	10			dBm	
Logic					
Logic Level "HIGH" Input Voltage	$V_{BATT}-0.2$		V_{BATT}	V	
Logic Level "LOW" Input Voltage	0.0		0.2	V	
Input Source Current at Logic "HIGH"		5	10	μA	
Switch Leakage Current at Logic "LOW"			1	μA	
Antenna Switch					
RF to Control Isolation		50		dB	
ANT1 to ANT2 Isolation		20		dB	
T/R Switching Time			1	μs	

Control Logic

Mode	CE	C_RX_TX	C_LNA	ANTSEL
TX-ANT1	High	High	Low	Low
TX-ANT2	High	High	Low	High
RX-ANT1 LNA	High	Low	Low	Low
RX-ANT1 BYP	High	Low	High	Low
RX-ANT2 LNA	High	Low	Low	High
RX-ANT2 BYP	High	Low	High	High
Power Down	Low	Low	Low	Low

Pin	Function	Description
1	GND	Ground.
2	CE	Control voltage pin for chip enable. See logic table.
3	GND	Ground.
4	CT	Center tap for passing DC voltage to RFN/RFP pins that connect to the TXVR SoIC.
5	RFN	Differential bi-directional RF port. Matched to 50Ω single-ended, 100Ω differential.
6	RFP	Differential bi-directional RF port. Matched to 50Ω single-ended, 100Ω differential.
7	GND	Ground.
8	VCC_DIG	Voltage supply pin for digital logic circuitry.
9	GND	Ground.
10	VCC_PA	Voltage supply pin for Tx power amplifier.
11	N/C	Not connected.
12	GND	Ground.
13	GND	Ground.
14	GND	Ground.
15	ANT1	Antenna port 1. Match to 50Ω and DC blocked internally.
16	GND	Ground.
17	ANT2	Antenna port 2. Matched to 50Ω and DC blocked internally.
18	GND	Ground.
19	GND	Ground.
20	ANTSEL	Control pin for antenna selection. See logic table.
21	N/C	Not connected.
22	VCC_LNA	Voltage supply pin for Rx low noise amplifier.
23	C_LNA	Control voltage for pin for LNA/bypass modes. See logic table.
24	C_RX_TX	Control voltage pin for Tx/Rx modes. See logic table.

Package Drawing

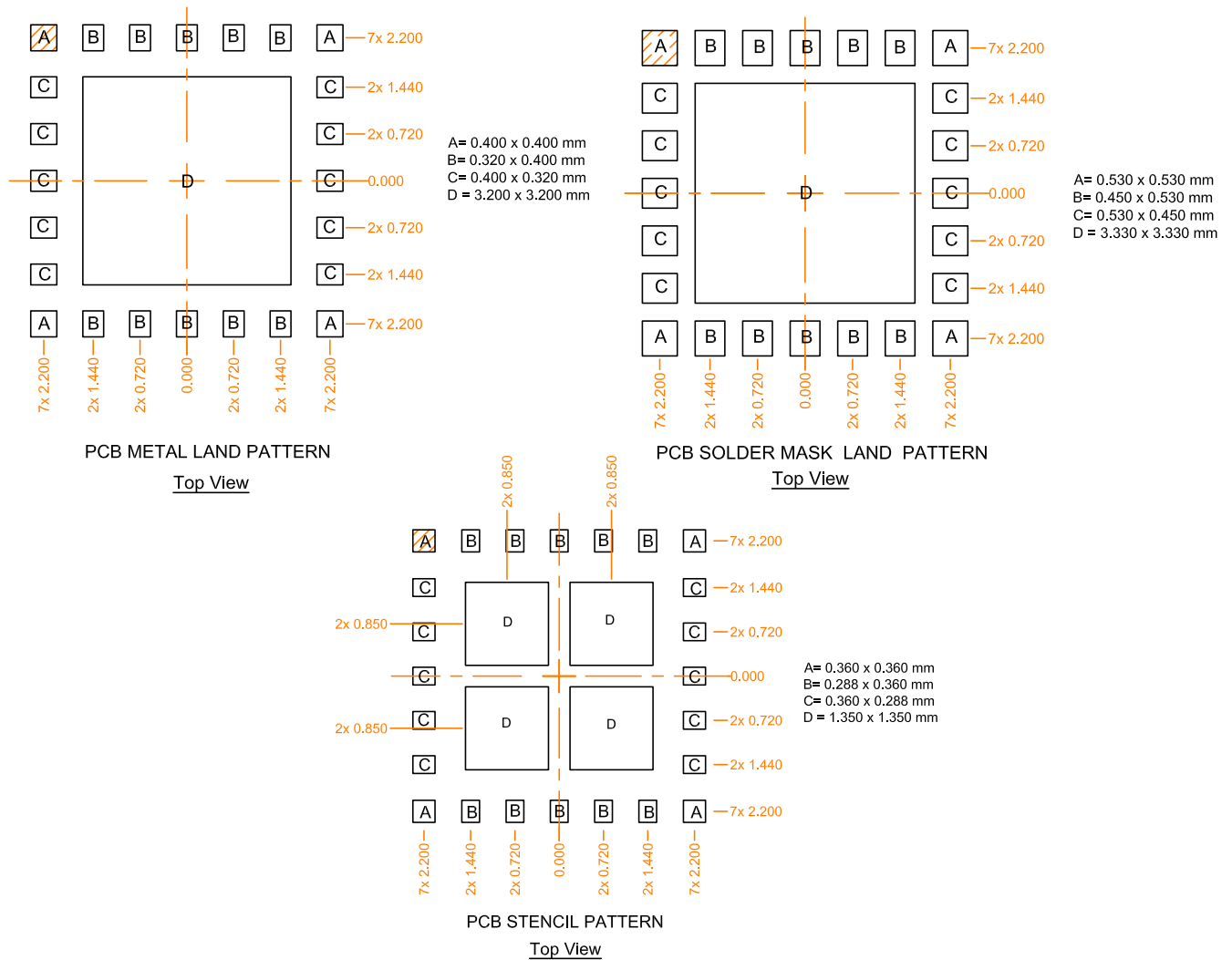


Notes:

1. Shaded area represents Pin 1 location

- A = 0.400 x 0.400 Typ
- B = 0.320 x 0.400 Typ
- C = 0.320 x 0.440 Typ
- D = 0.400 x 0.320 Typ
- E = 0.440 x 0.320 Typ

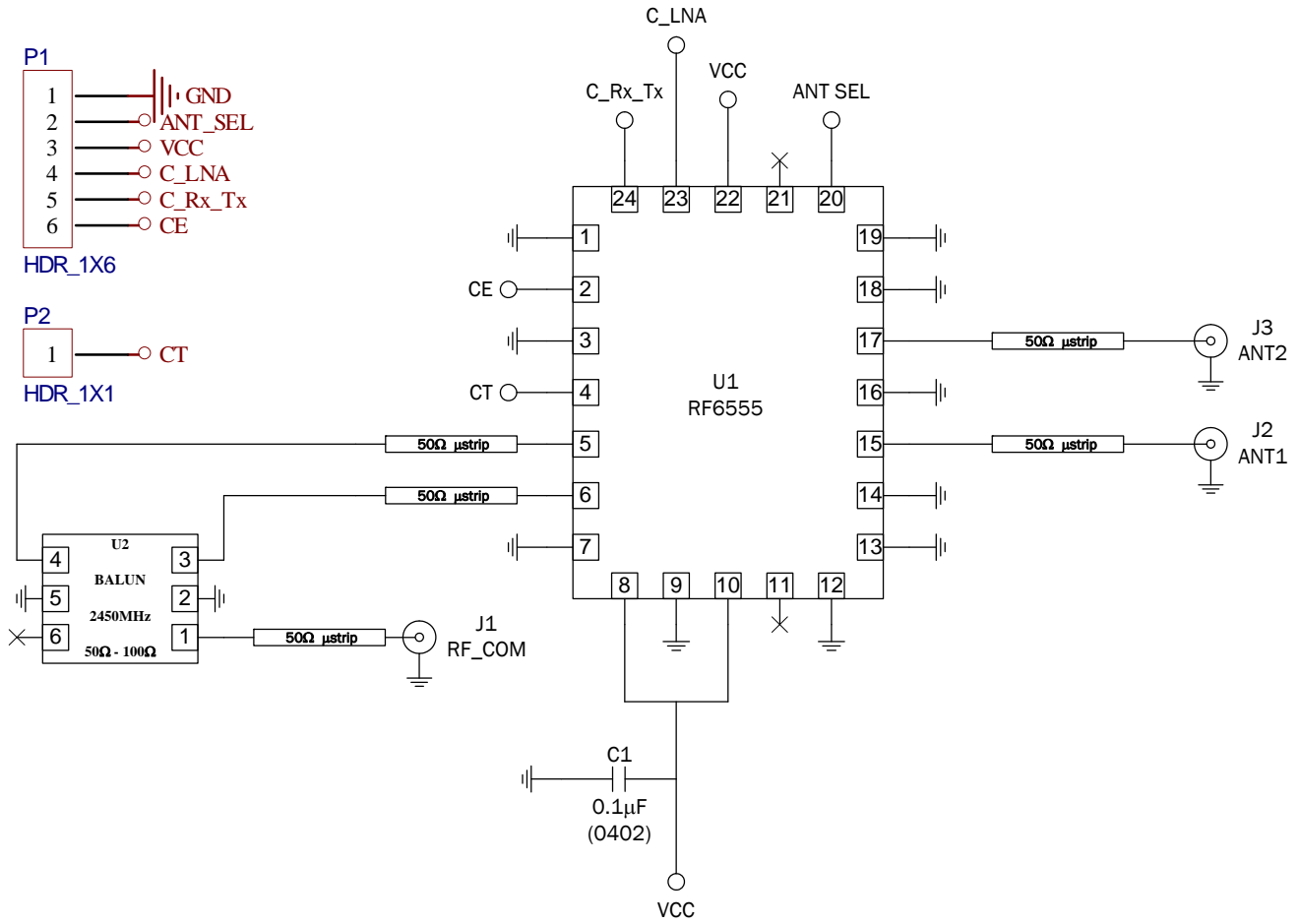
PCB Design Requirements



Notes:
 1. Shaded area represents Pln 1 locallon

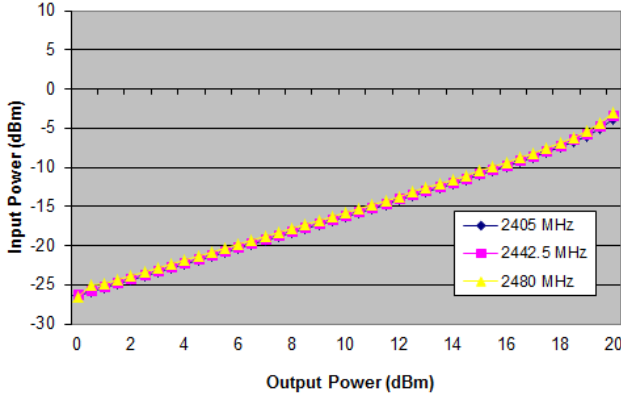
Thermal vias for center slug “D” should be incorporated into the PCB design. The number and size of thermal vias will depend on the application, power dissipation and electrical requirements. Example of the number and size of vias can be found on the RFMD evaluation board layout (gerber files are available upon request).

Evaluation Board Schematic

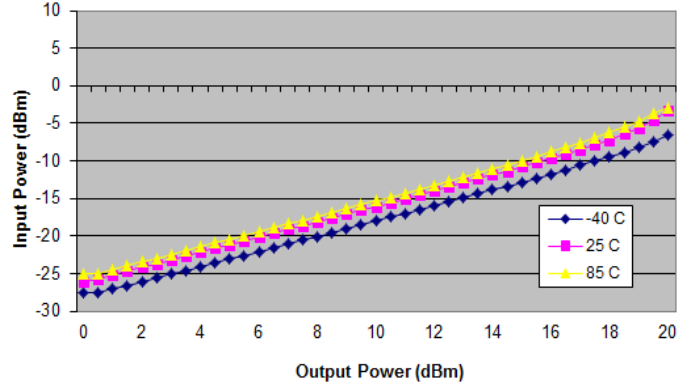


RF6555 2.4 GHz Front End Module

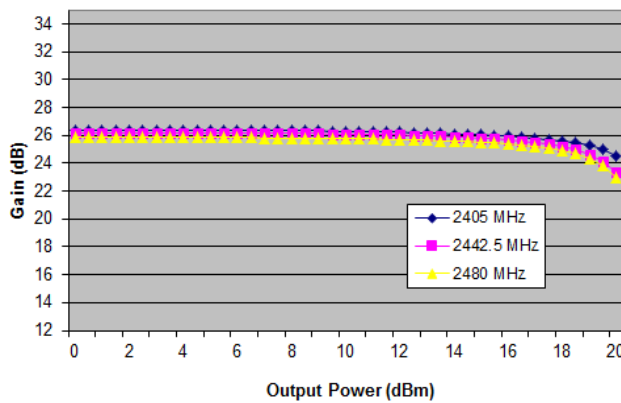
Input Power versus Output Power
Vcc = 3.0V; TX_EN = 3.0V



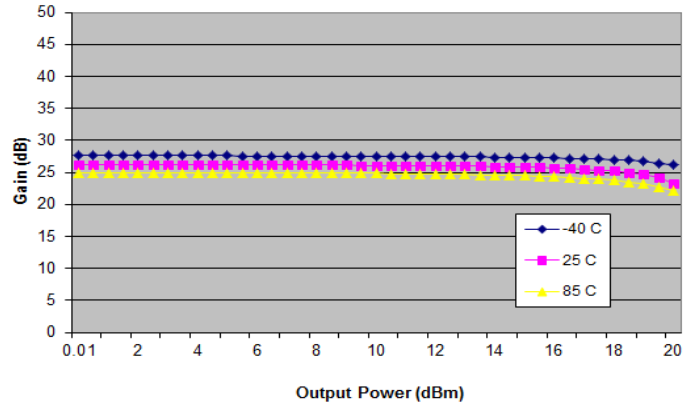
Input Power versus Output Power
(Over Temperature at 2442.5 MHz)
Vcc = 3.0V; TX_EN = 3.0V



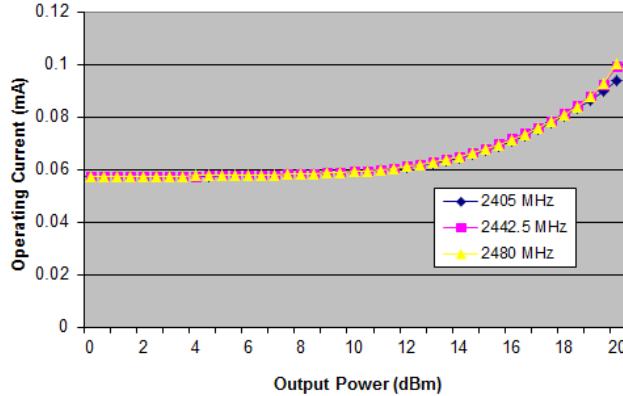
Gain versus Output Power
Vcc = 3.0V; TX_EN = 3.0V



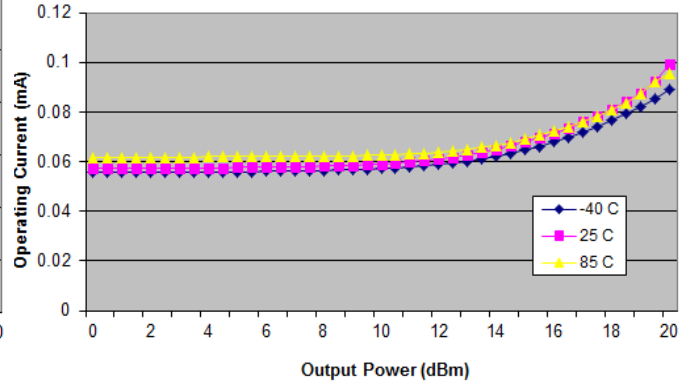
Gain versus Output Power
(Over Temperature at 2442.5 MHz)
Vcc = 3.0V; TX_EN = 3.0V



Operating Current versus Output Power
Vcc = 3.0V; TX_EN = 3.0V



Operating Current versus Output Power
(Over Temperature at 2442.5 MHz)
Vcc = 3.0V; TX_EN = 3.0V



RF6555 Evaluation Board Layout

Board Size 1.5" x 1.5"

Board Thickness 0.032" +/-10%

Board Material FR-4; Multi-Layer

