SPECTRUM DIGITAL INCORPORATED

eZdsp™ F28335

Technical Reference

2007 ***DSP Development Systems***

eZdsp™ F28335
Technical Reference

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About This Manual

This document describes board level operations of the eZdsp™ F28335 based on the Texas Instruments TMS320F28335 Digital Signal Controller (DSC).

The eZdsp™ F28335 is a stand-alone module permitting engineers and software developers evaluation of certain characteristics of the TMS320F28335 DSC to determine processor applicability to design requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The “eZdsp™ F28335” will sometimes be referred to as the “eZdsp”.

“eZdsp” will include the socketed or unsocket version

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320F28335 Digital Signal Controllers Data Manual, literature #SPRS439
Texas Instruments TMS320C28x DSP CPU and Instruction Set Reference Guide, literature #SPRU430
Texas Instruments TMS320C28x Assembly Language Tools Users Guide, literature #SPRU513
Texas Instruments TMS320C28x Optimizing C/C++ Compiler User’s Guide, literature #SPRU514
Texas Instruments Code Composer Studio Getting Started Guide, literature #SPRU509

Table 1: Manual History

Revision	History
A	Production Release
B	Updated Figures, Text, Schematics
C	Updated Figures, Tables, Text

Table 2: Board History

PWB Revision	History
A	Production Release
B	Updated Silk-screen

Chapter 1

Introduction to the eZdsp™ F28335

This chapter provides a description of the eZdsp™ for the TMS320F28335 Digital Signal Controller, key features, and block diagram of the circuit board.

Topic **Page**

1.0 Overview of the eZdsp™ F28335

The eZdsp™ F28335 is a stand-alone card--allowing developers to evaluate the TMS320F28335 digital signal controller (DSC) to determine if it meets their application requirements. Furthermore, the module is an excellent platform to develop and run software for the TMS320F28335 processor.

The eZdsp™ F28335 is shipped with a TMS320F28335 DSC. The eZdsp™ F28335 allows full speed verification of F28335 code. Several expansion connectors are provided for any necessary evaluation circuitry not provided on the as shipped configuration.

To simplify code development and shorten debugging time, a C2000 Code Composer Studio™ driver is provided. In addition, an onboard JTAG connector provides interface to emulators, with assembly language and 'C' high level language debug.

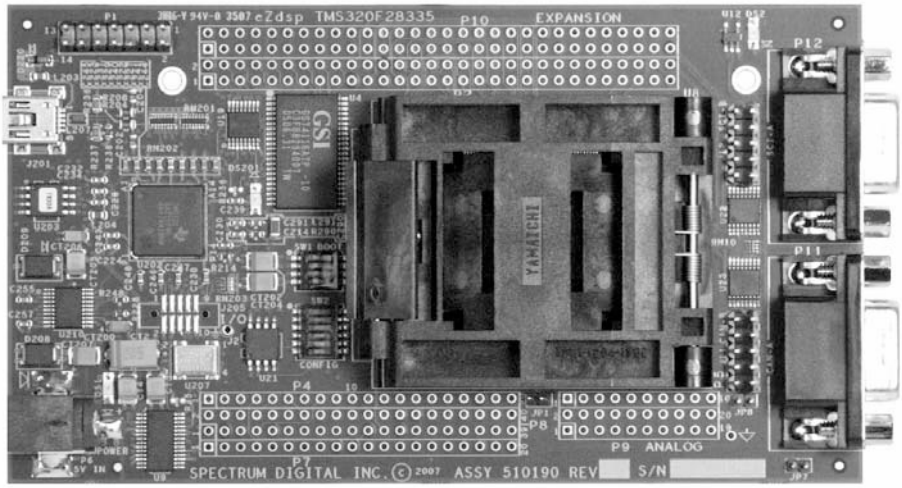

Figure 1-1, eZdsp F28335

1.1 Key Features of the eZdsp™ F28335

1.1.1 Hardware Features

The eZdsp™ F28335 has the following features:

- TMS320F28335 Digital Signal Controller
- 150 Mhz. operating speed
- On chip 32-bit floating point unit
- 68K bytes on-chip RAM
- 512K bytes on-chip Flash memory
- 256K bytes off-chip SRAM memory
- On chip 12 bit Analog to Digital (A/D) converter with 16 input channels
- 30 MHz. input clock
- On board RS-232 connector with line driver
- On board CAN 2.0 interface with line driver and connector
- Multiple Expansion Connectors (analog, I/O)
- On board embedded USB JTAG Controller
- 5-volt only operation with supplied AC adapter
- On board IEEE 1149.1 JTAG emulation connector

1.1.2 Software Features

- TI F28xx Code Composer Studio™ Integrated Development Environment, Version 3.3
- Texas Instruments' Flash APIs to support the F28335
- Texas Instruments' F28335 header files and example software

1.2 Functional Overview of the eZdsp™ F28335

Figure 1-1 shows a block diagram of the basic configuration for the eZdsp™ F28335. The major interfaces of the eZdsp are the JTAG interface, and expansion interface.

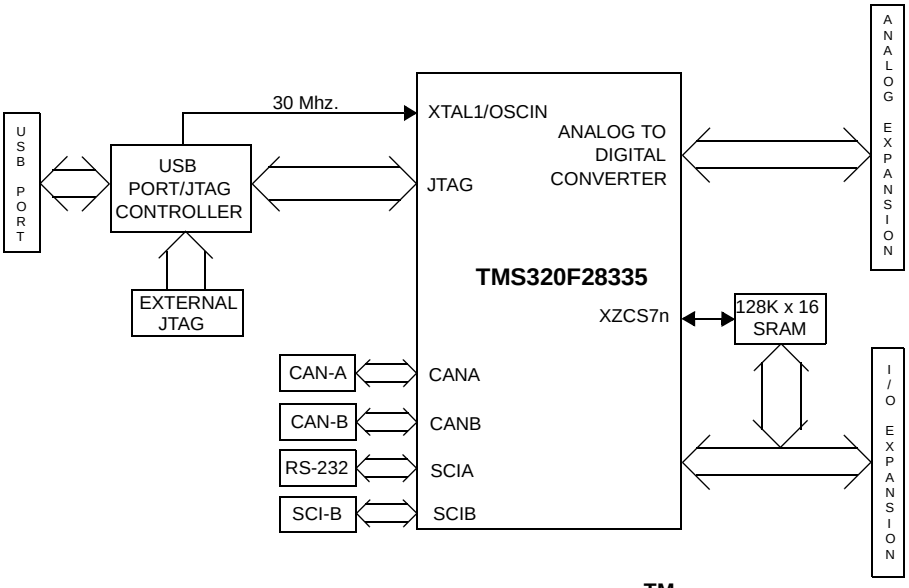

Figure 1-2, BLOCK DIAGRAM eZdsp™ F28335

Chapter 2

Operation of the eZdsp™ F28335

This chapter describes the operation of the eZdsp™ F28335, key interfaces and includes a circuit board outline.

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2.0 The eZdsp™ F28335 Operation

This chapter describes the eZdsp™ F28335, key components, and operation. Information on the eZdsp's various interfaces is also included. The eZdsp™ F28335 consists of four major blocks of logic:

- Analog Interface Connector
- I/O Interface Connector
- On board Memory
- JTAG Interface
- Embedded USB JTAG Controller Interface

2.1 The eZdsp™ F28335 Board

The eZdsp™ F28335 is a 5.35 x 3.0 inch, multi-layered printed circuit board, powered by an external 5-Volt only power supply. Figure 2-1 shows the layout of the top side of the F28335 eZdsp.

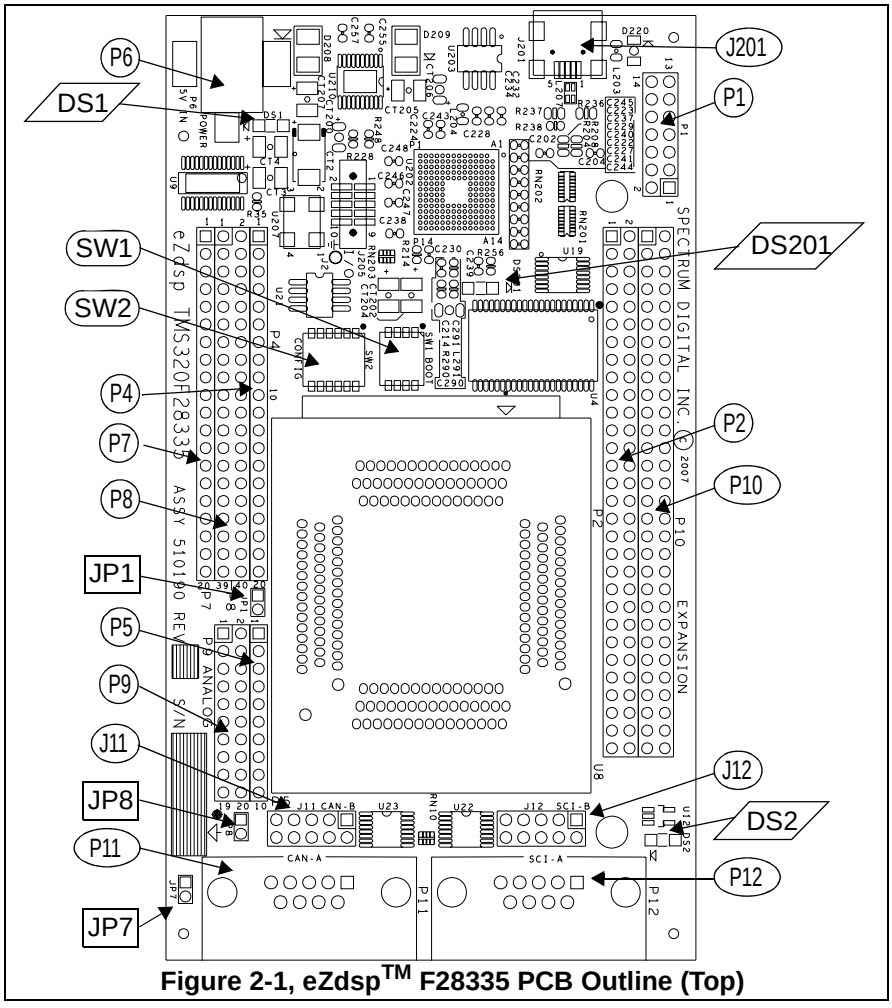

Figure 2-1, eZdsp™ F28335 PCB Outline (Top)

Figure 2-2 shows the layout of the bottom side of the F28335 eZdsp.

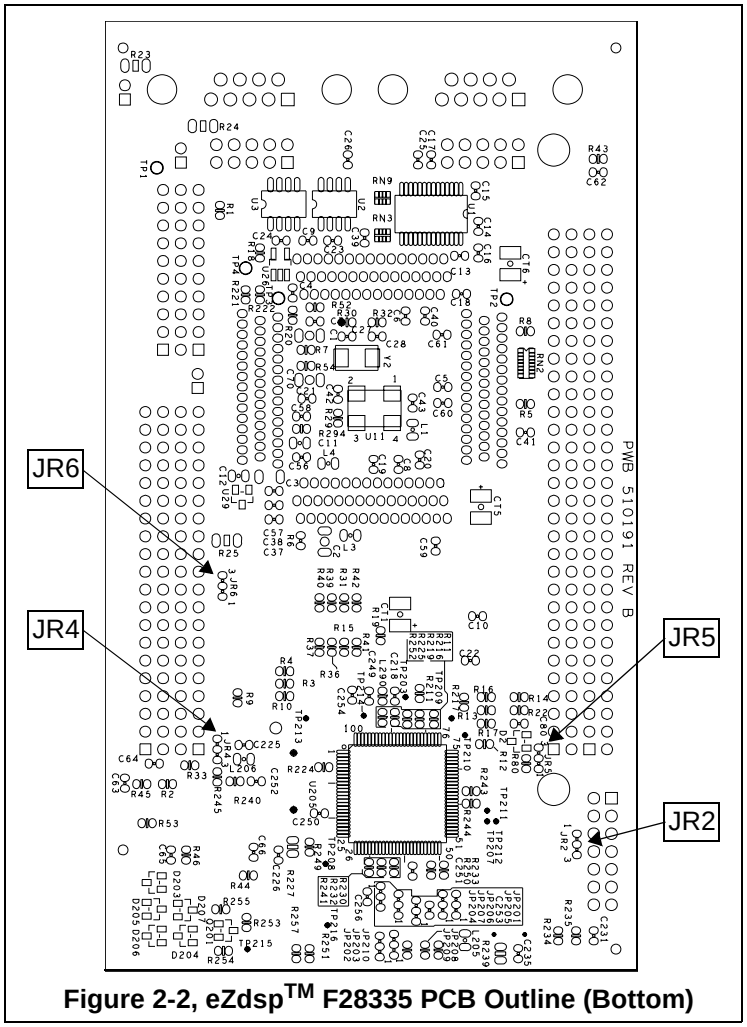

Figure 2-2, eZdsp™ F28335 PCB Outline (Bottom)

2.1.1 Power Connector

The eZdsp™ F28335 is powered by a +5 Volt only power supply, included with the unit. The power is supplied via connector P6. If expansion boards are connected to the eZdsp, a higher amperage power supply may be necessary.

2.2 eZdsp™ F28335 Memory

The eZdsp includes the following on-chip memory:

- 256K x 16 Flash
- 8 blocks of 4K x 16 single access RAM (SARAM)
- 2 blocks of 8K x 16 SARAM
- 2 blocks of 1K x 16 SARAM

In addition 128K x 16 off-chip SRAM is provided. The processor on the eZdsp can be configured for boot-loader mode or non-boot-loader mode.

The eZdsp can load ram for debug or FLASH ROM can be loaded and run. For larger software projects it is suggested to do a initial debug with on eZdsp F28335 module which supports a total RAM environment. With careful attention to the I/O mapping in the software the application code can easily be ported to the F28335.

The table below shows the external chip select signal and its use.

Table 1: External Chip Select and Usage

Chip Select Signal	Use
XZCS0n	Expansion header
XZCS6n	Expansion Header
XZCS7n	External SRAM

2.2.1 Memory Map

The figure below shows the memory map configuration on the eZdsp^{TM} F28335.

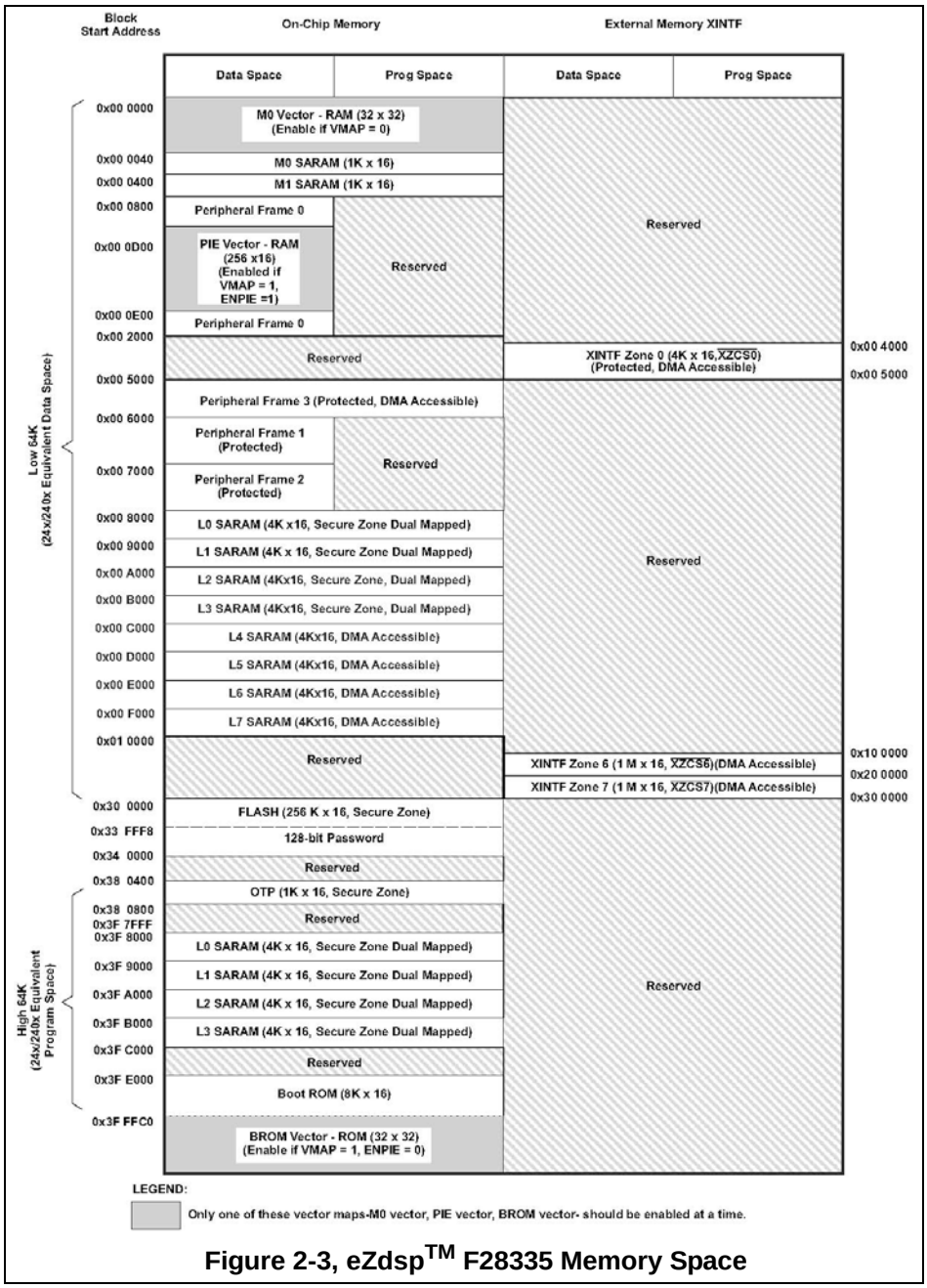

Figure 2-3, eZdsp^{TM} F28335 Memory Space

Note: The on-chip flash memory has a security key which can prevent visibility when enabled.

2.3 eZdsp™ F28335 Connectors

The eZdsp™ F28335 has fourteen connectors. The function of each connector is shown in the table below:

Table 2: eZdsp™ F28335 Connectors

Connector	Function
P1	JTAG Interface
P2	Expansion
P4/P8/P7	I/O Interface
P5/P9	Analog Interface
P6	Power Connector
P10	Expansion
P11	CAN-A
P12	SCI-A
J11	CAN-B
J12	SCI-B
J201	Embedded JTAG

2.3.1 P1, JTAG Interface

The eZdsp™ F28335 is supplied with a 14-pin header interface, P1. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs.

The positions of the 14 pins on the P1 connector are shown in the diagram below as viewed from the top of the eZdsp.

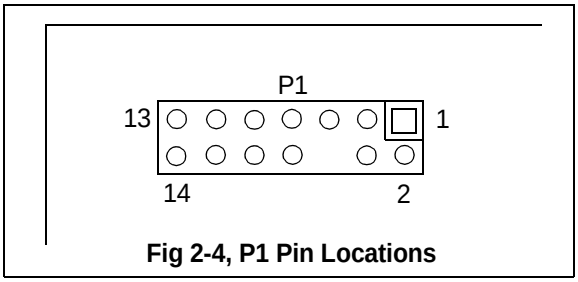

Fig 2-4, P1 Pin Locations

The definition of P1, which has the JTAG signals is shown below.

Table 3: P1, JTAG Interface Connector

Pin #	Signal	Pin #	Signal
1	XTMS	2	XTRST-
3	XTDI	4	GND
5	XTPD (+3.3/5V)	6	**no pin**
7	T_TDO	8	USBSEL
9	T_TCK RET	10	GND
11	XTCK	12	GND
13	T_EMU0	14	T_EMU1

WARNING !

The TMS320F28335 supports +3.3V Input/Output levels which are NOT +5V tolerant. Connecting the eZdsp to a system with +5V Input/Output levels will damage the TMS320F28335. If the eZdsp is connected to another target then the eZdsp must be powered up first and powered down last to prevent lactchup conditions.

2.3.2 P2, Expansion Interface

The positions of the 60 pins on the P2 connector are shown in the figure below.

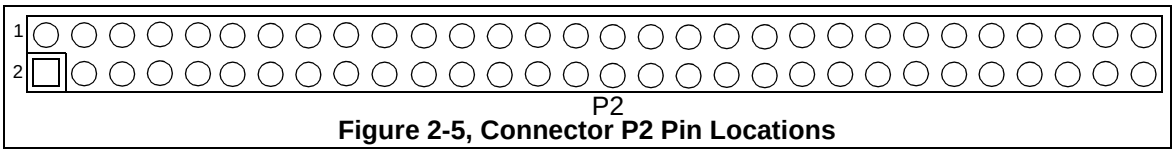

Figure 2-5, Connector P2 Pin Locations

The definition of P2, which has the I/O signal interface is shown below.

Table 4: P2, Expansion Interface Connector

Pin #	Signal	Pin #	Signal
1	+3.3V/+5V/NC *	2	+3.3/+5V/NC *
3	GPIO79_XD0	4	GPIO78_XD1
5	GPIO77_XD2	6	GPIO76_XD3
7	GPIO75_XD4	8	GPIO74_XD5
9	GPIO73_XD6	10	GPIO72_XD7
11	GPIO71_XD8	12	GPIO70_XD9
13	GPIO69_XD10	14	GPIO68_XD11
15	GPIO67_XD12	16	GPIO66_XD13
17	GPIO65_XD14	18	GPIO64_XD15
19	GPIO40_XA0_XWE1n	20	GPIO41_XA1
21	GPIO42_XA2	22	GPIO43_XA3
23	GPIO44_XA4	24	GPIO45_XA5
25	GPIO46_XA6	26	GPIO47_XA7
27	GPIO80_XA8	28	GPIO81_XA9
29	GPIO82_XA10	30	GPIO83_XA11
31	GPIO84_XA12	32	GPIO85_XA13
33	GPIO86_XA14	34	GPIO87_XA15
35	GND	36	GND
37	GPIO36_SCIRXDA-XZCS0n	38	GPIO37_ECAP2_XZCS7n
39	GPIO34_ECAP1_XREADY	40	B_GPIO28_SCIRXDA_XZCS6n
41	GPIO35_SCIRXDA_XRNW	42	10K Pull-up
43	GPIO38_WE0n	44	XRDn
45	+3.3V	46	No connect
47	DSP_RSn	48	XCLKOUT
49	GND	50	GND
51	GND	52	GND
53	GPIO39_XA16	54	GPIO31_CANTXA_XA17
55	GPIO30_CANRXA_XA18	56	GPIO14_TZ3n_XHOLDn_SCITXB_MCLKXB
57	GPIO15_XHOLDAn_SCIRXDB_MFSXB	58	GPIO29_SCITXDA_XA19
59	No connect	60	No connect

* Default is No Connect (NC). User can jumper to +3.3V or +5V on backside of eZdsp with JR5.

2.3.3 P4/P8/P7, I/O Interface

The connectors P4, P8, and P7 present the I/O signals from the DSC. The layout of these connectors are shown below.

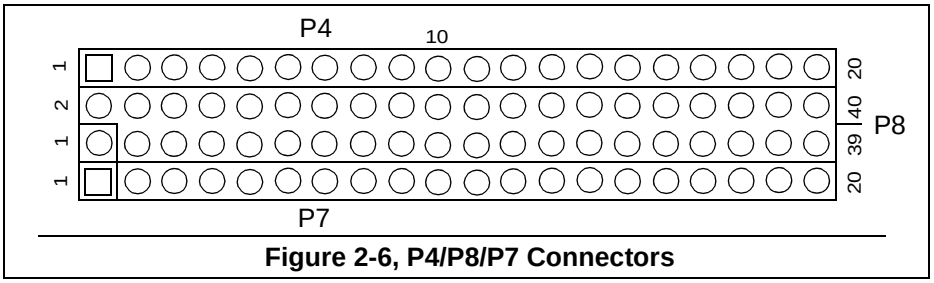

Figure 2-6, P4/P8/P7 Connectors

The pin definition of the P4 connector is shown in the table below.

Table 5: P4, I/O Connectors

Pin #	Signal
1	+3.3V/+5V/NC *
2	No connect
3	GPIO22_EQEP1S_MCLKRA_SCITXDB
4	GPIO7_EPWM4B_MCLKRA_ECAP2
5	GPIO23_EQEP1_MFSXA_SCIRXDB
6	GPIO5_EPWM3B_MFSRA_ECAP1
7	GPIO20_EAEP1A_MXDA_CANTXB
8	GPIO21_EQEP1B_MDRA_CANRXB
9	No connect
10	GND
11	GPIO3_EPWM2B_ECAP5_MCLKRB
12	GPIO1_EPWM1B/ECAP6/MFSRB
13	No connect
14	No connect
15	No connect
16	No connect
17	No connect
18	GPIO14_TZ3n_XHOLD_SCITXDB_MCLKXB
19	GPIO15_TZ4n_XHOLDA_SCIRXDB_MFSXB
20	GND

The pin definition of the P8 connector is shown in the table below.

Table 6: P8, I/O Connectors

Pin #	Signal	Pin #	Signal
1	+3.3V/+5V/NC *	2	+3.3V/+5V/NC *
3	MUX_GPIO29_SCITXDA_XA19	4	MUX_GPIO28_SCIRXDA_XZCS6n
5	GPIO14_TZ3n_XHOLD_SCITXDB_MCLKXB	6	GPIO20_EAEP1A_MXDA_CANTXB
7	GPIO21_EQEP18_MDRA_CANRXB	8	GPIO23_EQEP1_MFSXA_SCIRXDB
9	GPIO0_EPWM1A	10	GPIO1_EPWM1B/ECAP6/MFSRB
11	GPIO2_EPWM2A	12	GPIO3_EPWM2B_ECAP5_MCLKRB
13	GPIO4_EPWM3A	14	GPIO5_EPWM3B_MFSRA_ECAP1
15	GPIO27_ECAP4_EQEP2S_MFSXB	16	GPIO6_EPWMN4A_EPWMSYNCI/EPWMSYNCO
17	GPIO13_TZ2N_CANRXB_MDRB	18	GPIO34_ECAP1_XREADY
19	GND	20	GND
21	GPIO7_EPWM4B_MCLKRA_ECAP2	22	GPIO15TZ4n_XHOLDA_SCIRXDB_MFSXB
23	GPIO16_SPISIMOA_CANTXB_TZ5n	24	GPIO17_SPISOMIA_CANRXB_TZ6n
25	GPIO18_SPICLKA_SCITXDB_CANRXA	26	GPIO19_SPISTAn_SCIRXDB_CANTXA
27	_MUX_GPIO31_CANRXA_XA17	28	MUX_GPIO30_CANRXA_XA18
29	MUX_GPIO11_EPWM6B_SCIRXDB_ECAP4	30	MUX_GPIO8EPWM5A_CANTXB_ADCSOCA0nP3
31	MUX_GPIO9_EPWM5B_SCITXDB_ECAP3	32	MUX_GPIO10_EPWM6A_CANRXB_ADCASOCB0n
33	MUX_GPIO22	34	GPIO25_ECAP2_EPEQ2B_MDRB
35	GPIO26_ECAP3_EQEP21_MCLKXB	36	GPIO32_SDAA_EPWMSYNCI_ADCSOCAOn
37	GPIO12_TZ1N_CANTXB_MDXB	38	GPIO33_SCLA_EPWNSYNCVO_ADCSOCBOn
39	GND	40	GND

* Default is No Connect (NC). User can jumper to +3.3V or +5V on backside of eZdsp with JR4.

The P7 connector is supplied for backwards compatibility. Signals from other connectors can be wired to this connector to support existing user interfaces. The pin definition of P7 connector is shown in the table below.

Table 7: P7, I/O Connector

Pin #	Signal	Pin #	Signal
1	No connect	11	No connect
2	No connect	12	No connect
3	No connect	13	No connect
4	No connect	14	No connect
5	No connect	15	No connect
6	No connect	16	No connect
7	No connect	17	No connect
8	No connect	18	No connect
9	No connect	19	No connect
10	No connect	20	GND

2.3.4 P5/P9, Analog Interface

The position of the 30 pins on the P5/P9 connectors are shown in the diagram below as viewed from the top of the eZdsp.

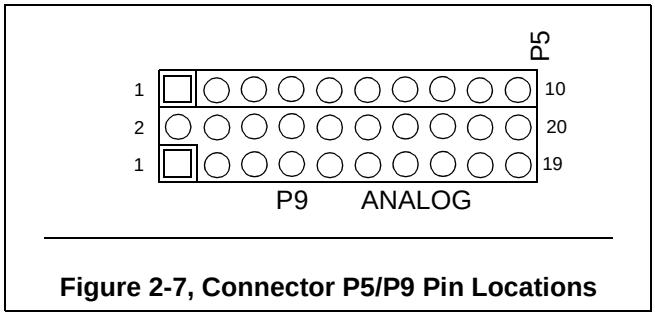

Figure 2-7, Connector P5/P9 Pin Locations

The definition of P5/P9 signals are shown in the table below.

Table 8: P5/P9, Analog Interface Connector

P5 Pin #	Signal	P9 Pin #	Signal	P9 Pin #	Signal
1	ADCINB0	1	GND	2	ADCINA0
2	ADCINB1	3	GND	4	ADCINA1
3	ADCINB2	5	GND	6	ADCINA2
4	ADCINB3	7	GND	8	ADCINA3
5	ADCINB4	9	GND	10	ADCINA4
6	ADCINB5	11	GND	12	ADCINA5
7	ADCINB6	13	GND	14	ADCINA6
8	ADCINB7	15	GND	16	ADCINA7
9	ADCREFM	17	GND	18	ADCLO *
10	ADCREFP	19	GND	20	No connect

* Connect ADCLO to AGND or ADCLO of target system for proper ADC operation.

2.3.5 P6, Power Connector

Power (5 volts) is brought onto the eZdsp^{TM} F28335 via the P6 connector. The connector has an outside diameter of 5.5 mm. and an inside diameter of 2.5 mm. The position of the P6 connector is shown below.

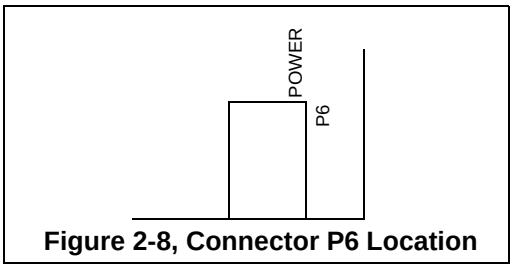

Figure 2-8, Connector P6 Location

The diagram of P6, which has the input power is shown below.

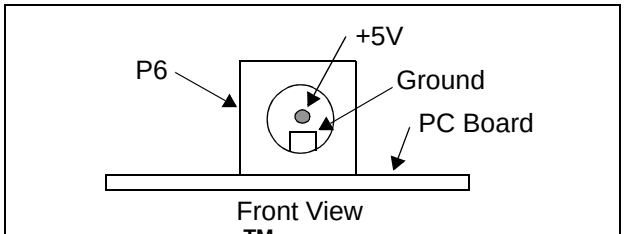

Figure 2-9, eZdsp^{TM} F28335 Power Connector

2.3.6 P10, Expansion Interface

The positions of the 60 pins on the P10 connector are shown in the figure below.

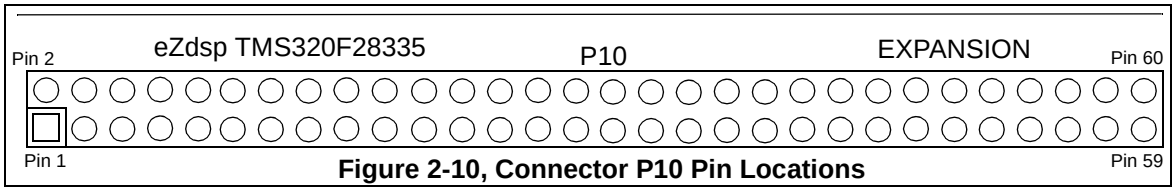

Figure 2-10, Connector P10 Pin Locations

The definition of P10, which has the I/O signal interface is shown below.

Table 9: P10, Expansion Interface Connector

Pin #	Signal	Pin #	Signal
1	+3.3V/+5V/NC	2	+3.3V/+5V/NC
3	GPIO63_SCITXDC_XD16	4	GPIO62_SCIRXDC_XD17
5	GPIO61_MFSRB_XD18	6	GPIO60_MCLKRB_XD19
7	GPIO59_MFSRA_XD20	8	GPIO58_MCLKRA_XD21
9	GPIO57_SPISTEAn_XD22	10	GPIO56_SPICLKA_XD23
11	GPIO55_SPISOMIA_XD24	12	GPIO54_SPISIMOA_XD25
13	GPIO53EQEP1_XD26	14	GPIO52_EQEP1S_XD27
15	GPIO51_EAEP1B_XD28	16	GPIO50_EQEP1A_XD29
17	GPIO49_ECAP6_XD30	18	GPIO48_ECAP5_XD31
19	No connect	20	No Connect
21	No connect	22	No Connect
23	No connect	24	No Connect
25	No connect	26	No Connect
27	No connect	28	No Connect
29	No connect	30	No Connect
31	No connect	32	No Connect
33	No connect	34	No Connect
35	No connect	36	No Connect
37	No connect	38	No Connect
39	No connect	40	No Connect
41	No connect	42	No Connect
43	No connect	44	No Connect
45	No connect	46	No Connect
47	No connect	48	No Connect
49	No connect	50	No Connect
51	No connect	52	No Connect
53	No connect	54	No Connect
55	No connect	56	No Connect
57	No connect	58	No Connect
59	GND	60	GND

2.3.7 P11, CANA Connector

The eZdsp F28335 has a 9 Pin female D-connector which brings out the CANA transmit and receive signals. This CAN interface uses the SN65HVD235 CAN driver. The pin positions for the P11 connector as viewed from the edge of the printed circuit shown below.

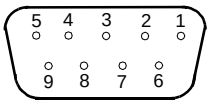

Figure 2-11, P11, DB9 CANA Female Connector

The pin numbers and their corresponding signals are shown in the table below.

Table 10: P11, CANA Pinout

Pin #	Signal Name
1	No Connect
2	CANLA
3	GND
4	No Connect
5	No Connect
6	No Connect
7	CANHA
8	No Connect
9	No Connect

2.3.8 P12, RS-232 Connector

The eZdsp F28335 has an RS-232 connector which brings out the SCIA transmit and receive signals to be used as UART. This UART uses the MAX3238 RS-232 line driver and is routed to a male 9 pin D-connector, P12. The pin positions for the P10 connector as viewed from the edge of the printed circuit board are shown below.

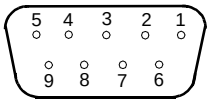

Figure 2-12, P12, DB9 RS-232 Female Connector

The pin numbers and their corresponding signals are shown in the table below. This corresponds to a standard dual row to DB-9 connector interface used on personal computers.

Table 11: P12, RS-232 Pinout

Pin #	Signal Name	Direction
1	No Connect	
2	PCRXDA	Out
3	PCTXDA	In
4	No Connect	
5	GND	N/A
6	No Connect	
7	No Connect	
8	No Connect	
9	No Connect	

2.3.9 J11, CANB 5 x 2 Header

The CANB signals are routed through the SN65HVD235 CAN driver to a 5 x 2 double row header, J11. The pin numbers for J11 and their corresponding signals are shown in the table below.

Table 12: J11, 5 x 2 Pinout

Pin #	Signal Name	Pin #	Signal Name
1	No Connect	2	No Connect
3	CANLB	4	CANHB
5	GND	6	No Connect
7	No Connect	8	No Connect
9	No Connect	10	No Connect

The location of the pins are shown in the figure below.

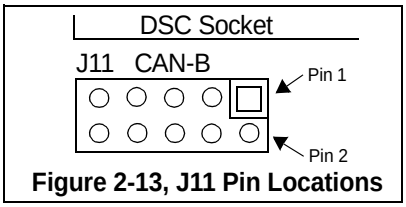

Figure 2-13, J11 Pin Locations

2.3.10 J12, SCIB 5 x 2 Header

The SCIB signals are routed through the MAX3238 line driver to a 5 x 2 double row header, J10. The pin numbers for J12 and their corresponding signals are shown in the table below.

Table 13: J12, 5 x 2 Pinout

Pin #	Signal Name	Direction	Pin #	Signal Name	Direction
1	No Connect		2	No Connect	
3	PCRXDB	Out	4	No Connect	
5	PCTXDB	In	6	No Connect	
7	No Connect		8	No Connect	
9	GND	N/A	10	No Connect	

The location of the pins are shown in the figure below.

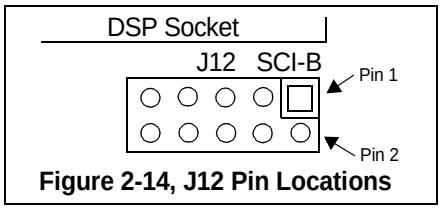

Figure 2-14, J12 Pin Locations

2.3.11 J201, Embedded USB JTAG Interface

The USB connector J201 is used to connect to the host development system which is running the software development suite. The signals on this connector are shown in the table below.

Table 14: J201, Embedded USB JTAG Interface

Pin #	Signal Name
1	USBVDD
2	D-
3	D+
4	NC
5	USBVSS

2.3.12 Connector Part Numbers

The table below shows the part numbers for connectors which can be used on the eZdsp™ F28335. Part numbers from other manufacturers may also be used.

Table 15: eZdsp™ F28335 Suggested Connector Part Numbers

Connector	Male Part Numbers	Female Part Numbers
P1	SAMTEC TSW-1-10-07-G-T	SAMTEC SSW-1-10-01-G-T
P2	SAMTEC TSW-1-20-07-G-T	SAMTEC SSW-1-20-01-G-T

*SSW or SSQ Series can be used

2.4 eZdsp™ F28335 Jumpers

The eZdsp™ F28335 has 7 jumpers available to the user which determine how features on the eZdsp™ F28335 are utilized. The table below lists the jumpers and their function. The following sections describe the use of each jumper.

Table 16: eZdsp™ F28335 Jumpers

Jumper #	Size	Function	Position As Shipped From Factory
JP1	1 x 2	U29, Pin 2 to ADCREFIN	Installed
JR2	1 x 3	+3.3/5V to XTPD	+3.3 volts
JR4	1 x 3	+5/3.3V to P4, P8	Not populated
JR5	1 x 3	+5/3.3V to P2, P10	Not populated
JR6	1 x 3	MUX GPIO22_24 Select	GPIO24
JP7	1 x 2	CANA Terminator Resistor	Installed
JP8	1 x 2	CANB Terminator Resistor	Installed

2.4.1 JP1, ADCREFIN Select

Jumper JP1 is used to connect the output of U29, REF3020 to ADCREFIN. When the jumper is shorted the +2.048 voltage level is routed to the ADCREFIN signal of the DSC. When the jumper is open the ADCREFIN floats.The positions are shown in the table below.

Table 17: JP1, U29, Pin 2 to ADCREFIN Select

Position	Function
Shorted *	Output of U29 (+2.048V) connected to ADCREFIN
Open	Use internal reference for ADCREFIN

* as shipped from factory

The layout of this jumper is shown in the figure below.

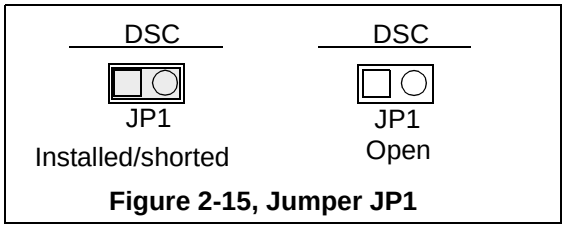

Figure 2-15, Jumper JP1

2.4.2 JR2, XTPD Voltage Select

Jumper JR2 is a surface mount jumper located on the bottom side of the board. To use a configuration a zero ohm resistor should be used for shorting. This jumper is used to select either +3.3 or +5 volts to be touted to the XTPD pin on the external JTAG header P1, pin 5. In configuration A, +5 volts is routed to XTPD. When configuration B is selected +3.3 volts is routed to XTPD. This is shown below.

Table 18: JR2, XTPD Voltage Select

Configuration	Function
A *	+5 volts routed to XTPD
B	+3.3 volts routed to XTPD

* default

The layout of this jumper is shown in the figure below.

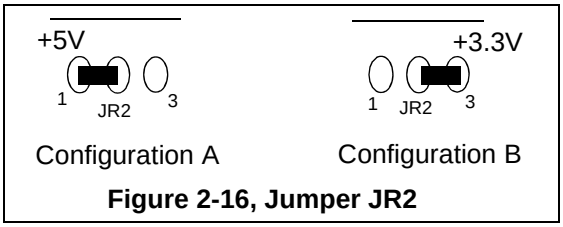

Figure 2-16, Jumper JR2

2.4.3 JR4, Connector P4, P8 Voltage Select

Jumper JR4 is a surface mount jumper located on the bottom side of the board. To use a configuration a zero ohm resistor should be used for shorting. This jumper allows the user to bring +5 or +3.3 volts to connector P4, pin1, and connector P8, pins 1 and 2. When configuration A is used +5 volts is brought to the connectors. Configuration B routes +3.3 volts to these connectors. These settings are shown below.

Table 19: JR4, Connector P4, P8 Voltage Select

Configuration	Function
A	+5 volts routed to P2, pins 1, P8, pins 1,2
B	+3.3 volts routed to P2, pins 1, P8, pins 1,2

The layout of this jumper is shown in the figure below.

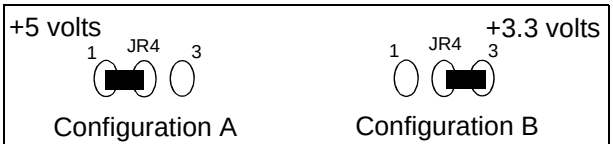

Figure 2-17, Jumper JR4

2.4.4 JR5, Connector P2, P10 Voltage Select

Jumper JR5 is a surface mount jumper located on the bottom side of the board. To use a configuration a zero ohm resistor should be used for shorting. This jumper allows the user to bring +5 or +3.3 volts to connector P2, pin1 and 2, and connector P10, pins 1 and 2. When configuration A is used +5 volts is brought to the connectors. Configuration B routes +3.3 volts to these connectors. These settings are shown below.

Table 20: JR5, Connector P2, P10 Voltage Select

Configuration	Function
A	+5 volts routed to P2, pins 1,2, P10, pins 1,2
B	+3.3 volts routed to P2, pins 1,2, P10, pins 1,2

The layout of this jumper is shown in the figure below.

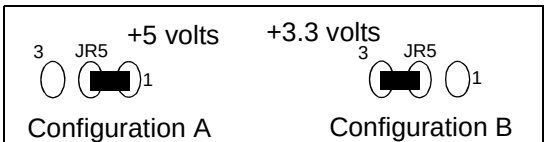

Figure 2-18, Jumper JR5

2.4.5 JR6, MUX GPIO22_24 Select

Jumper JR6 is a surface mount jumper located on the bottom side of the board. To use a configuration a zero ohm resistor should be used for shorting. This jumper is used to route the signal GPIO22 or GPIO24 to connector P8, pin 33 (MUX GPIO22). In configuration A GPIO22 is selected. When configuration B is used GPIO24 is selected. These configurations are shown below.

Table 21: JR6, MUX GPIO22 Select

Configuration	Function
A	GPIO22 routed to MUX GPIO22_24
B *	GPIO24 routed to MUX GPIO22_24

* as shipped from factory

The layout of this jumper is shown in the figure below.

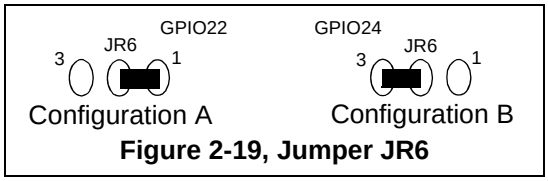

Figure 2-19, Jumper JR6

2.4.6 JP7, CANA Termination Resistor Select

Jumper JP7 is used to select the termination resistor on the CANA interface. When installed a termination resistor is placed between pins 2 and 7 of the connector P7. This jumper is installed at the factory. The positions are shown in the table below.

Table 22: JP7, CANA Termination Resistor Select

Configuration	Function
Installed/shorted	Termination resistor installed
Open	Termination resistor NOT resistor installed

The layout of this jumper is shown in the figure below.

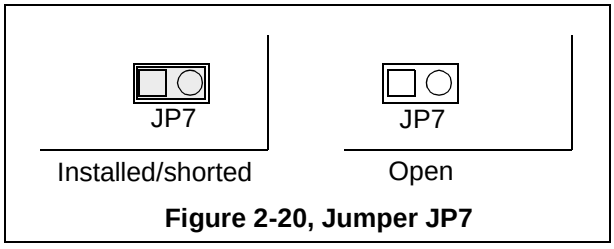

Figure 2-20, Jumper JP7

2.4.7 JP8, CANB Termination Resistor Select

Jumper JP8 is used to select the termination resistor on the CANB interface. When installed a termination resistor is placed between pins 3 and 4 of the connector J11. This jumper is installed at the factory. The positions are shown in the table below.

Table 23: JP8, CANB Termination Resistor Select

Configuration	Function
Installed/shorted	Termination resistor installed
Open	Termination resistor NOT resistor installed

The layout of this jumper is shown in the figure below.

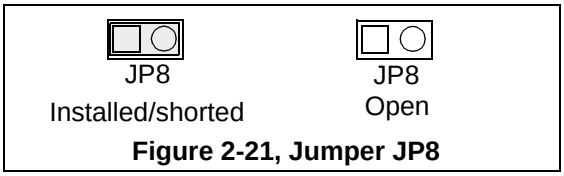

Figure 2-21, Jumper JP8

2.5 LEDs

The eZdsp^{TM} F28335 has three light-emitting diodes. DS1 indicates the presence of +5 volts and is normally ‘on’ when power is applied to the board. LED DS2 is under control of the GPIO32 line from the processor. DS201 is connected to the embedded USB emulator and shows the status of the emulation link. These are shown in the table below.

Table 24: LEDs

LED #	Color	Controlling Signal
DS1	Green	+5 Volts
DS2	Green	GPIO32
DS201	Green	Embedded emulation link status

2.6 Switches

The eZdsp™ F28335 has two switches. SW1 is used to select the power on boot load options. SW2 is used to select the processor configuration.

2.6.1 SW1, Boot Load Option Switch

Switch SW1 is used to select the boot load option used by the F28335 processor on power up. These selections are shown in the table below.

Table 25: SW1, Boot Load Option Switch

PIN	Position 4 Boot-3 XA15	Position 3 Boot-2 XA14	Position 2 Boot-1 XA13	Position 1 Boot-0 XA12	Boot Mode
1111	OFF	OFF	OFF	OFF	Jump to Flash
1110	OFF	OFF	OFF	ON	SCI-A boot
1101	OFF	OFF	ON	OFF	SPI-A boot *
1100	OFF	OFF	ON	ON	I^2C-A boot
1011	OFF	ON	OFF	OFF	eCAN-A boot
1010	OFF	ON	OFF	ON	McBSP-A boot
1001	OFF	ON	ON	OFF	Jump to XINTX x16
1000	OFF	ON	ON	ON	Jump to XINTX x32
0111	ON	OFF	OFF	OFF	Jump to OTP
0110	ON	OFF	OFF	ON	Parallel GPIO I/O boot
0101	ON	OFF	ON	OFF	Parallel XINTF boot
0100	ON	OFF	ON	ON	Jump to SARAM
0011	ON	ON	OFF	OFF	Branch to check boot mode
0010	ON	ON	OFF	ON	Branch to Flash, skip ADC CAL
0001	ON	ON	ON	OFF	Branch to SARAM, skip ADC CAL
0000	ON	ON	ON	ON	Branch to SCI, skip ADC CAL

* As shipped from the factory.

The figure below shows the layout of SW1.

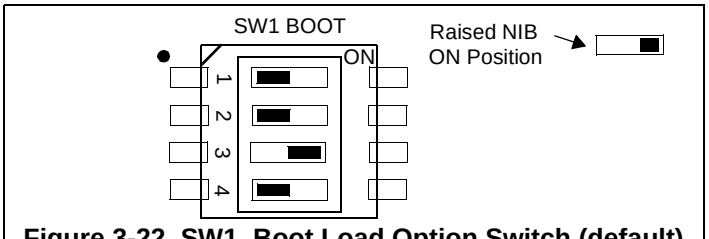

Figure 3-22, SW1, Boot Load Option Switch (default)

2.6.1 SW2, Processor Configuration Switch

Switch SW2 is used to select the processor configuration. The eZdsp™ F28335 supports 2 on board SCI ports and 2 on board CAN ports. These ports can be used on board or routed to expansion connectors. Switch SW2 controls this configuration. These selections are shown in the table below.

Table 26: SW2, Processor Configuration Switch

Position	State	Value	Function
1	OFF	1	Select GPIO28, GPIO29, GPIO30, GPIO31 as expansion
1	ON *	0	Select GPIO28, GPIO29, GPIO30, GPIO31 as on board SCI/CAN A
2	OFF	1	Disable MUX U22
2	ON *	0	Enable MUX U22
3	OFF	1	Select GPIO8, GPIO9, GPIO10, GPIO11 as expansion
3	ON *	0	Select GPIO8, GPIO9, GPIO10, GPIO11 as on board SCI/CAN B
4	OFF	1	Disable MUX U23
4	ON *	0	Enable MUX U23
5	OFF	1	Write protect I^2C EEPROM
5	ON *	0	Enable Writes to I^2C EEPROM
6	OFF	1	I^2C EEPROM lowest address is 1
6	ON *	0	I^2C EEPROM lowest address is 0

* default

The figure below shows the layout of SW2.

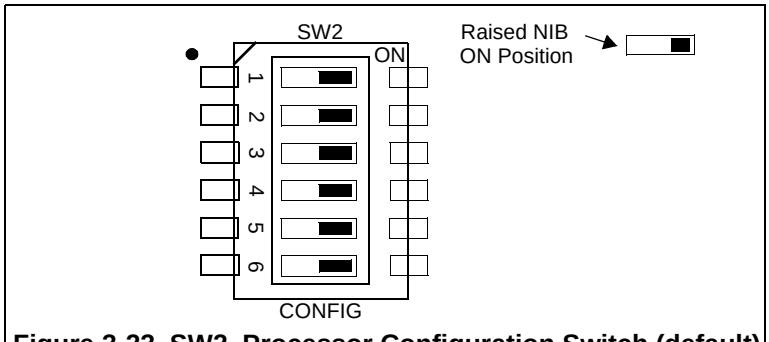

Figure 3-23, SW2, Processor Configuration Switch (default)

2.7 Test Points

The eZdsp™ F28335 has fifteen test points. Their location on the bottom of the board are shown in the figure below.

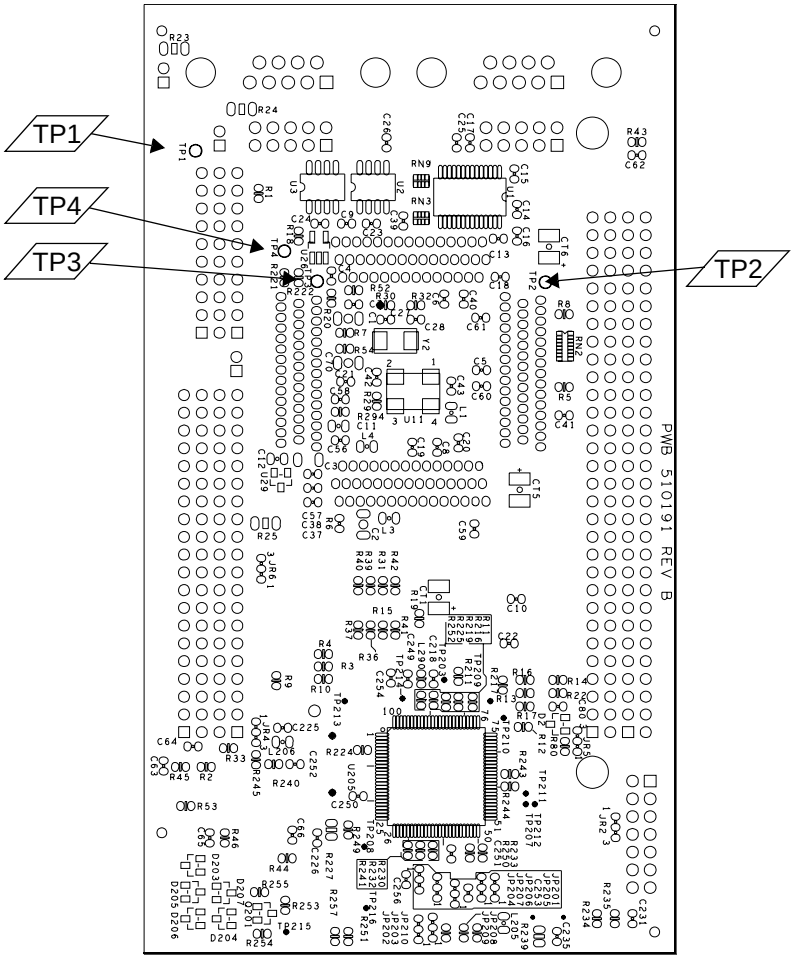

Figure 2-24, eZdsp™ F28335 Test Points (Bottom)

The signals each test point is tied to is listed in the table below.

Table 27: Test Points

Test Point	Signal
TP1	AGND
TP2	XCLKOUT
TP3	U8(DSP) Pin 81, TEST1
TP4	U8(DSP) Pin 82, TEST2

Appendix A

eZdsp™ F28335 Schematics

The schematics for the eZdsp™ F28335 can be found on the CD-ROM that accompanies this board. The schematics were drawn on ORCAD.

The schematics are correct for both the socketed and unsocketed version of the eZdsp™.

WARNING !

The TMS320F28335 supports +3.3V Input/Output levels which are NOT +5V tolerant. Connecting the eZdsp to a system with +5V Input/Output levels will damage the TMS320F28335. If the eZdsp is connected to another target then the eZdsp must be powered up first and powered down last to prevent lactchup conditions.

Design Notes:

1. The TMS320F28335 X1/CLKIN pin is +1.8 volt input. The clock input is buffered with a SN74LVC1G14 whose supply is +1.8 volts. This provides +3.3 volts to the +1.8 volt clock translation. Refer to sheet 4 of the schematics.

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ALPHA RELEASE	29-July-2007	
B	PRODUCTION RELEASE	15-Sept-2007	

SCHEMATIC CONTENTS

SHEET01 - TITLE PAGE
SHEET02 - TMS320F28335 DSP
SHEET03 - DSP DECOUPLING CAPS
SHEET04 - BOOT SWITCHES,OSC
SHEET05 - MEMORY
SHEET06 - I/O MULTIPLEXING
SHEET07 - CAN, RS232
SHEET08 - EMIF EXPANSION
SHEET09 - I/O EXPANSION
SHEET10 - ANALOG EXPANSION

SHEET11 - JTAG
SHEET12 - POWER
SHEET13 - PLACEMENT TOP
SHEET14 - PLACEMENT BOTTOM

The TMS320F28335 EzDSP design is based on preliminary information(SPRS439 June 2007) for the TMS320F28335 device. This schematic is subject to change without notification. Spectrum Digital Inc. assumes no liability for applications assistance, customer product design or infringement of patents described herein.

REVISION STATUS OF SHEETS

REV													
SH	1	2	3	4	5	6	7						
REV	A	A	A	A	A	A	A						
SH	8	9	10	11	12	13	14						
REV	B	A	A	A	A	A	A						
SH	1	2	3	4	5	6	7						

NEXT ASSY | USED ON | APPLICATION

PWN DATE
CHK DATE
ENGR DATE
ENGR MGR DATE
QA DATE
MFG DATE
PLGE DATE

SPECTRUM DIGITAL INCORPORATED

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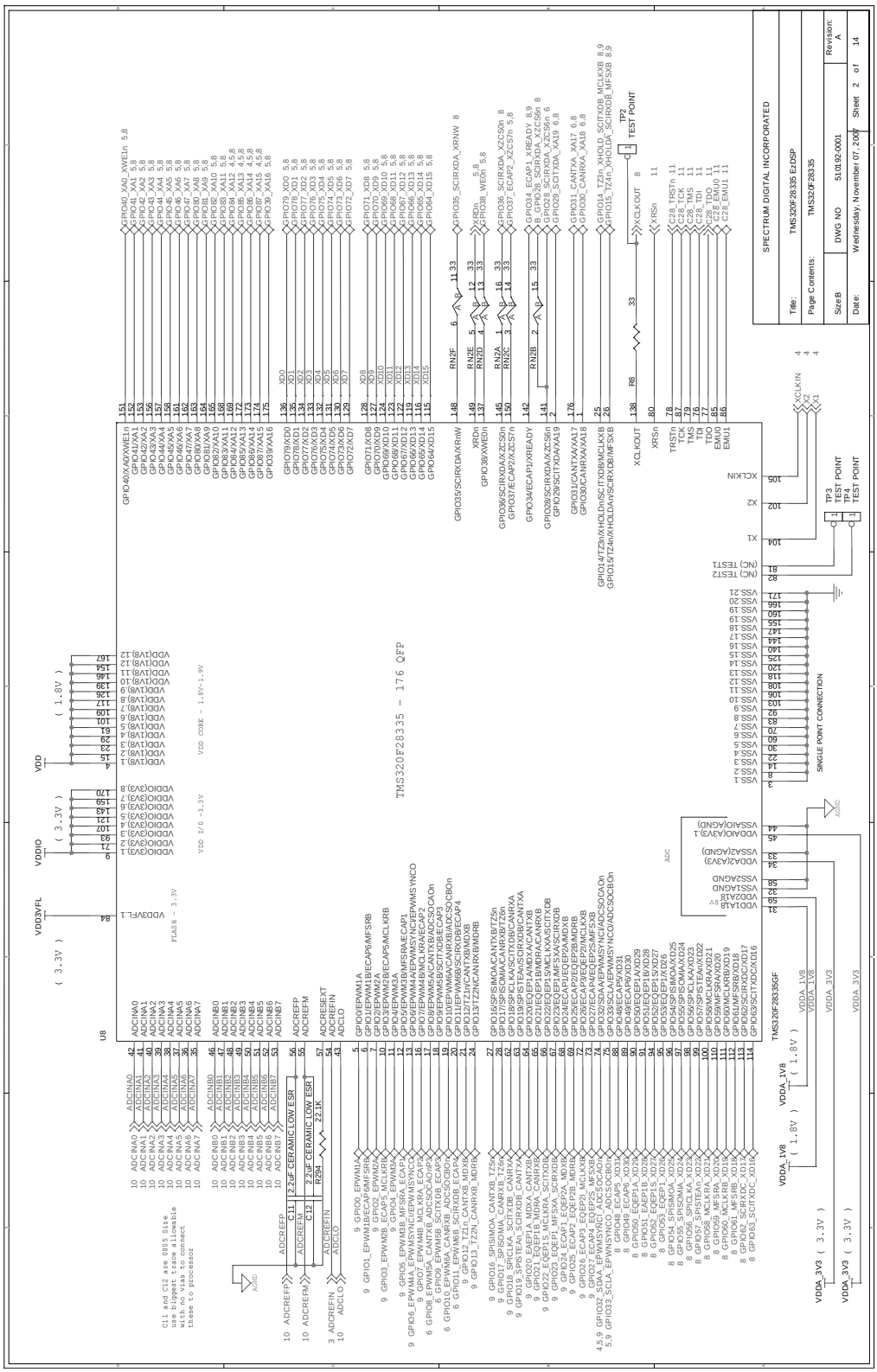
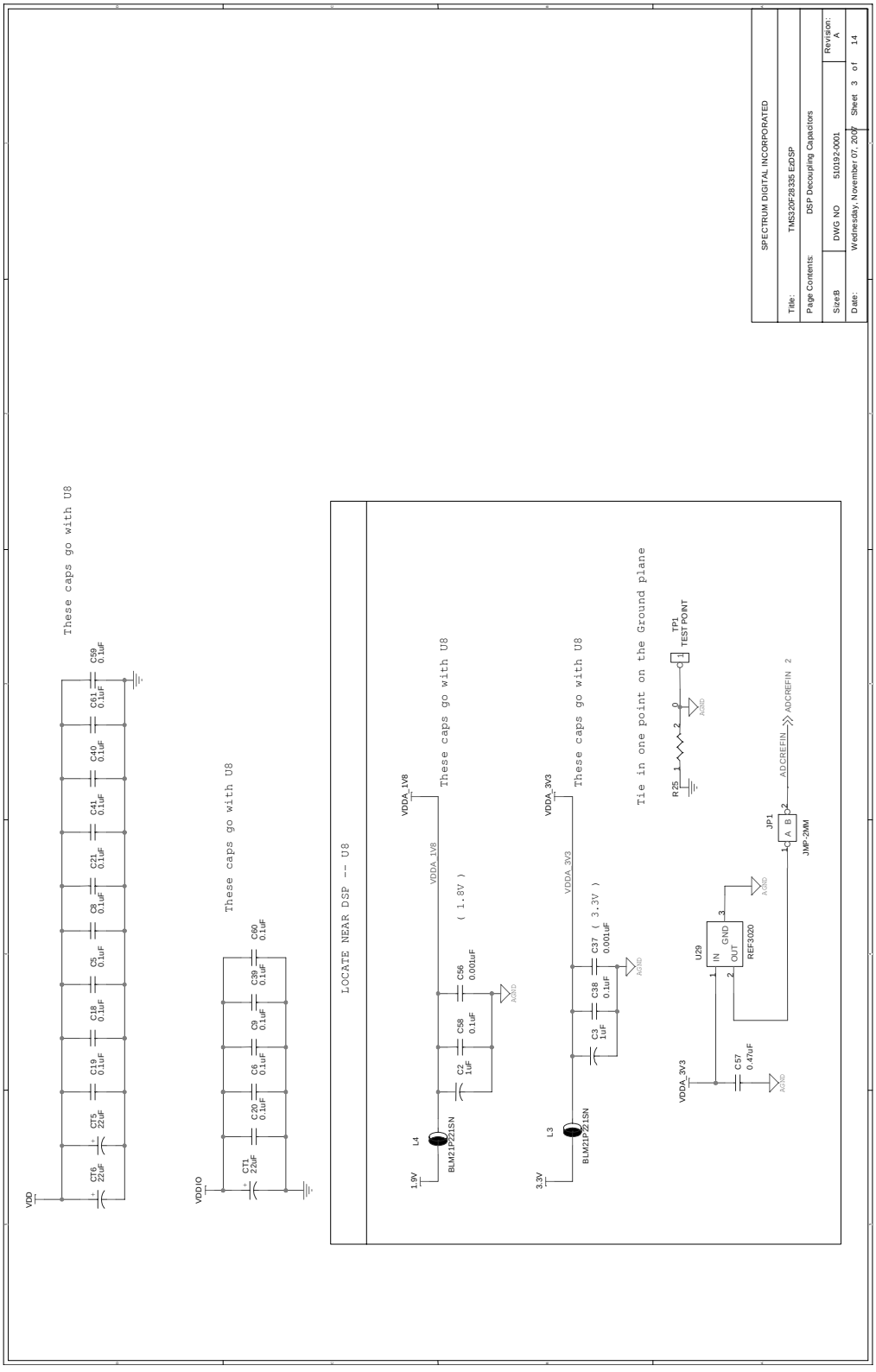
Page Contents: Title Block
Size:B | DWG NO 510192-0001 | Revision: B
Date: Wednesday, November 07, 2007 | Sheet 1 of 14




These caps go with U8
VDD
C76 22uF
C75 22uF
C19 0.1uF
C18 0.1uF
C5 0.1uF
C8 0.1uF
C21 0.1uF
C41 0.1uF
C10 0.1uF
C61 0.1uF
C59 0.1uF
These caps go with U8
VDDIO
C71 22uF
C20 0.1uF
C6 0.1uF
C9 0.1uF
C39 0.1uF
C60 0.1uF
LOCATE NEAR DSP -- U8
VDDA_1V8
These caps go with U8
(1.8V)
1.9V
L4
BLM21PZ221SN
C2 1uF
C58 0.1uF
C56 0.001uF
AGND
VDDA_3V3
These caps go with U8
(3.3V)
3.3V
L3
BLM21PZ221SN
C3 1uF
C38 0.1uF
C37 0.001uF
AGND
Tie in one point on the Ground plane
R25
TP1
TESTPOINT
AGND
JP1
A B
JMP-2MM
ADCREFIN
ADCREFIN 2
U29
IN
GND
OUT
REF3020
VDDA_3V3
C57 0.47uF
AGND
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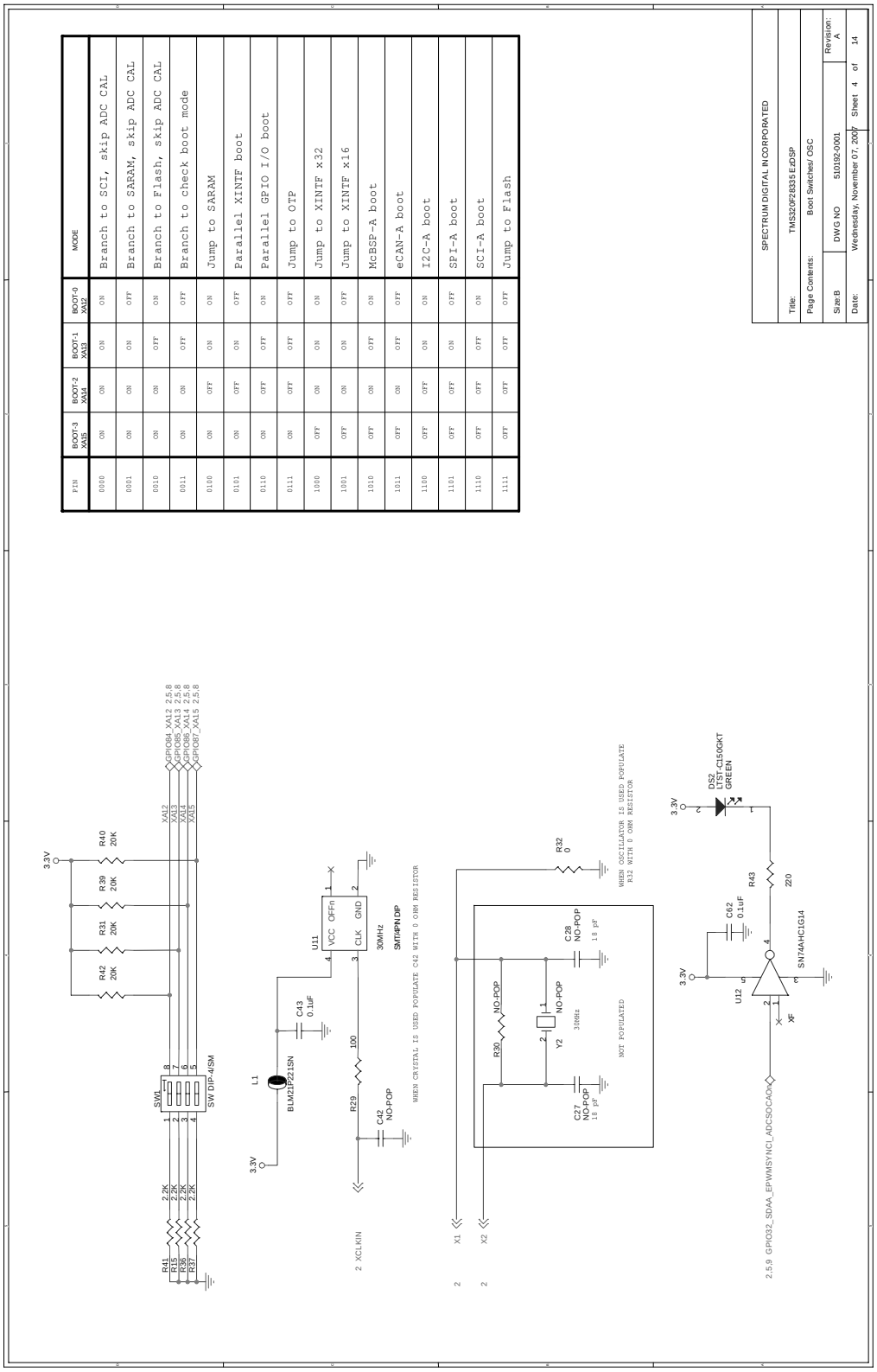
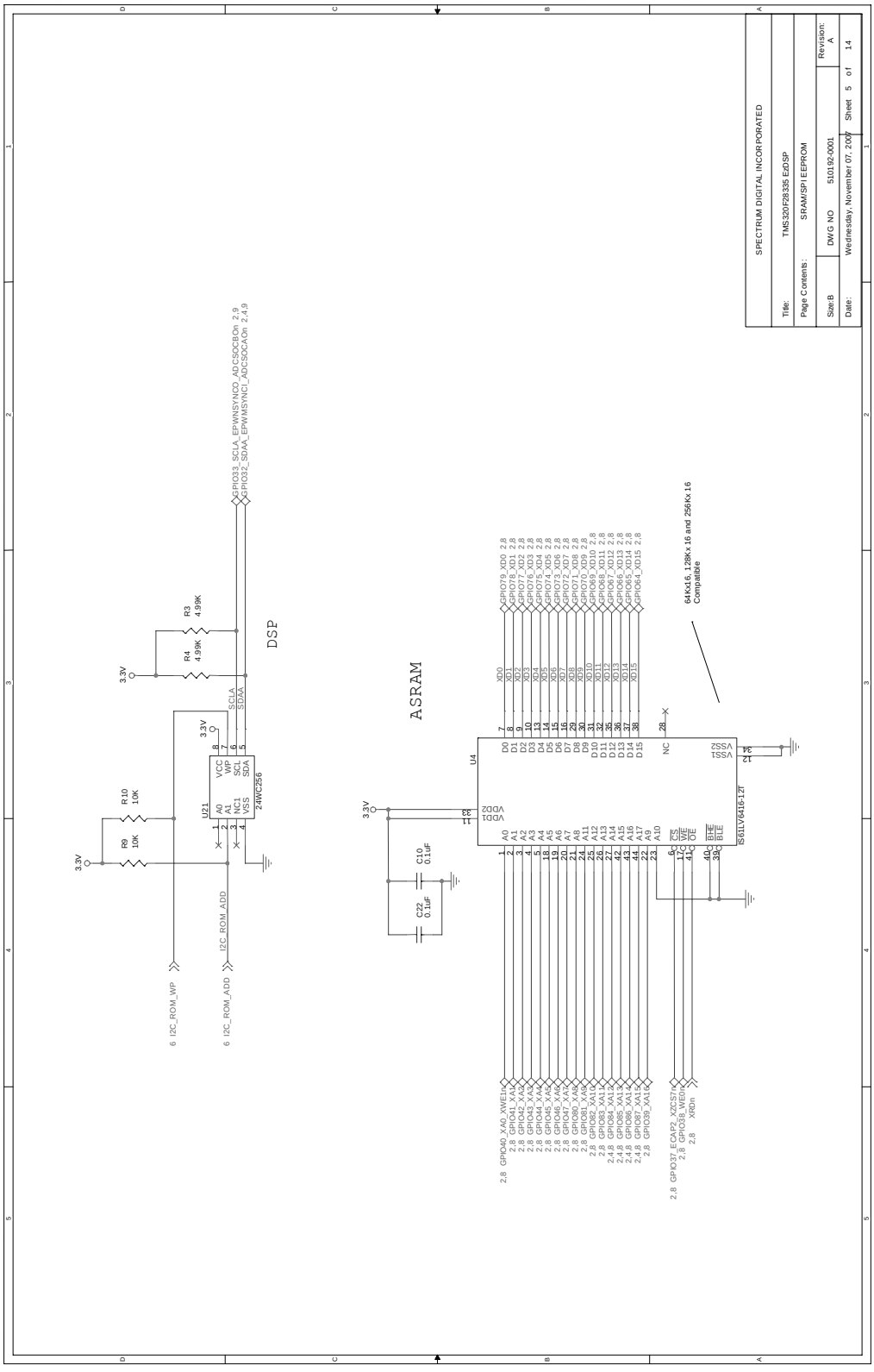
Title: TMS320F28335 EzDSP
Page Contents: DSP Decoupling Capacitors
Size:B
DWG NO 510192-0001
Revision: A
Date: Wednesday, November 07, 2007
Sheet 3 of 14



PIN	BOOT-3 XA15	BOOT-2 XA14	BOOT-1 XA13	BOOT-0 XA12	MODE
0000	ON	ON	ON	ON	Branch to SCI, skip ADC CAL
0001	ON	ON	ON	OFF	Branch to SARAM, skip ADC CAL
0010	ON	ON	OFF	ON	Branch to Flash, skip ADC CAL
0011	ON	ON	OFF	OFF	Branch to check boot mode
0100	ON	OFF	ON	ON	Jump to SARAM
0101	ON	OFF	ON	OFF	Parallel XINTF boot
0110	ON	OFF	OFF	ON	Parallel GPIO I/O boot
0111	ON	OFF	OFF	OFF	Jump to OTP
1000	OFF	ON	ON	ON	Jump to XINTF x32
1001	OFF	ON	ON	OFF	Jump to XINTF x16
1010	OFF	ON	OFF	ON	McBSP-A boot
1011	OFF	ON	OFF	OFF	eCAN-A boot
1100	OFF	OFF	ON	ON	I2C-A boot
1101	OFF	OFF	ON	OFF	SPI-A boot
1110	OFF	OFF	OFF	ON	SCI-A boot
1111	OFF	OFF	OFF	OFF	Jump to Flash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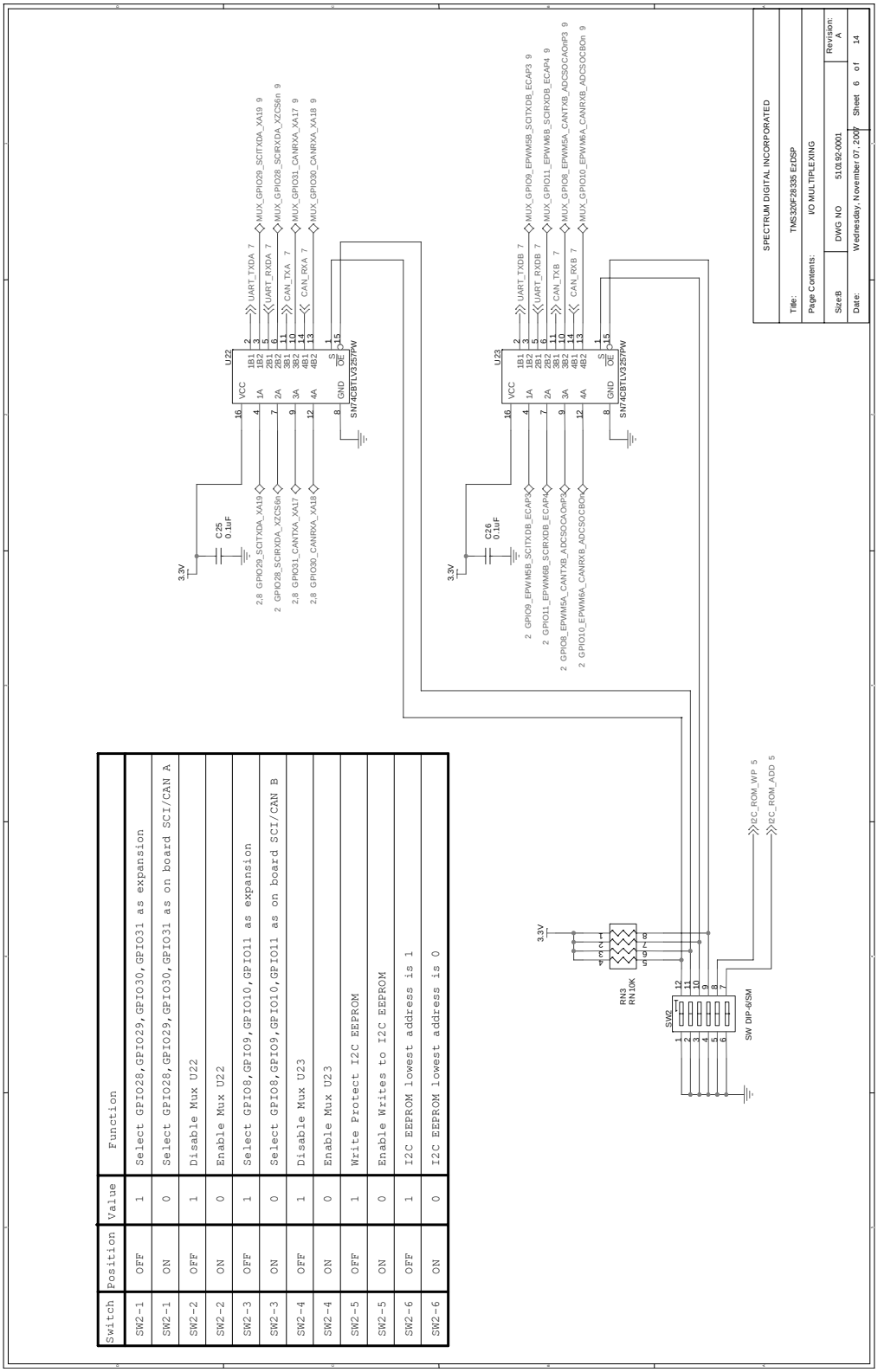
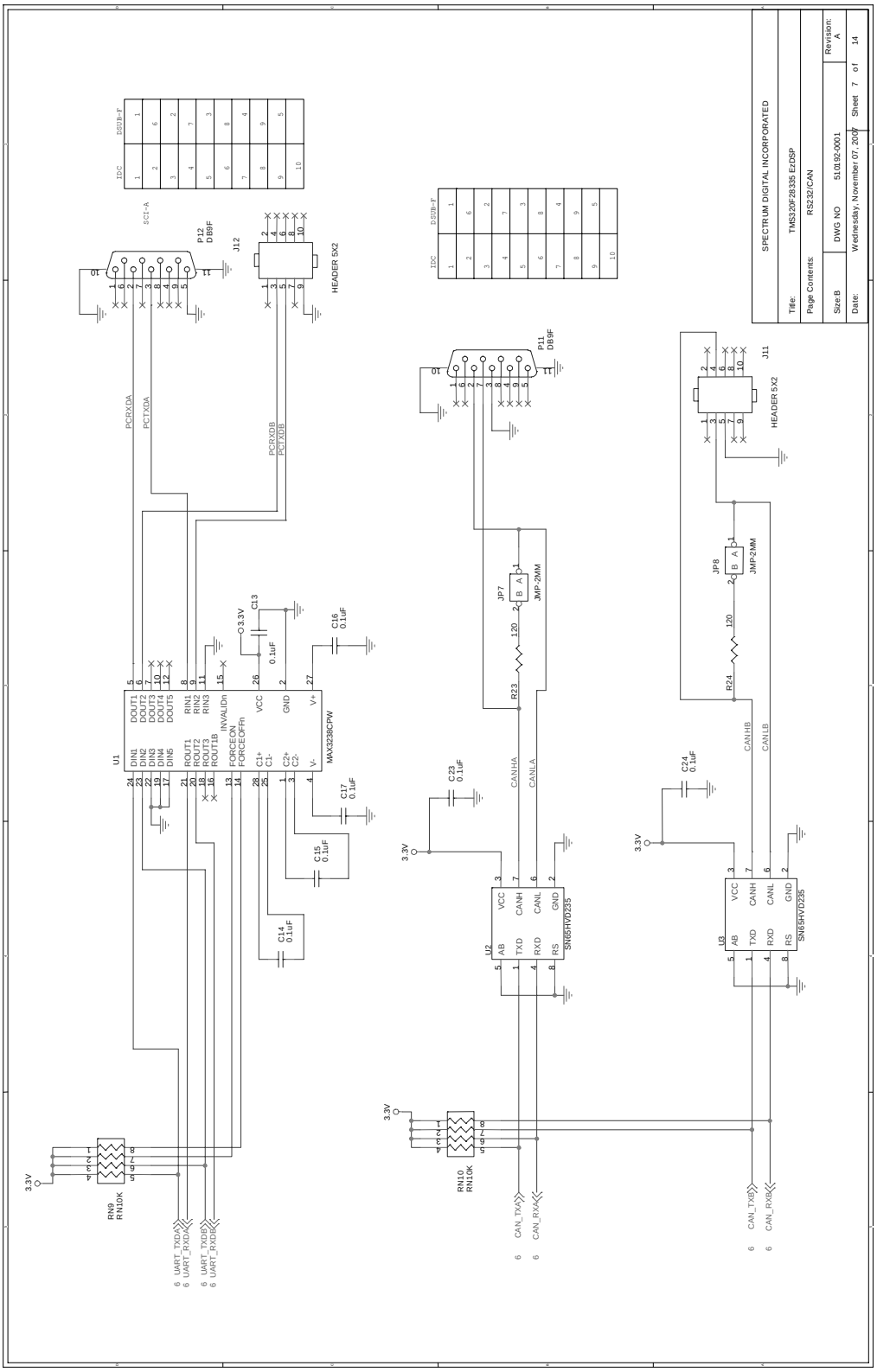
Size: B
DWG NO 5101102-0001
Revision: A
Date: Wednesday, November 07, 2007
Sheet 5 of 14
DSP
ASRAM
U4
IS61LV6416-12T
64Kx16, 128Kx 16 and 256Kx 16 Compatible
U21
24WC256
R3 4.99K
R4 4.99K
R9 10K
R10 10K
C10 0.1uF
C22 0.1uF
3.3V
SCLA
SDAA
I2C_ROM_WP
I2C_ROM_ADD
GPIO33_SCLA_EPWNSYNCO_ADCSOCBOn 2,9
GPIO32_SDAA_EPWMSYNCI_ADCSOCAOn 2,4,9



Switch	Position	Value	Function
SW2-1	OFF	1	Select GPIO28,GPIO29,GPIO30,GPIO31 as expansion
SW2-1	ON	0	Select GPIO28,GPIO29,GPIO30,GPIO31 as on board SCI/CAN A
SW2-2	OFF	1	Disable Mux U22
SW2-2	ON	0	Enable Mux U22
SW2-3	OFF	1	Select GPIO8,GPIO9,GPIO10,GPIO11 as expansion
SW2-3	ON	0	Select GPIO8,GPIO9,GPIO10,GPIO11 as on board SCI/CAN B
SW2-4	OFF	1	Disable Mux U23
SW2-4	ON	0	Enable Mux U23
SW2-5	OFF	1	Write Protect I2C EEPROM
SW2-5	ON	0	Enable Writes to I2C EEPROM
SW2-6	OFF	1	I2C EEPROM lowest address is 1
SW2-6	ON	0	I2C EEPROM lowest address is 0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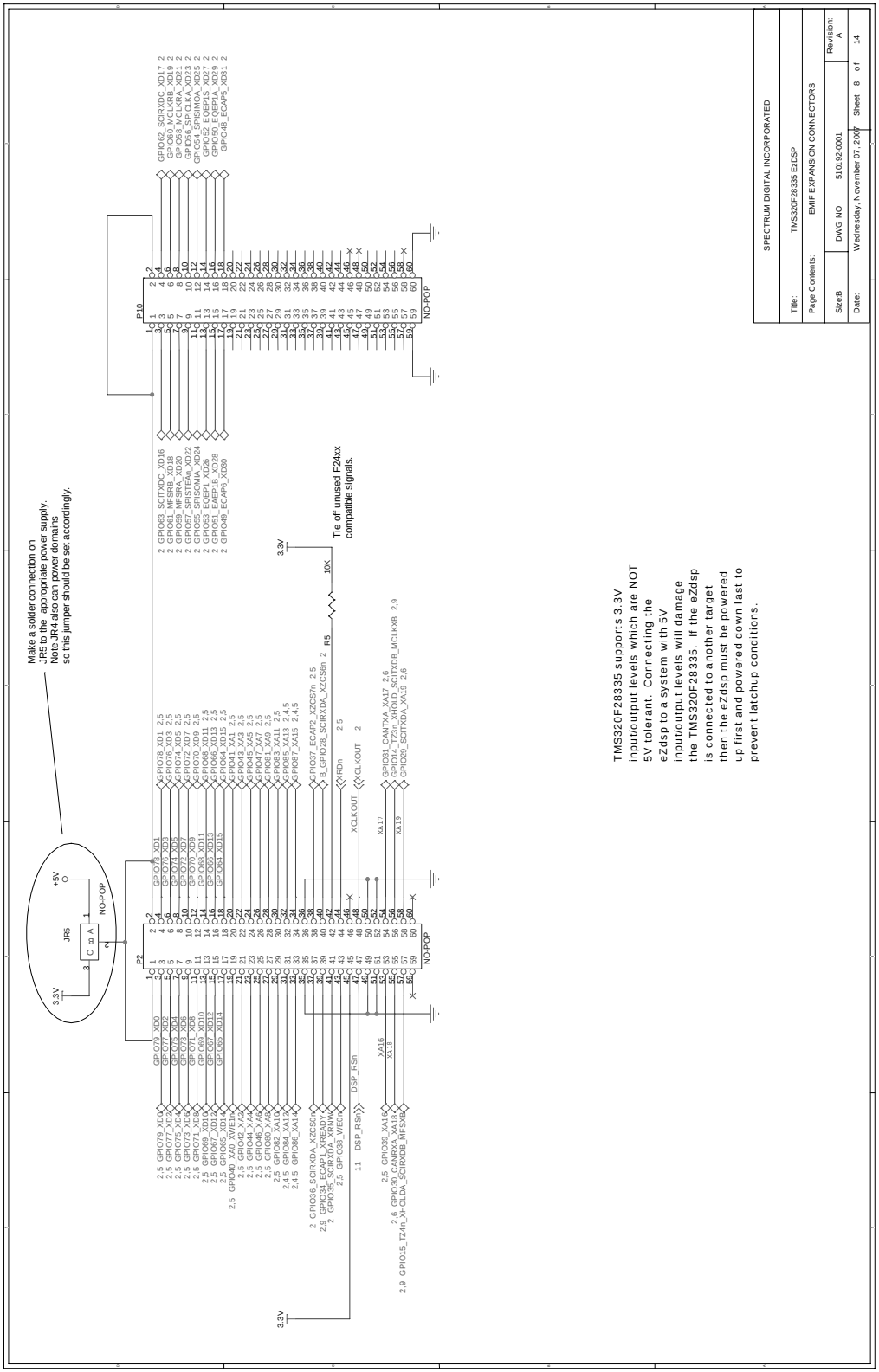
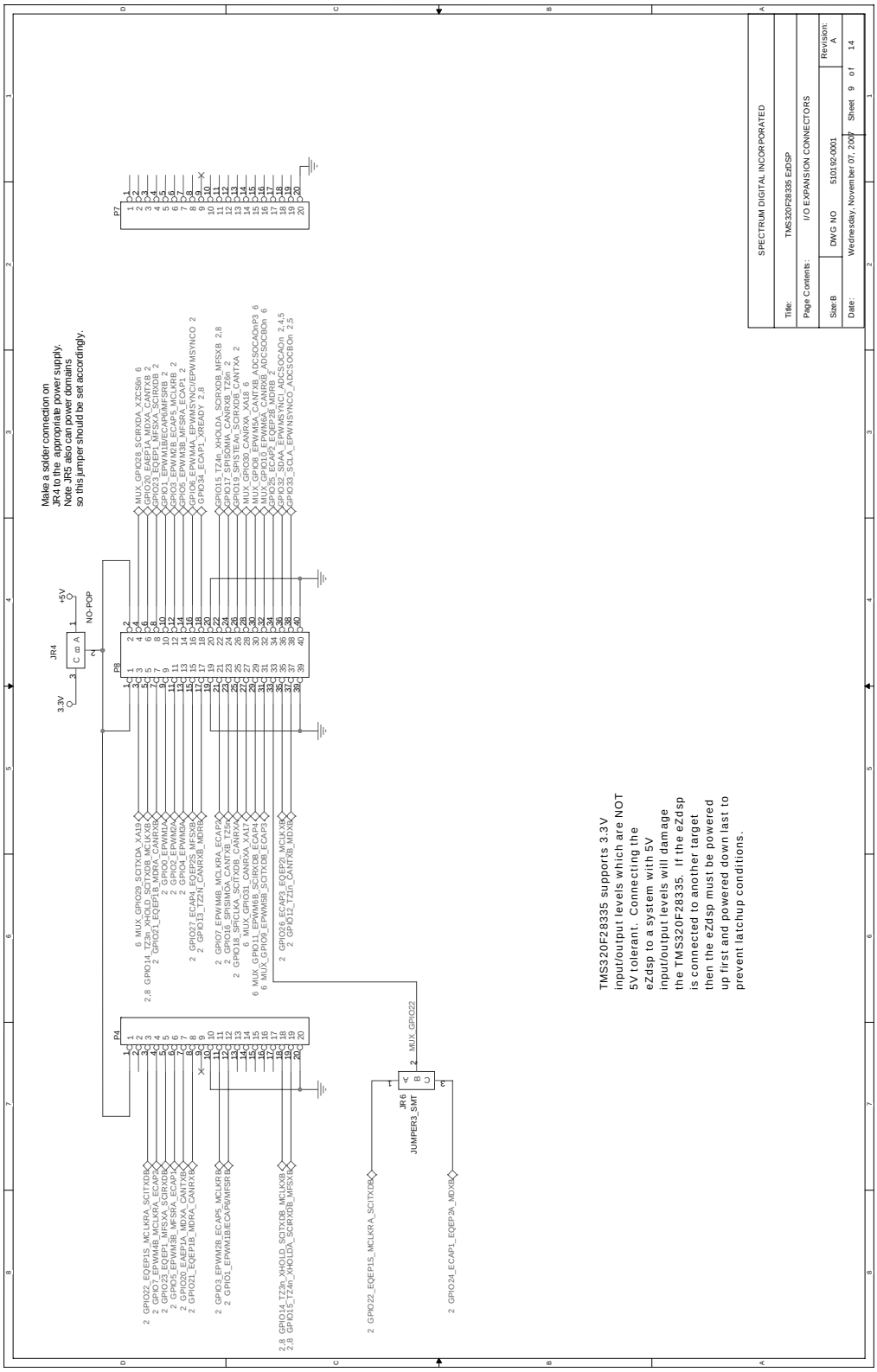
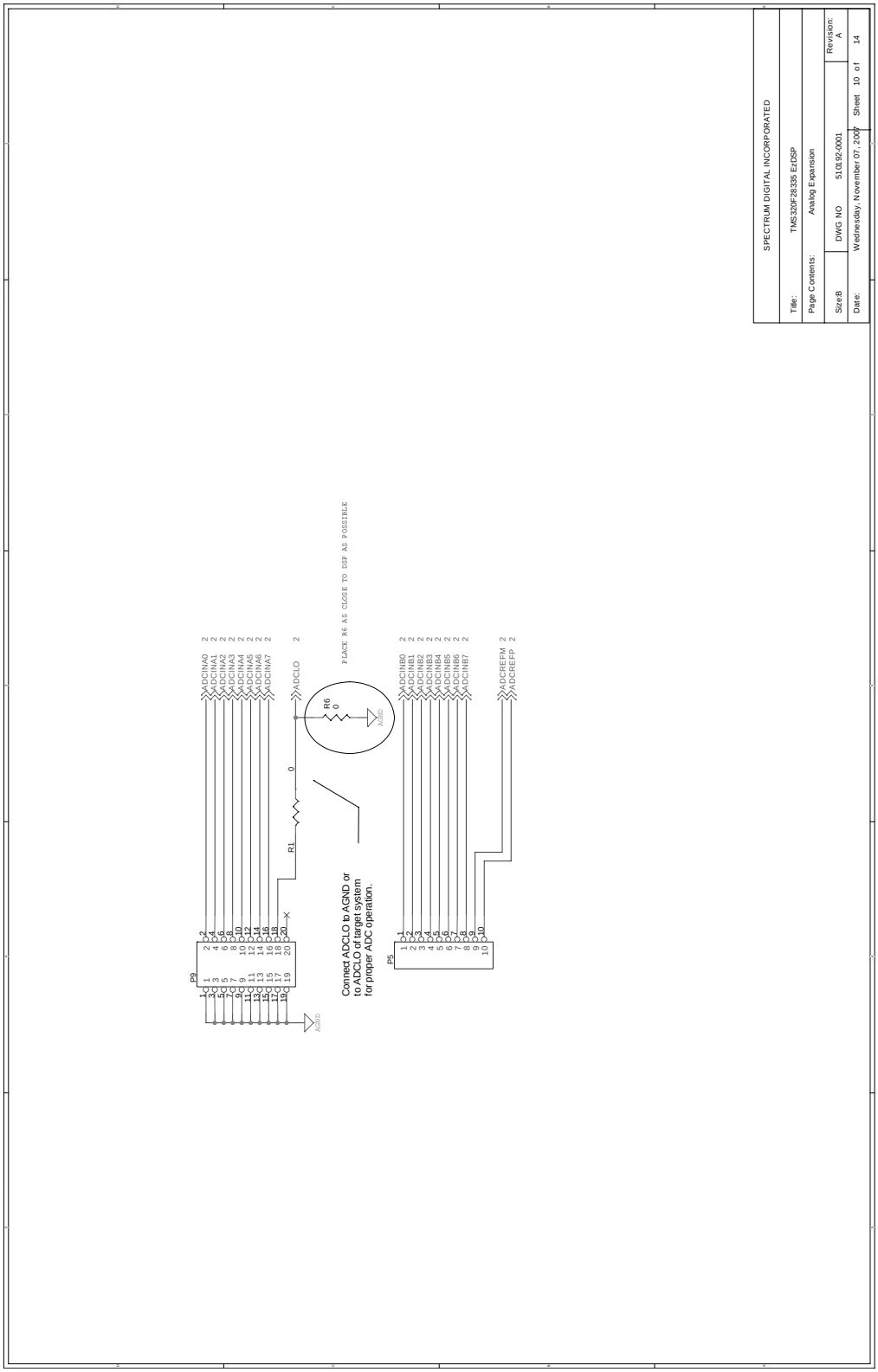
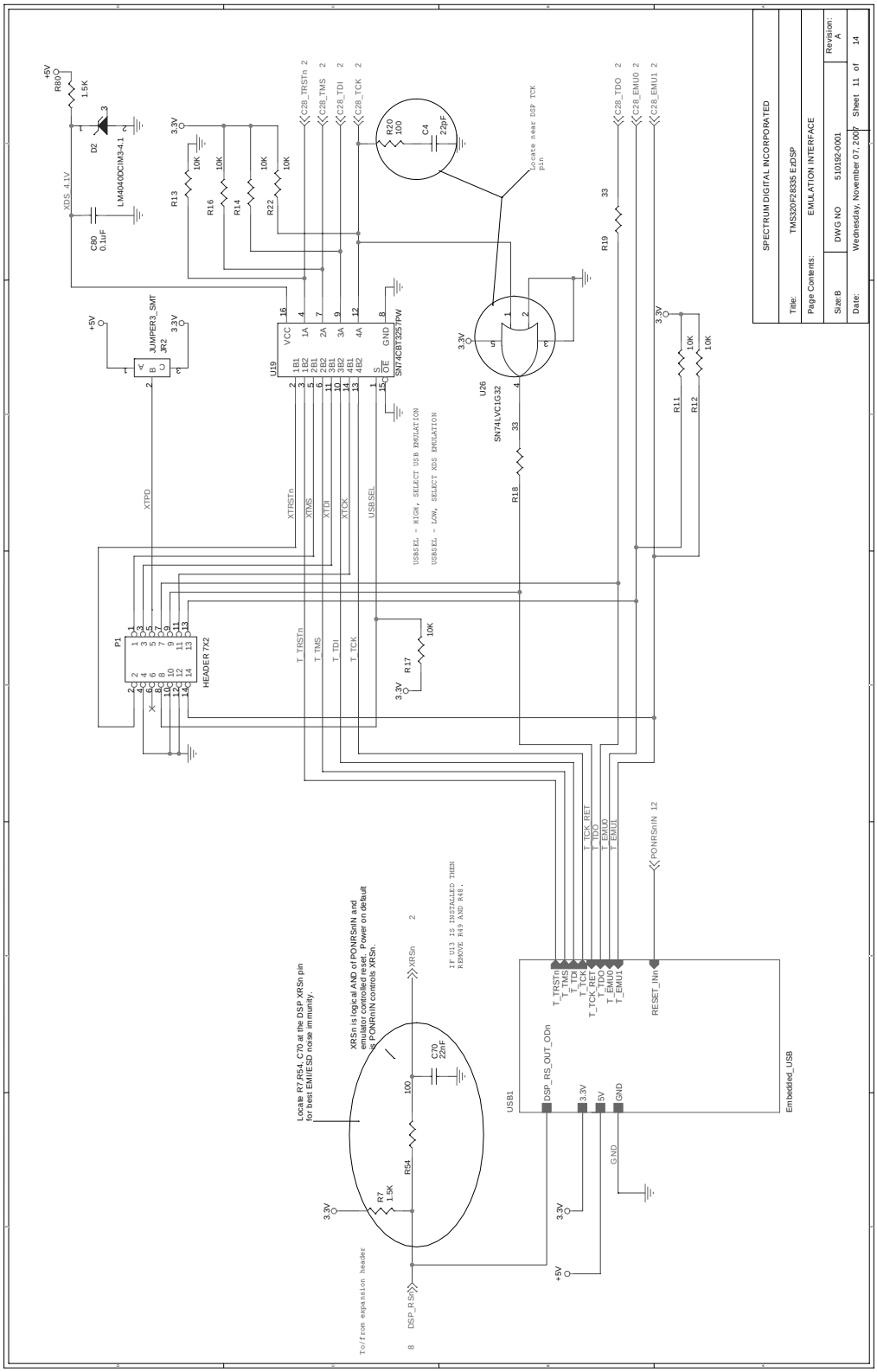
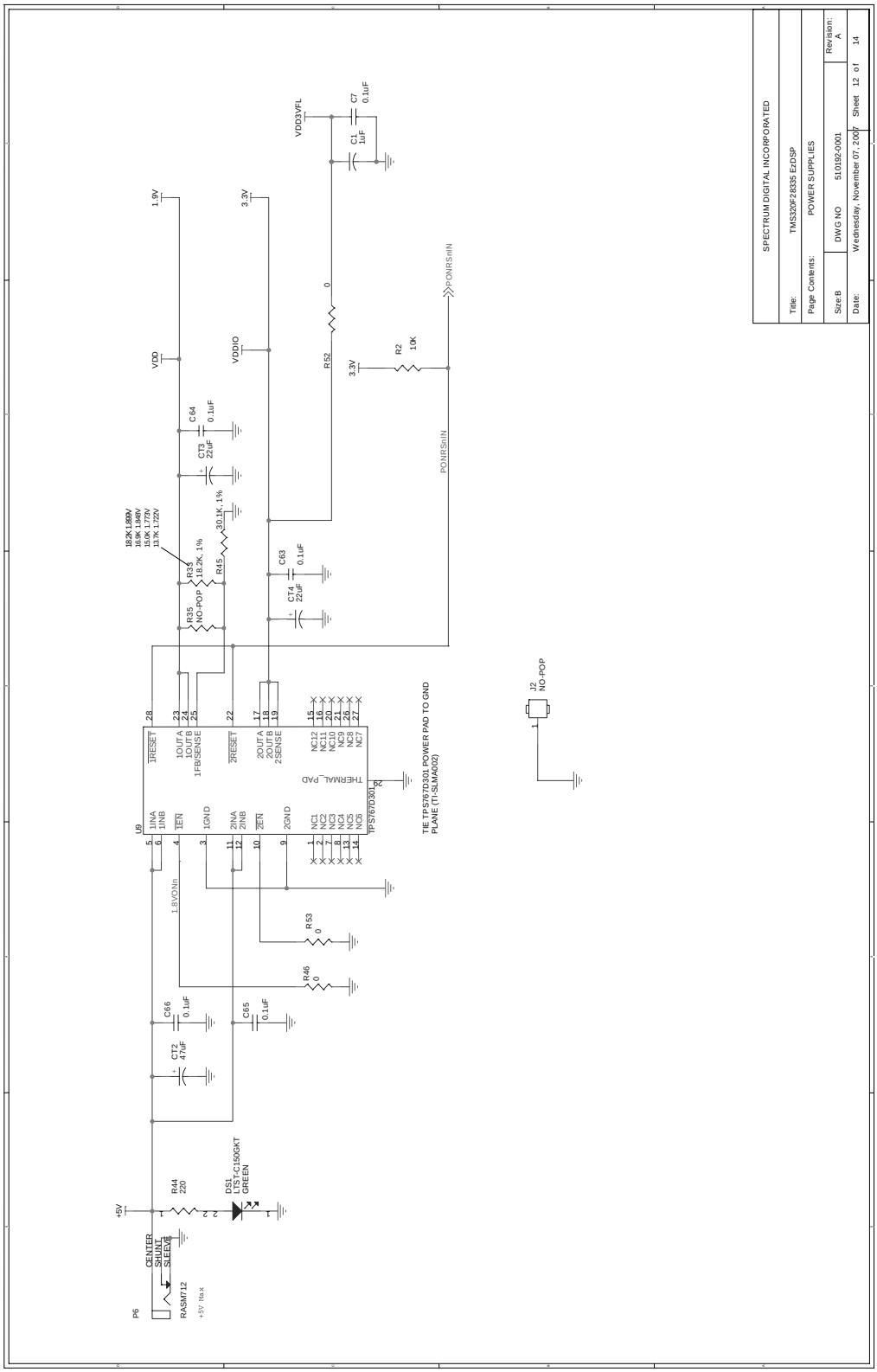
DWG NO 510192-0001
Revision: A
Date: Wednesday, November 07, 2007
Sheet 7 of 14
U1
MAX3238CPW
U2
SN65HVD235
U8
SN65HVD235
P11 DB9F
P12 DB9F
J11 HEADER 5X2
J12 HEADER 5X2
JP7 JMP-2MM
JP8 JMP-2MM
RN9 RN10K
RN10 RN10K
3.3V
C13 0.1uF
C14 0.1uF
C15 0.1uF
C16 0.1uF
C17 0.1uF
C23 0.1uF
C24 0.1uF
R23 120
R24 120
PCRXDA
PCTXDA
PCRXDB
PCTXDB
CANHA
CANLA
CANHB
CANLB
UART_TXDA
UART_RXDA
UART_TXDB
UART_RXDB
CAN_TXA
CAN_RXA
CAN_TXB
CAN_RXB

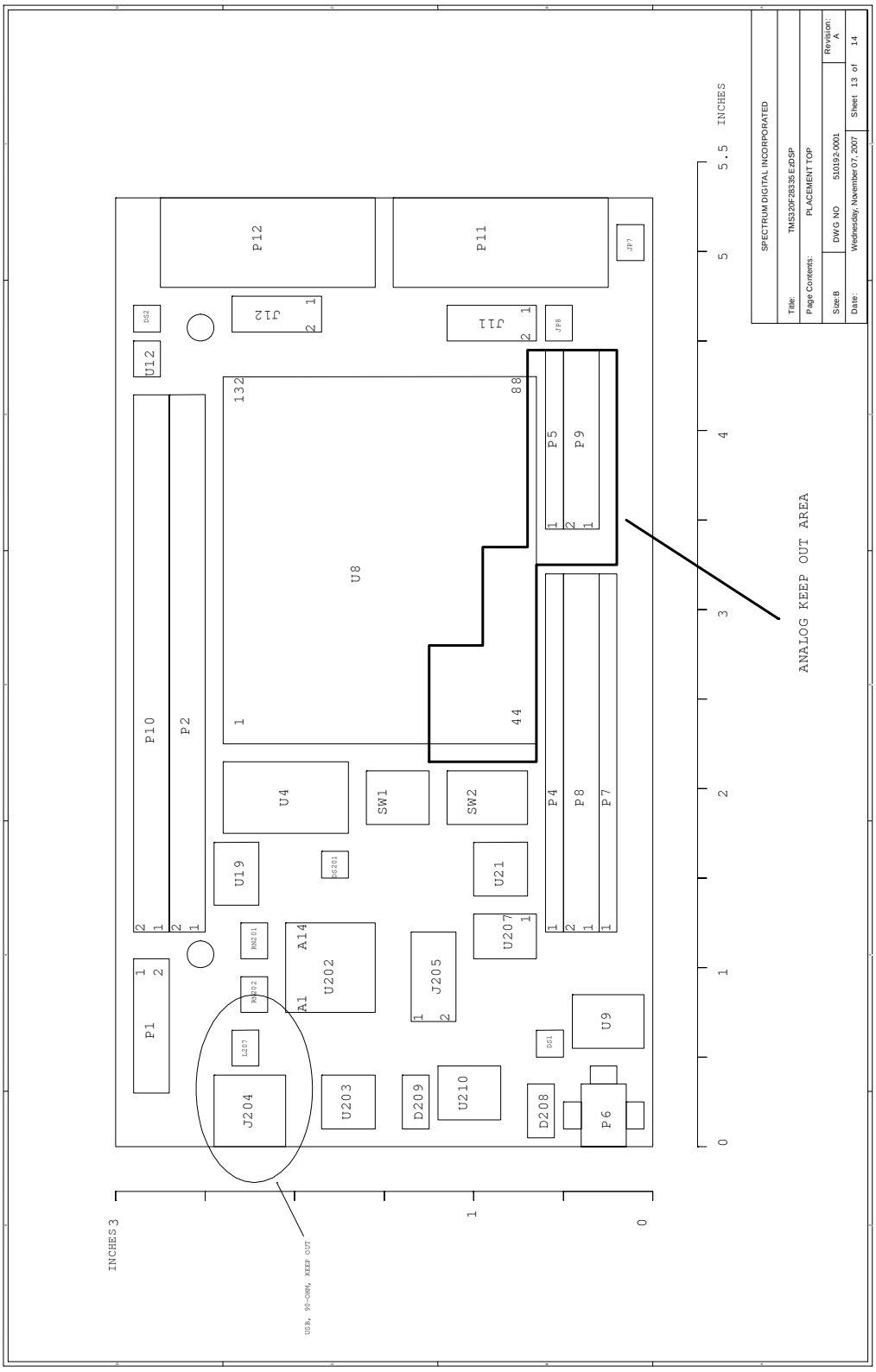

Make a solder connection on
JR5 to the appropriate power supply.
Note JR4 also can power domains
so this jumper should be set accordingly.
Tie off unused F24xx
compatible signals.
TMS320F28335 supports 3.3V
input/output levels which are NOT
5V tolerant. Connecting the
eZdsp to a system with 5V
input/output levels will damage
the TMS320F28335. If the eZdsp
is connected to another target
then the eZdsp must be powered
up first and powered down last to
prevent latchup conditions.
SPECTRUM DIGITAL INCORPORATED
TMS320F28335 EzDSP
EMIF EXPANSION CONNECTORS
5102-0001
Wednesday, November 07, 2007

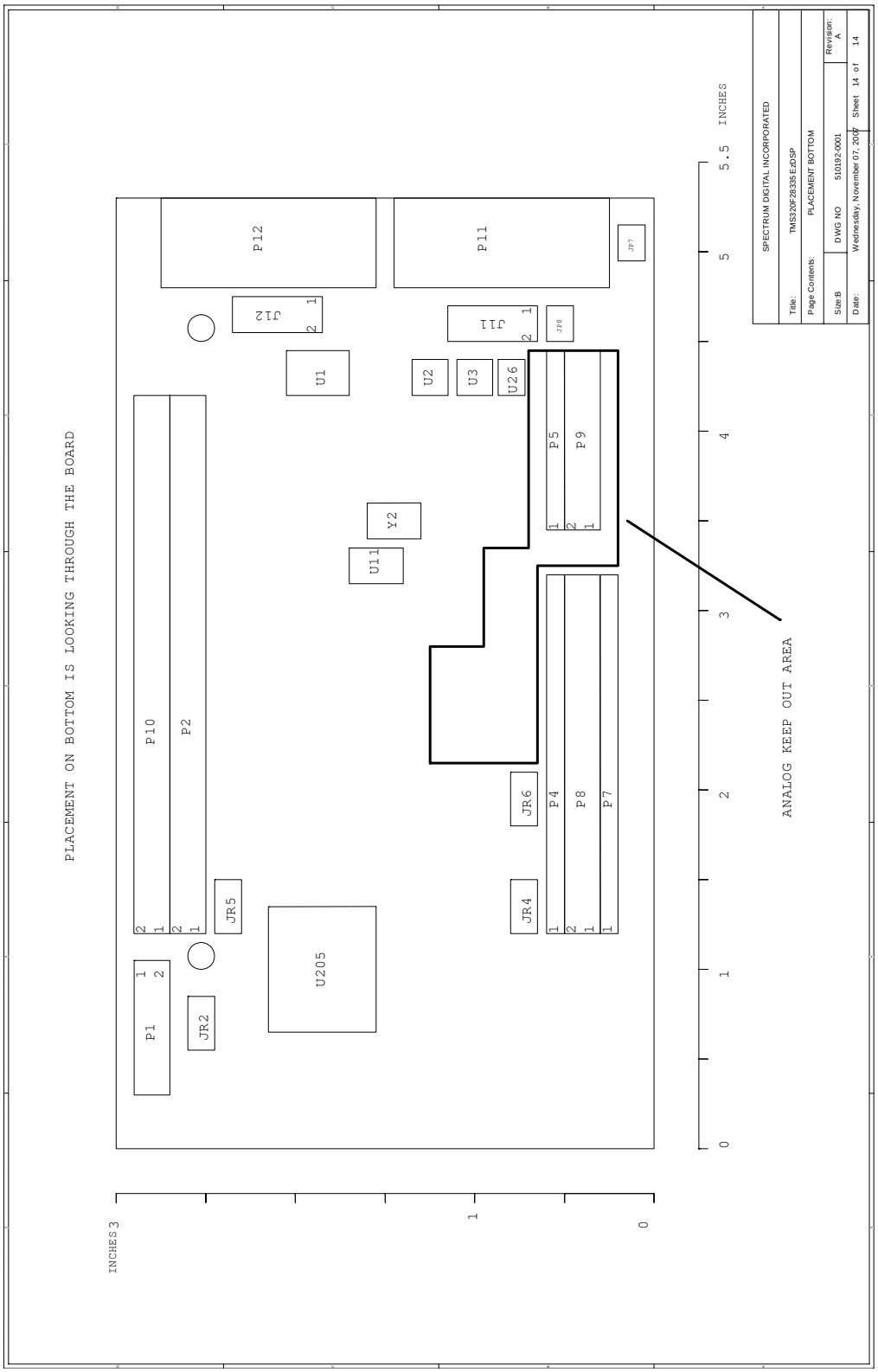

Make a solder connection on JR4 to the appropriate power supply.
Note: JR5 also can power domains so this jumper should be set accordingly.
JR4
3.3V
+5V
NO-POP
P8
P7
P4
JR6
JUMPER3_SMT
MUX_GPIO22
TMS320F28335 supports 3.3V input/output levels which are NOT 5V tolerant. Connecting the eZdsp to a system with 5V input/output levels will damage the TMS320F28335. If the eZdsp is connected to another target then the eZdsp must be powered up first and powered down last to prevent latchup conditions.
SPECTRUM DIGITAL INCORPORATED
Title: TMS320F28335 EzDSP
Page Contents: I/O EXPANSION CONNECTORS
Size:B
DWG NO 5101102-0001
Revision: A
Date: Wednesday, November 07, 2007
Sheet 9 of 14


SPECTRUM DIGITAL INCORPORATED
Title: TMS320F2833x EzDSP
Page Contents: Analog Expansion
Size:B
DWG NO 510.92-0001
Revision: A
Date: Wednesday, November 07, 2007
Sheet 10 of 14
P9
P5
R1
0
R6
0
ADCLO
PLACE R6 AS CLOSE TO DSP AS POSSIBLE
Connect ADCLO to AGND or to ADCLO of target system for proper ADC operation.
ADCINA0
ADCINA1
ADCINA2
ADCINA3
ADCINA4
ADCINA5
ADCINA6
ADCINA7
ADCINB0
ADCINB1
ADCINB2
ADCINB3
ADCINB4
ADCINB5
ADCINB6
ADCINB7
ADCREFM
ADCREFP
AGND


SPECTRUM DIGITAL INCORPORATED
Title: TMS320F28335 eZDSP
Page Contents: EMULATION INTERFACE
Size:B DWG NO 510192-0001 Revision: A
Date: Wednesday, November 07, 2007 Sheet 11 of 14
XDS_4.1V
LM4040DCIM3-4.1
C60 0.1uF
R60 1.5K
D2
R13 10K
R16 10K
R14 10K
R22 10K
C28_TRSTn 2
C28_TMS 2
C28_TDI 2
C28_TCK 2
R20 100
C4 22pF
Locate near DSP TCK pin
C28_TDO 2
C28_EMU0 2
C28_EMU1 2
R19 33
JUMPER3_SMT
JR2
U19 SN74CBT3257PW
U26 SN74LVC1G32
R18 33
R11 10K
R12 10K
XTPD
XTRSTn
XTMS
XTDI
XTCK
USBSEL
USBSEL - HIGH, SELECT USB EMULATION
USBSEL - LOW, SELECT XDS EMULATION
P1 HEADER 7X2
T_TRSTn
T_TMS
T_TDI
T_TCK
R17 10K
T_TCK_RET
T_TDO
T_EMU0
T_EMU1
PONRSnIN 12
Locate R7,R54, C70 at the DSP XRSn pin for best EMI/ESD noise immunity.
XRSn is logical AND of PONRSnIN and emulator controlled reset. Power on default is PONRnIN controls XRSn.
IF U13 IS INSTALLED THEN REMOVE R49 AND R48.
XRSn 2
C70 22pF
100
R54
R7 1.5K
DSP_RS
To/from expansion header
USB1
DSP_RS_OUT_ODn
RESET_INn
Embedded_USB


SPECTRUM DIGITAL INCORPORATED
Title: TMS320F28335 EzDSP
Page Contents: POWER SUPPLIES
Size:B
DWG NO 510192-0001
Revision: A
Date: Wednesday, November 07, 2007
Sheet 12 of 14
VDD3VFL
C7 0.1uF
C1 1uF
1.9V
3.3V
VDD
VDDIO
R52 0
R2 10K
PONRSnIN
C64 0.1uF
CT3 22uF
R35 18.2K, 1%
R45 30.1K, 1%
R35 NO-POP
C63 0.1uF
CT4 22uF
U9
TPS767D301
1RESET
1OUT A
1OUT B
1FB/SENSE
2RESET
2OUT A
2OUT B
2SENSE
THERMAL_PAD
1IN A
1IN B
1EN
1GND
2IN A
2IN B
2EN
2GND
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
NC9
NC10
NC11
NC12
TIE TPS767D301 POWER PAD TO GND PLANE (TI-SLMA002)
J2 NO-POP
1.8VDNn
R53 0
R46 0
C66 0.1uF
C65 0.1uF
CT2 47uF
+5V
R44 220
DS1 LTST-C150GKT GREEN
P6
CENTER SHUNT SLEEVE
RASM712
+5V Max

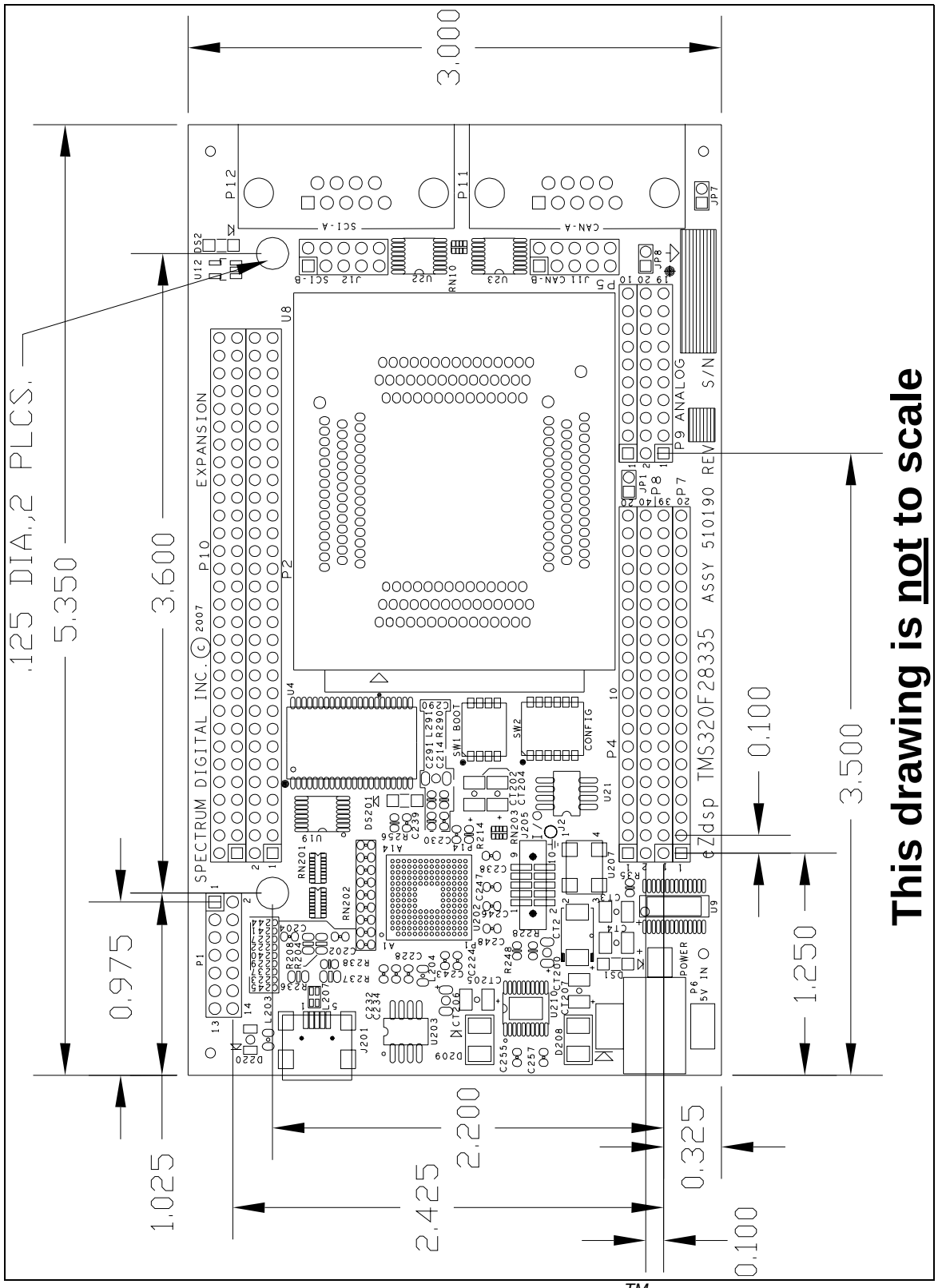

SPECTRUM DIGITAL INCORPORATED
Title: TMS320F28335 eZDSP
Page Contents: PLACEMENT TOP
Size:B
DWG NO 510192-0001
Revision: A
Date: Wednesday, November 07, 2007
Sheet 13 of 14
ANALOG KEEP OUT AREA
USB, 90-OHM, KEEP OUT
INCHES
P12
P11
P10
P2
P1
P5
P9
P8
P4
P7
U8
U4
U19
U21
U207
U202
U203
U210
U9
J204
J205
J12
J11
SW1
SW2
P6
D208
D209


PLACEMENT ON BOTTOM IS LOOKING THROUGH THE BOARD
ANALOG KEEP OUT AREA
INCHES
INCHES
P12
P11
P10
P2
P1
P5
P9
P4
P8
P7
J12
J11
U1
U2
U3
U26
Y2
U11
U205
JR2
JR4
JR5
JR6
JP7
JP8
SPECTRUM DIGITAL INCORPORATED
Title: TMS320F28335 EZDSP
Page Contents: PLACEMENT BOTTOM
Size:B
DWG NO 510192-0001
Revision: A
Date: Wednesday, November 07, 2007
Sheet 14 of 14

Appendix B

eZdsp™ F28335 Mechanical Information

This appendix contains the mechanical information about the socketed and unsocketed versions of the eZdsp™ F28335


3.000
.125 DIA.,2 PLCS.
5.350
3.600
0.975
1.025
2.200
2.425
0.325
0.100
1.250
3.500
0.100
This drawing is not to scale
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EXPANSION
ASSY 510190 REV
S/N
TMS320F28335
P1
P2
P4
P5
P6
P7
P8
P9 ANALOG
P10
P11
P12
U8
U4
U21
U9
SW1 BOOT
SW2
CONFIG
POWER
5V IN

[redacted]

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